FEELING TECHNOLOGY

FM8P73B

EPROM-Based 8-Bit Microcontroller with 10 bit ADC

Devices Included in this Data Sheet:

- FM8P73BA : 16-pin EPROM device
- FM8P73BB : 14-pin EPROM device
- FM8P73BC : 18-pin EPROM device with VR pin
- FM8P73BD : 16-pin EPROM device with VR pin

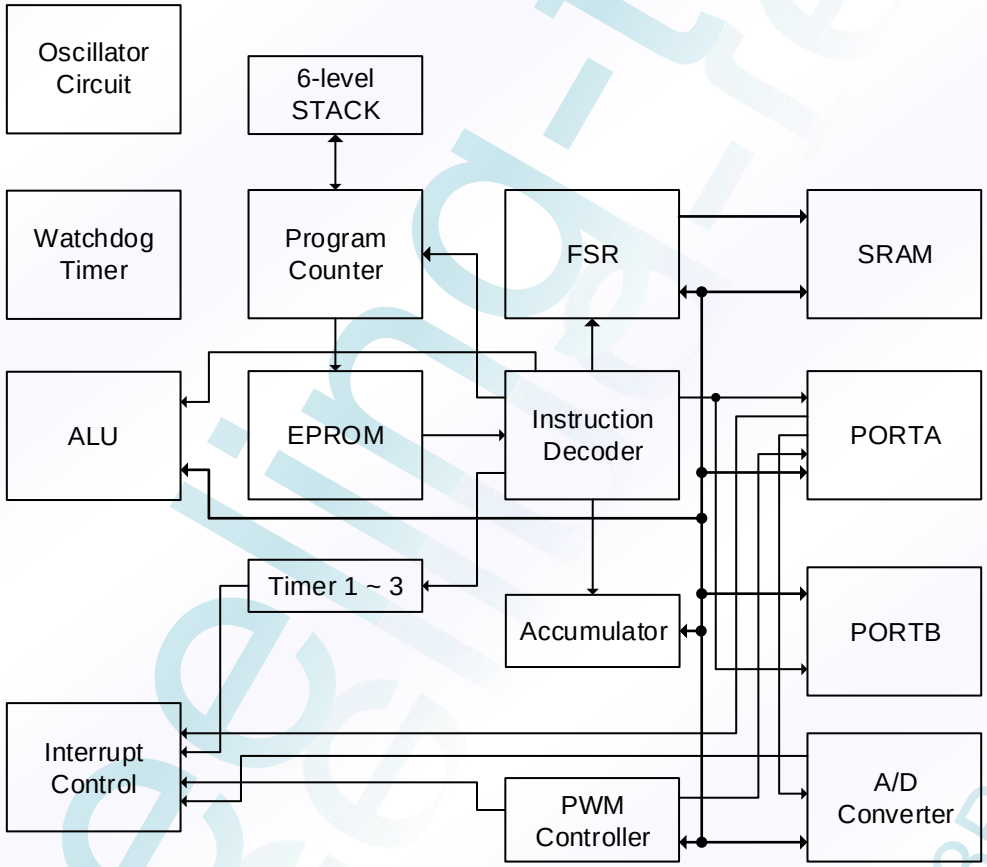
FEATURES

- Total 11 channel 10bit AD converter with ±2LSB resolution
- All instructions are single cycle except for program branches which are two-cycles
- 14-bit wide instructions
- Configurable CPU clock per instruction cycle: Focs/4 and Fosc/2
- All EPROM area GOTO instruction
- All EPROM area subroutine CALL instruction
- 8-bit wide data path
- 6-level deep hardware stack
- 1K x 14 bits on chip EPROM
- 27x8 bits on chip special purpose registers and 64 x 8 bits on chip general purpose registers (SRAM)
- Operating speed: DC-20 MHz clock input, or DC-100 ns instruction cycle
- Direct, indirect addressing modes for data accessing
- Three real time down-count Timer with 3-bit programmable prescaler
  - TMR1: 8-bit, PWM1(Period) & Timer
  - TMR2: 8-bit, PWM1(Duty) & Timer
  - TMR3: 8-bit Timer
- Built-in 3 levels Low Voltage Detector (LVDT) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation.
- Two I/O ports IOA, and IOB with independent direction control
  - 13 Bi-direction I/O port (Programmable Pull-up enable in Input mode)
  - One Input only port (IOB3/RSTB)
- Four kinds of interrupt source: 3 Timers, 8 external interrupt sources: IOB0~IOB7, Internal watchdog timer (i_WDT) wakeup, and A/D end of conversion
- Wake-up from SLEEP:
  - Port B (IOB0~IOB7) pin change wakeup
  - WDT overflow
  - i_WDT overflow
- Power saving SLEEP mode
- Programmable Code Protection
- Selectable oscillator options:
  - ERC: External Resistor/ Voltage Controlled Oscillator
  - XT: Crystal/Resonator Oscillator
  - HF: High Frequency Crystal/Resonator Oscillator
  - LF: Low Frequency Crystal Oscillator
  - IRC: Internal Resistor/Capacitor Oscillator
- Wide-operating voltage range:
  - EPROM : 2.2V to 5.5V

GENERAL DESCRIPTION

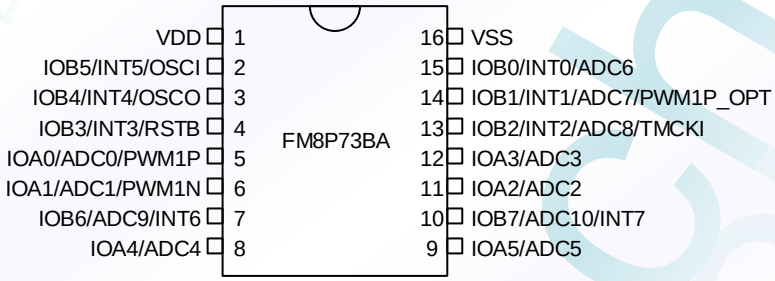
The FM8P73B is a low-cost, high speed, high noise immunity, EPROM-based 8-bit CMOS microcontrollers. It employs a RISC architecture with 33 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The FM8P73B consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Watchdog Timer, EPROM, SRAM, tri-state I/O port, I/O pull-high control, Power saving SLEEP mode, 3 real time programmable clock/counter, Interrupt, Wake-up from SLEEP mode, and Code Protection for EPROM products. There are five oscillator configurations to be chosen from, including the power-saving LF (Low Frequency) oscillator and cost saving internal RC oscillator.
The FM8P73B address 1K×14 of program memory.
The FM8P73B can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.
The FM8P73B provides total 11 channel 10bit AD converter with ±2LSB resolution.

BLOCK DIAGRAM

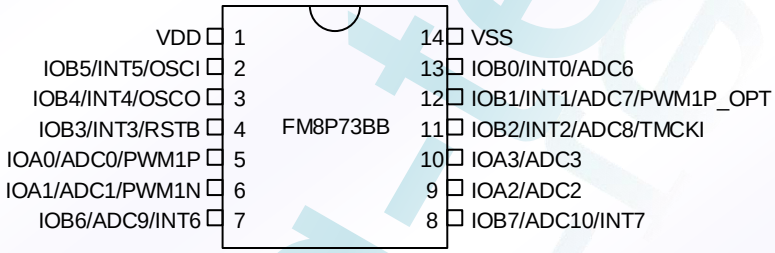


PIN CONNECTION

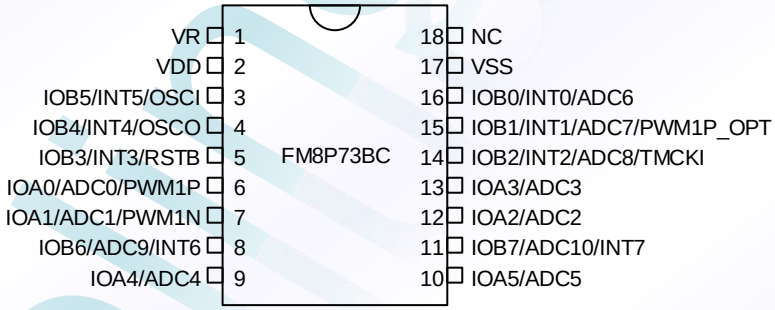
PDIP16, SOP16



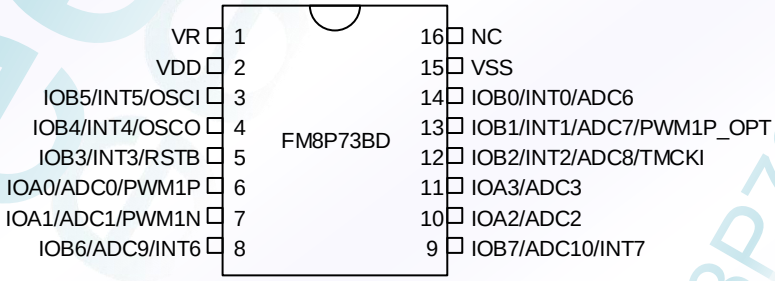
PDIP14, SOP14



PDIP18, SOP18 (With VR PIN)



PDIP16, SOP16 (With VR PIN)



PIN DESCRIPTIONS

Name	I/O	Description
IOA0 ~ IOA5	I/O	• Bi-direction I/O pin • Software controlled pull-high • A/D converter input • IOA0 is PWM1P output (by option, default) • IOA1 is PWM1N output (by option)
IOB0 ~ IOB2	I/O	• Bi-direction I/O pin with system wake-up/pin change interrupt function • Software controlled pull-high • A/D converter input • IOB1 is PWM1P output(by option) • IOB2 is External CLK input for Timer
IOB3/RSTB	I	• Input pin only with system wake-up/pin change interrupt function; **voltage on this pin must not exceed VDD.** • System clear (RESET) input. This pin is an active low RESET to the device
IOB4/OSCO	I/O	• Bi-direction I/O port with system wake-up/pin change interrupt function • Software controlled pull-high • Oscillator output (HF, XT, LF, ERC mode)
IOB5/OSCI	I/O	• Bi-direction I/O port with system wake-up/pin change interrupt function (IRC mode) • Software controlled pull-high • Oscillator input (HF, XT, LF, ERC mode)
IOB6 ~ IOB7	I/O	• Bi-direction I/O pin with system wake-up/pin change interrupt function • Software controlled pull-high • A/D converter input
VR	-	ADC module reference input, **voltage on this pin must not exceed VDD.**
VDD	-	Positive supply
VSS	-	Ground

Legend: I=input, O=output, I/O=input/output

Note: Please refer to 2.2 for detail IO type description

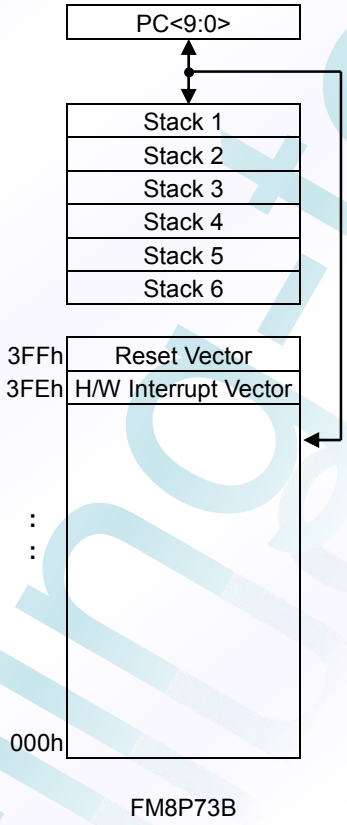
1.0 MEMORY ORGANIZATION

FM8P73B memory is organized into program memory and data memory.

1.1 Program Memory Organization

The FM8P73B has a 10-bit Program Counter capable of addressing a 1K×14 program memory space.
The RESET vector for the FM8P73B is at 3FFh.
The H/W interrupt vector is at 3FEh.
User can use “CALL/GOTO” instructions to program user's code within entire program area.

Figure 1.1: Program Memory Map and STACK



1.2 Data Memory Organization

Data memory is composed of 27 bytes Special Function Registers and 64 bytes General Purpose Registers. The data memory can be accessed either directly or indirectly through the FSR register.

Table 1.1: Registers File Map for FM8P73B

Address	Description
00h : : 24h	Special Purpose Register
30h : : 6Fh	General Purpose Register

Table 1.2: Special Purpose Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
System									
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
02h (r/w)	PCL	Low order 8 bits of PC							
03h (r/w)	STATUS	-	-	PS	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h (r/w)	FSR	0	Indirect data memory address pointer						
IO PAD & CONTROL									
05h (r/w)	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
06h (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
07h (r/w)	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	-	IOSTB2	IOSTB1	IOSTB0
08h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
Timer1: 8-bit Timer & PWM1 Period									
0Bh (r/w)	T1CON	T1EN	T1LOAD	T1SO1	T1SO0	T1EDG	T1PS2	T1PS1	T1PS0
0Ch (r/w)	PWM1CON	T12MOD	PWMS	POPS	-	PIR13	PIR12	PIR11	PIR10
0Dh (r/w)	T1LA	8-bit real-time timer Latch							
14h (r/w)	SYNPWM	SYNEN	PINV	DISN	-	-	-	DELS1	DELS0
Timer2: 8-bit Timer & PWM1 Duty									
0Fh (r/w)	T2CON	T2EN	T2LOAD	T2SO1	T2SO0	T2EDG	T2PS2	T2PS1	T2PS0
10h (r/w)	T2LA	8-bit real-time timer Latch							
Timer3: 8-bit Timer									
22h (r/w)	T3CON	T3EN	T3LOAD	T3SO1	T3SO0	T3EDG	T3PS2	T3PS1	T3PS0
24h (r/w)	T3LA	8-bit real-time timer Latch							
IRQ									
15h (r/w)	INTEN	GIE	ADCIE	PBIE	-	-	T3IE	T2IE	T1P1IE
16h (r/w)	INTFLAG	-	ADCIF	PBIF	-	-	T3IF	T2IF	T1P1IF
ADC Control									
17h (r/w)	ADCON1	ADCEN	-	-	-	CHSL3	CHSL2	CHSL1	CHSL0
18h (r/w)	ADCON2	-	-	-	-	-	-	CLKSL1	CLKSL0
19h (r/w)	ADCON3	-	-	-	-	ANISL3	ANISL2	ANISL1	ANISL0
1Ah (r)	ADDATL	D1	D0	-	-	-	-	-	-
1Bh (r)	ADDATH	D9	D8	D7	D6	D5	D4	D3	D2

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
Others									
1Dh(r/w)	APHCON	-	-	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0
1Eh(r/w)	BPHCON	PHB7	PHB6	PHB5	PHB4	-	PHB2	PHB1	PHB0
20h(r/w)	INTPB	PB7IEN	PB6IEN	PB5IEN	PB4IEN	PB3IEN	PB2IEN	PB1IEN	PB0IEN
21h (r/w)	WDTCON	-	I_WDT	I_TWDT	EXCLK	-	WDTPS2	WDTPS1	WDTPS0

Legend: - = unimplemented, read as '0'.

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

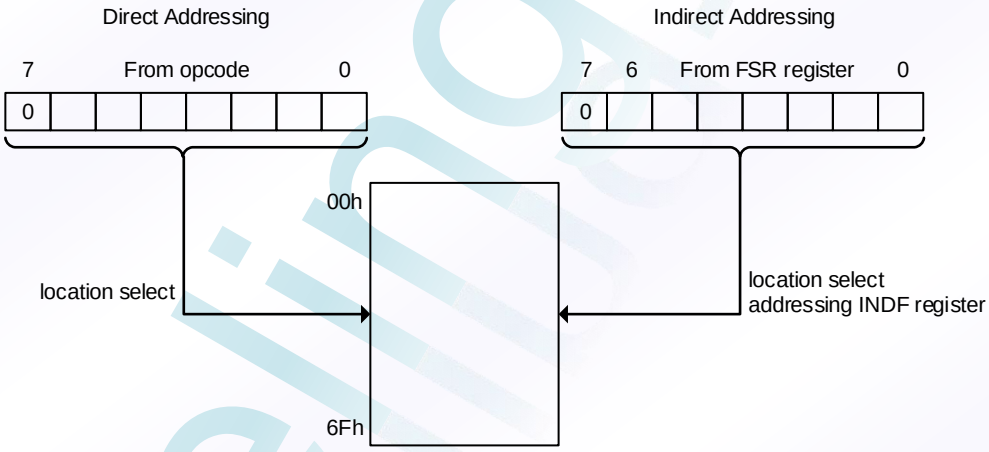
2.1.1 INDF (Indirect Addressing Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

Example 2.1: INDIRECT ADDRESSING
Register file 30 contains the value 10h
Register file 31 contains the value 0Ah
Load the value 30 into the FSR Register
A read of the INDF Register will return the value of 10h
Increment the value of the FSR Register by one (@FSR=31h)
A read of the INDF register now will return the value of 0Ah.

Figure 2.1: Direct/Indirect Addressing for FM8P73B



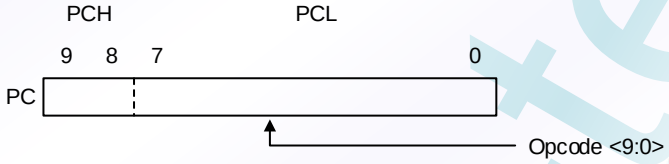
2.1.2 PCL (Low Bytes of Program Counter) & Stack

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
02h (r/w)	PCL	Low order 8 bits of PC							

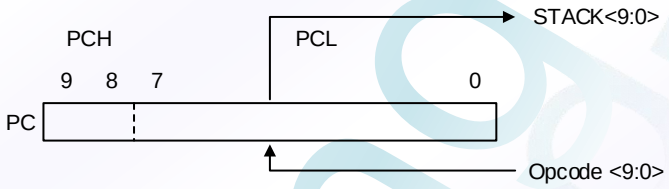
FM8P73B device have a 10-bits wide Program Counter (PC) and six-level deep 10-bit hardware push/pop stack. The low byte of PC is called the PCL register. This register is readable and writable.
As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

Figure 2.2: Loading of PC in Different Situations

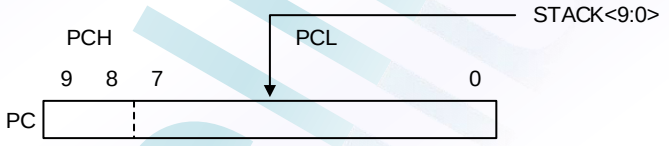
Situation 1: GOTO Instruction



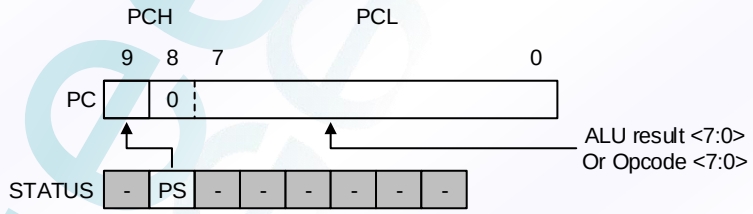
Situation 2: CALL Instruction



Situation 3: RETIA, RETFIE, or RETURN Instruction



Situation 4: Instruction with PCL as destination



Note: PC<9:8> cannot be accessed.

2.1.3 STATUS (Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	-	-	PS	$\overline{TO}$	$\overline{PD}$	Z	DC	C

Legend: - = unimplemented, read as '0'.

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C : Carry/borrow bit.
ADDAR
= 1, Carry occurred.
= 0, No Carry occurred.
SUBAR
= 1, No borrow occurred.
= 0, Borrow occurred.
Note : A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC : Half carry/half borrow bit
ADDAR
= 1, Carry from the 4th low order bit of the result occurred.
= 0, No Carry from the 4th low order bit of the result occurred.
SUBAR
= 1, No Borrow from the 4th low order bit of the result occurred.
= 0, Borrow from the 4th low order bit of the result occurred.

Z : Zero bit.
= 1, The result of a logic operation is zero.
= 0, The result of a logic operation is not zero.

$\overline{PD}$: Power down flag bit.
= 1, after power-up or by the CLRWDT instruction.
= 0, by the SLEEP instruction.

$\overline{TO}$: Watch-dog timer overflow flag bit.
= 1, after power-up or by the CLRWDT or SLEEP instruction
= 0, a watch-dog time overflow occurred

PS : ROM Page Select bit
= 1, 200h ~ 2FFh
= 0, 000h ~ 0FFh

2.1.4 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h (r/w)	FSR	0	Indirect data memory address pointer						

Bit6:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

Bit7 : Not used. Read as 0.

2.1.5 PORTA, PORTB, IOSTA and IOSTB (Port Data Registers and Port Direction Control Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (r/w)	IOSTA	-	-	IOSTA5	IOSTA4	IOSTA3	IOSTA2	IOSTA1	IOSTA0
06h (r/w)	PORTA	-	-	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
07h (r/w)	IOSTB	IOSTB7	IOSTB6	IOSTB5	IOSTB4	-	IOSTB2	IOSTB1	IOSTB0
08h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Legend: - = unimplemented, read as '0'.

The registers (IOSTA and IOSTB) are used to define the input or output of each port.

= 1, Input.

= 0, Output.

Reading the port (PORTA and PORTB register) reads the status of the pins independent of the pin's input/output modes. Writing to these ports will write to the port data latch. Please refer to 2.2 for detail I/O Port description.

Note: IOB3 is read only.

2.1.6 Timer1: 8-bit Timer & PWM1 Period

The Timer1 is an 8-bit down-count timer which include latch register. Please refer to 2.3 for detail Timer description.
The Timer1 can also be combined with Timer2 as PWM1 period and duty and controlled by the register PWM1CON. Please refer to 2.4 for detail PWM description.

2.1.6.1 T1CON (Timer1 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Bh (r/w)	T1CON	T1EN	T1LOAD	T1SO1	T1SO0	T1EDG	T1PS2	T1PS1	T1PS0

T1EN : TMR1 (PWM) Enable/Disable
= 1, TMR1 (PWM1) Enable.
= 0, TMR1 (PWM1) Disable.

T1LOAD : Enable/Disable Latch Buffer automatically load to counter register while writing to latch register
= 1, Enable TMR1 latch buffer automatically load to counter register while writing to latch register.
= 0, Disable TMR1 latch buffer automatically load to counter register while writing to latch register.
Note: This bit is only affected after latch register written. When the timer underflows, the latch register data will automatically load into counter register.

T1SO1:T1SO0 : TMR1 clock source selection

T1SO1	T1SO0	TMR1 clock source
0	0	TMCKI(IOB2)
0	1	Internal instruction clock cycle
1	0	Fosc
1	1	Fosc*2

T1EDG : TMR1 clock edge selection. This bit works only when external clock source TMCKI (IOB2) selected.
= 1, TMR1 increased on falling edge of TMCKI pin.
= 0, TMR1 increased on rising edge of TMCKI pin.

T1PS2:T1PS0 : TMR1 Prescaler selection

T1PS2	T1PS1	T1PS0	TMR1 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.6.2 PWM1CON (PWM1 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch (r/w)	PWM1CON	T12MOD	PWMS	POPS	-	PIR13	PIR12	PIR11	PIR10

Legend: - = unimplemented, read as '0'.

T12MOD : TMR1 operation mode select bit.
= 1, The TMR1 and TMR2 in PWM mode operation.
= 0, The TMR1 and TMR2 in Timer mode operation.

PWMS : Initial State of PWM1P output duty.
= 1, Set the initial state to L, change to H when TMR2 duty underflow.
= 0, Set the initial state to H, change to L when TMR2 duty underflow.

POPS : PWM Output Pin Select bit.
= 1, The PWM1P output from IOB1.
= 0, The PWM1P output from IOA0.

PIR13:PIR10 : Interrupt Event Rate of PWM1.
"1:N" means interrupt occurred after "N" PWM1 pulses.

PIR13 : PIR10				PWM1 Interrupt rate
0	0	0	0	1:1
0	0	0	1	1:2
0	0	1	0	1:3
0	0	1	1	1:4
		|		|
1	1	0	1	1:14
1	1	1	0	1:15
1	1	1	1	1:16

2.1.6.3 T1LA (Timer1 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Dh (r/w)	T1LA	8-bit real-time timer Latch							

T1LA is a Timer1 pre-set latch buffer, see 2.3 for detail description.

2.1.6.4 SYNPWM (Sync PWM Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
14h (r/w)	SYNPWM	SYNEN	PINV	DISN	-	-	-	DELS1	DELS0

Legend: - = unimplemented, read as '0'.

SYNEN : Sync PWM mode enable/disable.
In PWM mode:
= 1, Sync PWM mode Enable (PWM1N output on IOA1, PWM1P output on IOA0 or IOB1 select by POPS bit).
= 0, Sync PWM mode Disable, IOA1 is I/O.
In Timer mode:
Ignore

PINV : PWM_P invert bit.
In Sync PWM mode:
= 1, PWM1P is invert output.
= 0, PWM1P is normal output.
Note: This function is only available in pin IOA0.

else:
Ignore.

DISN : PWM1N enable/disable.
In Sync PWM mode:
= 1, IOA1 is normal I/O.
= 0, IOA1 is PWM1N output.

else:
Ignore

DELS1:DELS0 : Sync PWM Non overlap time (PWM1P & PWM1N) selection bits.

DELS1	DELS0	Non overlap time
0	0	1/2 cycle time
0	1	1 cycle time
1	0	3/2 cycle time
1	1	2 cycle time

2.1.7 Timer2: 8-bit Timer & PWM1 Duty

The Timer2 is an 8-bit down-count timer which include latch register. Please refer to 2.3 for detail Timer description.

2.1.7.1 T2CON (Timer2 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Fh (r/w)	T2CON	T2EN	T2LOAD	T2SO1	T2SO0	T2EDG	T2PS2	T2PS1	T2PS0

T2EN : TMR2 Enable/Disable
= 1, TMR2 (PWM1) Enable.
= 0, TMR2 (PWM1) Disable.
Note: At PWM mode, Timer2 is controlled by T1EN.

T2LOAD : Enable/Disable Latch Buffer automatically load to counter register while writing to latch register
= 1, Enable TMR2 latch buffer automatically load to counter register while writing to latch register.
= 0, Disable TMR2 latch buffer automatically load to counter register while writing to latch register.
Note: This bit is only affected after latch register written. When the timer underflows, the latch register data will automatically load into counter register.

T2SO1:T2SO0 : TMR2 clock source selection

T2SO1	T2SO0	TMR2 clock source
0	0	TMCKI(IOB2)
0	1	Internal instruction clock cycle
1	0	Fosc
1	1	Fosc*2

T2EDG : TMR2 clock edge selection. This bit works only when external clock source TMCKI (IOB2) selected.
= 0, TMR2 increased on rising edge of TMCKI pin.
= 1, TMR2 increased on falling edge of TMCKI pin.

T2PS2:T2PS0 : TMR2 Prescaler selection

T2PS2	T2PS1	T2PS0	TMR2 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.7.2 T2LA (Timer2 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
10h (r/w)	T2LA	8-bit real-time timer Latch							

T2LA is a Timer2 pre-set latch buffer, see 2.3 for detail description.

2.1.8 Timer3: 8-bit Timer

The Timer3 is an 8-bit down-count timer which include latch register. Please refer to 2.3 for detail Timer description.

2.1.8.1 T3CON (Timer3 Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
22h (r/w)	T3CON	T3EN	T3LOAD	T3SO1	T3SO0	T3EDG	T3PS2	T3PS1	T3PS0

T3EN : TMR3 Enable/Disable
= 1, TMR3 Enable.
= 0, TMR3 Disable.

T3LOAD : Enable/Disable Latch Buffer automatically load to counter register while writing to latch register
= 1, Enable TMR3 latch buffer automatically load to counter register while writing to latch register.
= 0, Disable TMR3 latch buffer automatically load to counter register while writing to latch register.
Note: This bit is only affected after latch register written. When the timer underflows, the latch register data will automatically load into counter register.

T3SO1:T3SO0 : TMR3clock source selection

T3SO1	T3SO0	TMR3clock source
0	0	TMCKI(IOB2)
0	1	Internal instruction clock cycle
1	0	Fosc
1	1	No function, don't use

T3EDG : TMR3 clock edge selection. This bit works only when external clock source TMCKI (IOB2) selected.
= 1, TMR3 increased on falling edge of TMCKI pin.
= 0, TMR3 increased on rising edge of TMCKI pin.

T3PS2:T3PS0 : TMR3 Prescaler selection

T3PS2	T3PS1	T3PS0	TMR3 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.1.8.2 T3LA (Timer3 Latch Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
24h (r/w)	T3LA	8-bit real-time timer Latch							

T3LA is a Timer3 pre-set latch buffer, see 2.3 for detail description.

2.1.9 INTEN (Interrupt Mask Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
15h (r/w)	INTEN	GIE	ADCIE	PBIE	-	-	T3IE	T2IE	T1P1IE

Legend: - = unimplemented, read as '0'.

GIE : Global interrupt enable bit.
= 1, Enable all un-masked interrupts.
= 0, Disable all interrupts.
Note : When an interrupt event occurred with the GIE bit and its corresponding interrupt enable bits are set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

ADCIE : ADC conversion completed interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

PBIE : PORTB interrupt enable
= 1, Enable interrupt.
= 0, Disable interrupt.

T3IE : Timer2 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

T2IE : Timer2 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

T1P1IE : Timer1 / PWM1 underflow interrupt enable bit.
= 1, Enable interrupt.
= 0, Disable interrupt.

2.1.10 INTFLAG (Interrupt Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
16h (r/w)	INTFLAG	-	ADCIF	PBIF	-	-	T3IF	T2IF	T1P1IF

Legend: - = unimplemented, read as '0'.

ADCIF : ADC Interrupt flag. Set when ADC conversion is completed, reset by software.

PBIF : Port B <7:0> Interrupt flag. Set when pin changed on selected I/O by register INTPB, and reset by software.

T3IF : TMR3 interrupt flag. Set when TMR3 underflows, and reset by software.

T2IF : TMR2 interrupt flag. Set when TMR2 underflows, and reset by software.

T1P1IF : TMR1 interrupt or PWM1 interrupt flag. Set when TMR1 underflows or PWM1 pulse counts to selected interrupt rate, and reset by software.

2.1.11 ADCON1 (AD converter Control Register1)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
17h (r/w)	ADCON1	ADCEN	-	-	-	CHSL3	CHSL2	CHSL1	CHSL0

Legend: - = unimplemented, read as '0'.

ADCEN : ADC enable/disable setting
= 0, Disable.
= 1, Enable.
Note : This bit should be set by software and would be reset by hardware after the ADC end of conversion.

CHSL3:CHSL0 : ADC input channel select

CHSL3	CHSL2	CHSL1	CHSL0	Input channel
0	0	0	0	Channel 0, IOA0 pin
0	0	0	1	Channel 1, IOA1 pin
0	0	1	0	Channel 2, IOA2 pin
0	0	1	1	Channel 3, IOA3 pin
0	1	0	0	Channel 4, IOA4 pin
0	1	0	1	Channel 5, IOA5 pin
0	1	1	0	Channel 6, IOB0 pin
0	1	1	1	Channel 7, IOB1 pin
1	0	0	0	Channel 8, IOB2 pin
1	0	0	1	Channel 9, IOB6 pin
1	0	1	0	Channel 10, IOB7 pin

2.1.12 ADCON2 (AD converter Control Register2)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
18h (r/w)	ADCON2	-	-	-	-	-	-	CLKSL1	CLKSL0

Legend: - = unimplemented, read as '0'.

CLKSL1:CLKSL0 : ADC Conversion clock source select bits.

CKSL1	CKSL0	Conversion clock
0	0	System clock /2 (fastest result, lowest quality)
0	1	System clock /8
1	0	System clock /32
1	1	System clock /128 (slowest result, best quality)

Note : The conversion clocks decide the conversion rate and precision. If fast conversion clock is selected, that will drop-off the precision. If want to get more accurate A/D data, use slow speed is recommended.

2.1.13 ADCON3 (AD converter Control Register3)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
19h (r/w)	ADCON3	-	-	-	-	ANISL3	ANISL2	ANISL1	ANISL0

Legend: - = unimplemented, read as '0'.

ANISL3:ANISL0 : Analog input select bits.

ANISL3	ANISL2	ANISL1	ANISL0	Analog input selection
0	0	0	0	All the ports are digital input
0	0	0	1	AN0
0	0	1	0	AN1
0	0	1	1	AN2
0	1	0	0	AN3
0	1	0	1	AN4
0	1	1	0	AN5
0	1	1	1	AN6
1	0	0	0	AN7
1	0	0	1	AN8
1	0	1	0	AN9
1	0	1	1	AN10

Note : To minimize power consumption, all the I/O pins should be carefully managed before entering sleep mode.

2.1.14 ADDATL, ADDATH (AD conversion data high and low)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Ah (r)	ADDATL	D1	D0	-	-	-	-	-	-
1Bh (r)	ADDATH	D9	D8	D7	D6	D5	D4	D3	D2

Legend: - = unimplemented, read as '0'.

The ADDATL and ADDATH registers is ADC conversion result. When ADC conversion is completed, the result is loaded into ADDATL and ADDATH, the ADCEN bit will be cleared, and the ADCIF bit will be set (if ADCIE are set).

2.1.15 APHCON, BPHCON (Port A and Port B Pull-high Control)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
1Dh(r/w)	APHCON	-	-	PHA5	PHA4	PHA3	PHA2	PHA1	PHA0
1Eh(r/w)	BPHCON	PHB7	PHB6	PHB5	PHB4	-	PHB2	PHB1	PHB0

Legend: - = unimplemented, read as '0'.

Those registers are used to setup pull-high resistor enable/disable of each IO pins.

= 1, Pull-high resistor enable.

= 0, Pull-high resistor disable.

2.1.16 INTPB (Port B Interrupt / Wakeup control)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
20h(r/w)	INTPB	PB7IEN	PB6IEN	PB5IEN	PB4IEN	PB3IEN	PB2IEN	PB1IEN	PB0IEN

This register is used to enable/disable the interrupt/wakeup function of Port B. Please refer to 2.7.1 for detail description of External Interrupt and Wake up function.

= 1, Selected IO interrupt/wakeup enable.

= 0, Selected IO interrupt/wakeup disable.

2.1.17 WDTCON (Watchdog Timer Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
21h (r/w)	WDTCON	-	I_WDT	I_TWDT	EXCLK	-	WDTPS2	WDTPS1	WDTPS0

Legend: - = unimplemented, read as '0'.

The FM8P73B builds in a watchdog timer with two different modes, normal watchdog reset and internal watchdog wakeup. The watchdog timer is controlled by this register (WDTCON). Please refer to 2.5 for detail Watchdog Timer description.

I_WDT : Internal Watchdog Wakeup mode selection.
= 1, Internal Watchdog Wakeup Enable.
= 0, Internal Watchdog Wakeup Disable.

I_TWDT : Watchdog Timer Stable time required when operating in I_WDT mode.
= 1, 1.25ms.
= 0, 2.5ms (default).

EXCLK : IOB2/TMCKI function selection
= 1, IOB2 is external clock input of timer.
= 0, IOB2 is normal I/O.

WDTPS2:WDTPS0 : Watchdog timer prescaler setting

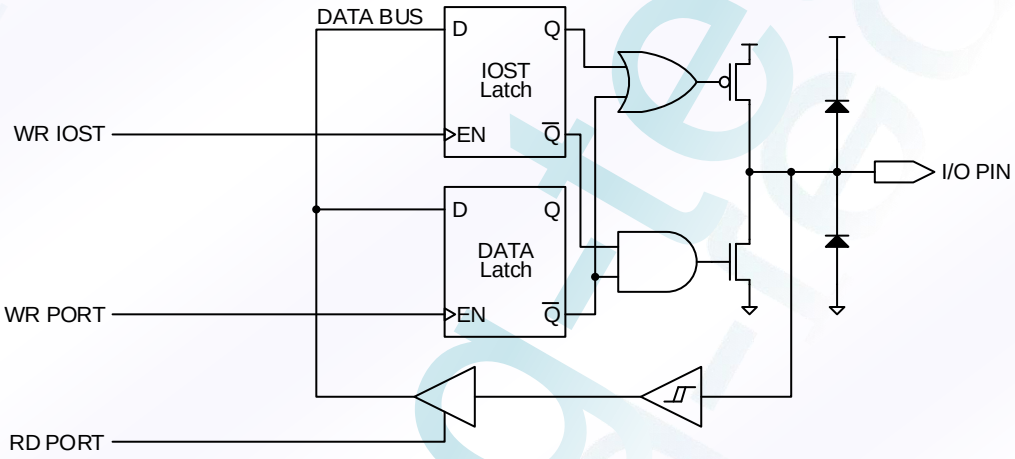
WDTPS2 : WDTPS0			WDT prescaler rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.2 I/O Ports

There are totally 13 bi-directional tri-state I/O ports and one (IOB3) input only. All I/O pins (IOA<5:0>, IOB<7:0>) have specified data direction control registers (IOSTA, IOSTB) which can configure these pins as output or input. All the IO pins can also enable or disable a weak internal pull-high by setting APHCON and BPHCON. This weak pull-high will be automatically turned off when the pin is configured as an output pin.
VR pin is reference voltage input pin of the ADC module, this pin does not have I/O function. **The voltage on this pin must not exceed VDD, otherwise it will cause the pin burned down.**

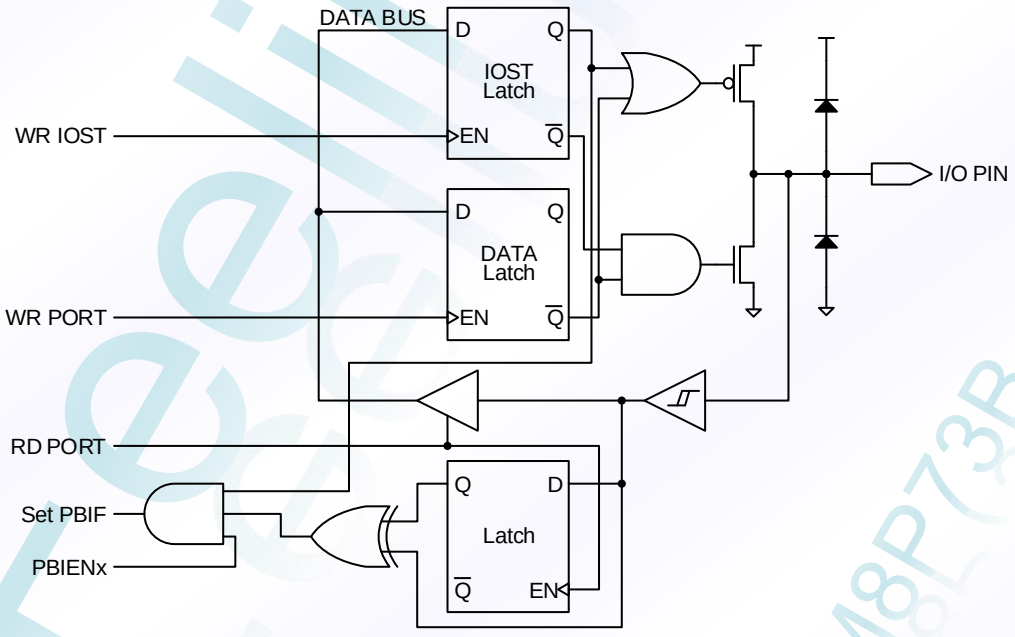
Figure 2.3: Block Diagram of I/O Pins

IOA5 ~ IOA0:



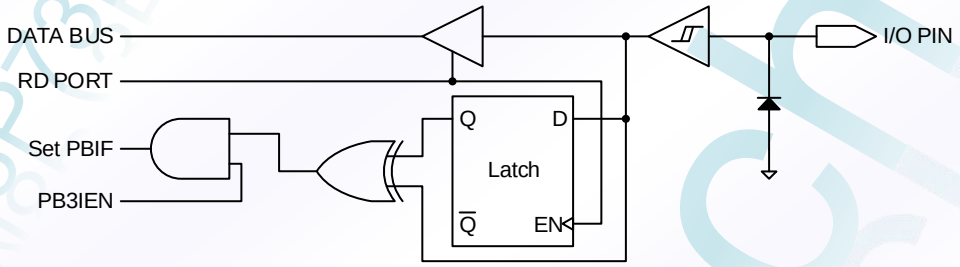
Pull-high/ADC control is not shown in this figure

IOB7 ~ IOB4, IOB2 ~ IOB0:



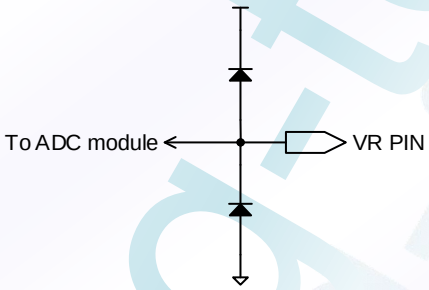
Pull-high/ADC/OSC control is not shown in this figure

IOB3:



Voltage on this pin must not exceed VDD.

VR:

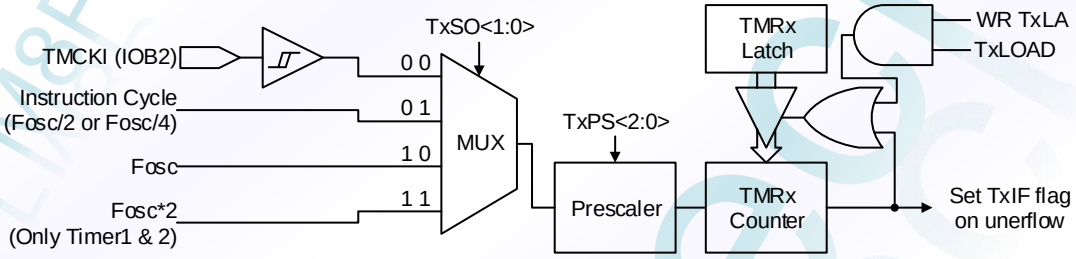


Voltage on this pin must not exceed VDD.

2.3 Timer/Event Counter (TMR1, TMR2, TMR3)

The FM8P73B contains three 8-bit down-count Timers. All these timers have auto reload function, TMR1/TMR2 can be combined to perform PWM function

Figure 2.4: Block Diagram of the Timer



2.3.1 Clock Source

There are 4 clock sources could be selected by each timer separately.

2.3.1.1 TMCKI (IOB2)

The event counter mode would be activated when the source of TMCKI (IOB2) used. At this mode, the rising/ falling edge of the event could also be selected separately.

2.3.1.2 Instruction cycle

In this mode, the timer will down-count on every instruction cycle (if prescaler is 1:1).

2.3.1.3 Fosc

In this mode, timer clock source defined by the Fosc bit in the configuration word.

2.3.1.4 Fosc *2

In this mode, the oscillator frequency is multiplied by 2, as the timer clock source. Oscillator modes defined by the Fosc bit in the configuration word.

Note : 1. In this mode, the frequency multiplier minimum operating voltage limits, please refer to electrical characteristics table VPWM item.
2. This mode only for Timer1 and Timer2.

2.3.2 Prescaler

Each timer contains a 3-bits prescaler which can scale the timer or counter from 1:1 to 1:128.

T1PS2 : T1PS0			TMR1 Prescal rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

2.4 Pulse Width Modulation (PWM)

FM8P73B provides one PWM output shared with TMR1/2, TMR1 becomes the period of PWM1 and TMR2 will be the duty of PWM1.
If the system frequency is 4MHz, the range of PWM period could be from 0.5us to 8,192ms.

2.4.1 Normal PWM mode

In this mode, it is a general purpose PWM mode. Please refer to the sample program and timing diagram below.

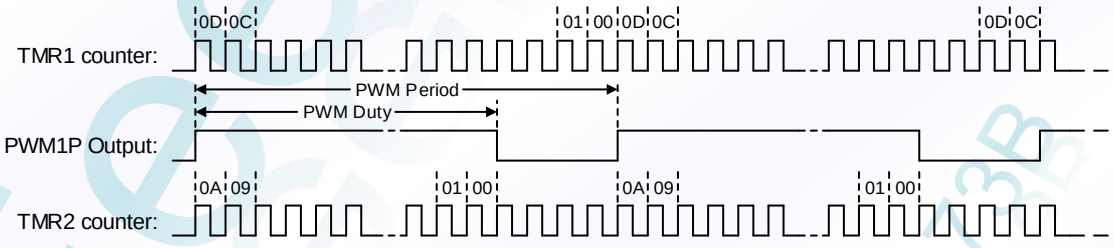
Note : When PWM duty or period needed to be changed, the auto-load control bit of the timer (TxLOAD) must be cleared before new data writes to latch register. If this bit still set, the data written to latch register would be load into counter register immediately and cause PWM output anomaly.

Example 2.2: PWM1 Setting (Normal mode)

Address	Code		
NA	#include <8P73B.ASH>		
	…		
	//Set PWM1 Period		
n	MOVIA	0x61	
n+1	MOVAR	T1CON	;Set source: 4MHz IRC (250nS) Prescaler 1:2
n+2	MOVIA	0x80	
n+3	MOVAR	PWM1CON	;Set PWM interrupt rate 1:1, output on IOA0
n+4	MOVIA	0x0F	
n+5	MOVAR	T1LA	;Set period (0x0F down count to 0x00)
			;Period time = 250ns x 16 x 2 = 8uS
	//Set PWM1 Duty		
n+6	MOVIA	0x61	
n+7	MOVAR	T2CON	;Set source 4MHz IRC (250nS) Prescaler 1:2
n+8	MOVIA	0x07	
n+9	MOVAR	T2LA	;Set Duty (0x07 down count to 0x00)
			;Duty time = 250ns x 8 x2 = 4uS
n+10	BSR	T1CON,T1EN_B	;Start PWM1
n+11	MOVIA	0x81	
n+12	MOVAR	INTEN	;Enable global & PWM1 interrupt
n+13	CLRR	INTFLAG	;Clear interrupt flag

Note: The PWM duty (Timer2) must be smaller than PWM period (Timer1).

Figure 2.5: Normal PWM Output Waveform



2.4.2 Sync PWM mode

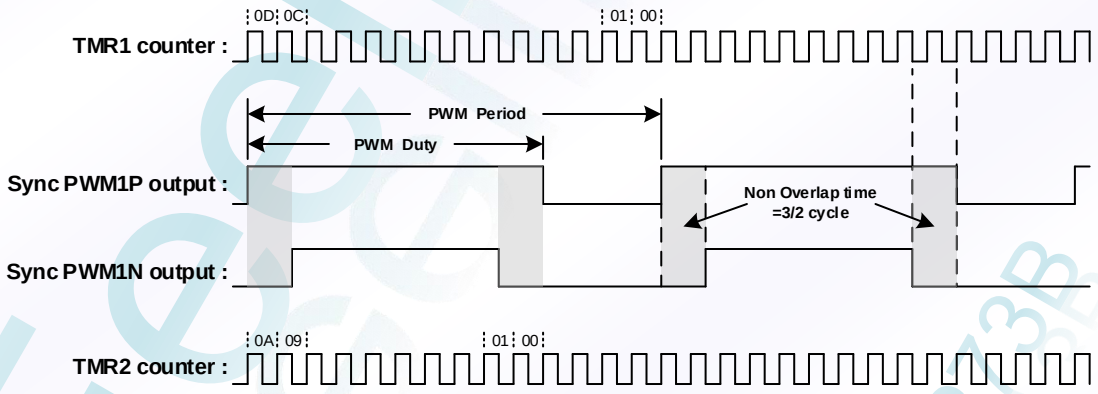
In Sync PWM mode, the PWM has two outputs. PWM1N Non overlap time can be adjusted from SYNPWM<1:0>, please refer to the sample program and the timing diagram below.

Example 2.3: PWM1 Setting (Sync mode)

Address	Code			
NA	#include	<8P73B.ASH>		
		…		
		//Set PWM1 Period		
n		MOVIA	0x61	
n+1		MOVAR	T1CON	;Set source: 4MHz IRC (250nS) Prescaler 1:2
n+2		MOVIA	0x80	
n+3		MOVAR	PWM1CON	;Set PWM interrupt rate 1:1, output on IOA0
n+4		MOVIA	0x0F	
n+5		MOVAR	T1LA	;Set period (0x0F down count to 0x00)
				;Period time = 250ns x 16 x 2 = 8uS
		//Set PWM1 Duty		
n+6		MOVIA	0x61	
n+7		MOVAR	T2CON	;Set source 4MHz IRC (250nS) Prescaler 1:2
n+8		MOVIA	0x07	
n+9		MOVAR	T2LA	;Set Duty (0x07 down count to 0x00)
				;Duty time = 250ns x 8 x2 = 4uS
		//Set Sync PWM		
n+10		MOVIA	0x82	
n+11		MOVAR	SYNPWM	;Set PWM1P is normal, IOA1 is PWM1N output
				;Non overlap time = 3/2 cycle time
n+12		BSR	T1CON,T1EN_B	;Start PWM1
n+13		MOVIA	0x81	
n+14		MOVAR	INTEN	;Enable global & PWM1 interrupt
n+15		CLRR	INTFLAG	;Clear interrupt flag

Note: The PWM duty (Timer2) must be smaller than PWM period (Timer1).

Figure 2.6: Sync PWM Waveform



2.5 Watch Dog Timer (WDT)

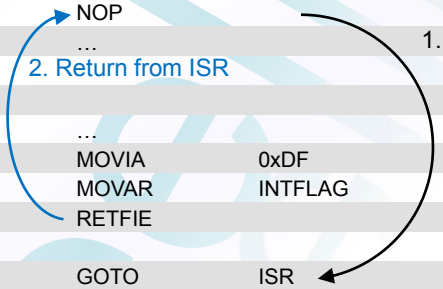
The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode.

The WDT has a typical time-out period of 20 ms (without prescaler). This period of this timer may be variant slightly because of temperature, voltage, and process variation. If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the WDTCON register <2:0>. Thus, the longest time-out period is approximately 2.56 seconds.
The CLRWDT instruction clears the WDT and prevents it from timing out and generating a device reset.
The SLEEP instruction also resets the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

There are two type of watchdog timer mode could be selected by I_WDT (WDTCON <6>). When I_WDT bit disable, normal watchdog timer reset is selected. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the $\overline{TO}$ bit (STATUS<4>) will be cleared.
If I_WDT bit enabled, the internal watchdog timer wakeup will be used. The system wakeups from sleep, then jumps into interrupt vector with external interrupt request PBIF (INTFLAG<5>) and continues from next instruction instead of triggering a reset event. There is a stabilization time required for internal watchdog wakeup could be selected by I_ TWDT (WDTCON<5>). The default value of this stabilization timer is 2.5ms.

Example 2.4: Internal Watchdog Wakeup

Address	Code			
NA	#include	<8P73B.ASH>		
		…		
n		MOVIA	0xA0	
n+1		MOVAR	INTEN	;Enable global & Port B interrupt
n+2		CLRWDT		
n+3		MOVIA	0x67	
n+4		MOVAR	WDTCON	;Sleep: 2.56S + Wakeup:1.25mS
n+5		…		
n+6		…		
n+7		SLEEP		
n+8		NOP		
		…		
N/A	ISR:			;In this example, ISR define at 0x200
200		…		;User WDT Wakeup ISR code
200+n		MOVIA	0xDF	
200+n+1		MOVAR	INTFLAG	;Clear PBIF flag(Note1)
200+n+2		RETFIE		
0x3FE		GOTO	ISR	
0x3FF		GOTO	START	



Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt save status code is not shown in this example.

Example 2.5: Typical Watchdog Reset

```
Address  Code
NA       #include    <8P73B.ASH>
                …
n        CLRWDT
n+1      MOVIA       0x07
n+2      MOVAR       WDTCON          ;Sleep: 2.56S + Wakeup:20mS
n+3      …
n+4      …
n+5      SLEEP
n+6      NOP
                …                          WDT Reset
                …
0x3FF    GOTO        START
```

2.6 Reset

FM8P73B device may be RESET in one of the following ways:

1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset, RSTB or WDT Reset.

A Power-on RESET pulse is generated on-chip when Vdd rise is detected. To use this feature, the user merely ties the RSTB pin to Vdd.

On-chip Low Voltage Detector (LVDT) places the device into reset when Vdd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation Vdd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.

A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

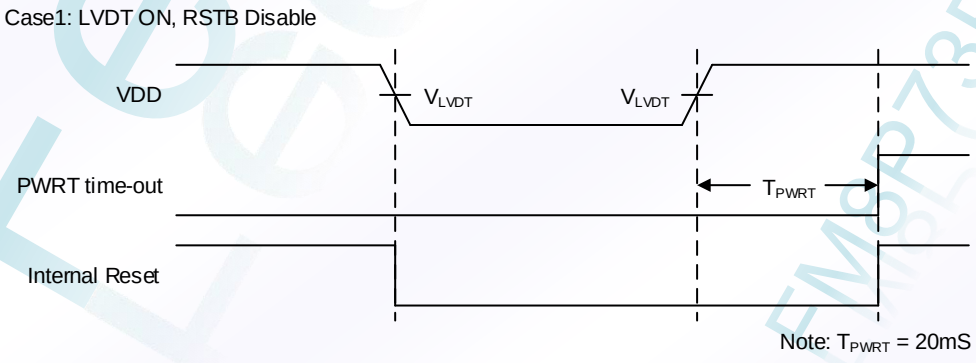
The $\overline{TO}$ and $\overline{PD}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.6.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 20ms delay after Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active.

The PWDT delay will vary from device to device due to Vdd, temperature, and process variation.

Figure 2.7: Reset Timing



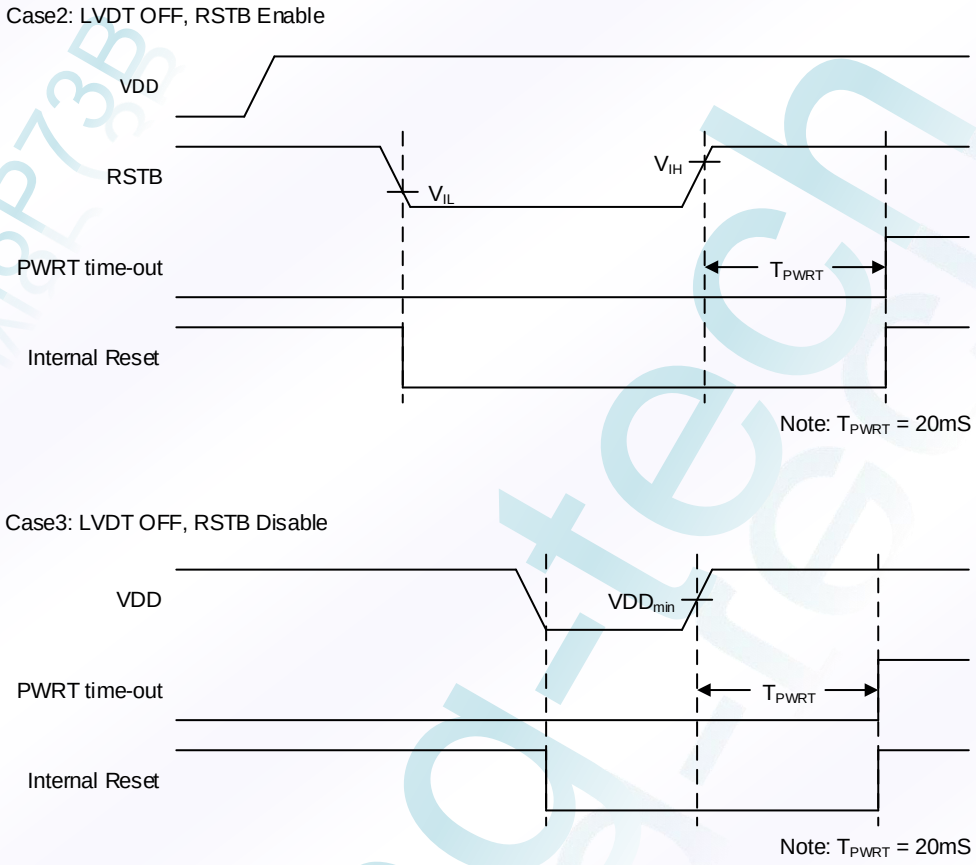


Figure 2.8: Simplified Block Diagram of on-chip Reset Circuit

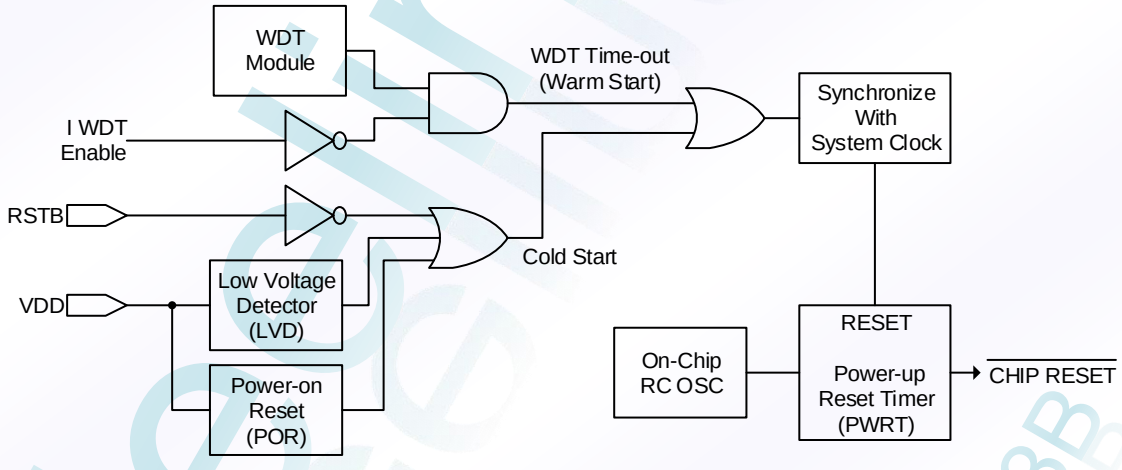


Table 2.1: Reset Conditions for Operational Registers

Register	Address	Power-on Reset Brown-out Reset	WDT Reset RSTB Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
INDF	00h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #xxx
FSR	04h	0xxx xxxx	0uuu uuuu
IOSTA	05h	0011 1111	0011 1111
PORTA	06h	00xx xxxx	00uu uuuu
IOSTB	07h	1111 0111	1111 0111
PORTB	08h	xxxx xxxx	uuuu uuuu
T1CON	0Bh	0000 0000	0000 0000
PWM1CON	0Ch	0000 0000	0000 0000
T1LA	0Dh	1111 1111	1111 1111
T2CON	0Fh	0000 0000	0000 0000
T2LA	10h	1111 1111	1111 1111
SYNPWM	14h	0000 0000	0000 0000
INTEN	15h	0000 0000	0000 0000
INTFLAG	16h	0000 0000	0000 0000
ADCON1	17h	0000 0000	0000 0000
ADCON2	18h	0000 0000	0000 0000
ADCON3	19h	0000 0000	0000 0000
ADDATL	1Ah	0000 0000	0000 0000
ADDATH	1Bh	0000 0000	0000 0000
APHCON	1Dh	0000 0000	0000 0000
BPHCON	1Eh	0000 0000	0000 0000
INTPB	20h	0000 0000	0000 0000
WDTCON	21h	0000 0111	0000 0111
T3CON	22h	0000 0000	0000 0000
T3LA	24h	1111 1111	1111 1111
General Purpose Registers	30 ~ 6Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented,
= refer to the following table for possible values.

Table 2.2: $\overline{TO}$ / $\overline{PD}$Status after Reset or Wake-up

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-on Reset / Brown-out reset
u	u	RSTB Reset during normal operation
1	0	RSTB Reset during SLEEP
0	1	WDT timer overflow from normal mode
0	0	WDT timer overflow from sleep mode

2.7 Interrupt

The FM8P73B has three kinds of interrupt sources:
1. 8 External IOB<0:7> pin changed interrupt
2. 3 Timers underflow interrupt (or PWM interrupt)
3. ADC conversion completion interrupt

INTFLAG is the interrupt flag register that recodes the interrupt requests to the relative flags.
A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/ disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 3FEh. The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.
The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.
The flag bit in INTFLAG register is set by interrupt event regardless of the status of its mask bit.

2.7.1 PORTB<0:7> External Interrupt and Wakeup Function

The external interrupt on PORTB<0:7> are selected by INTPB<0:7> and PBIE (INTEN<5>). When the device is in normal mode and the specified IO status changed, the interrupt event will be triggered and the program will jump to 3FEh.
When the device is in sleep mode, those interrupts can also be used as an external wakeup signal. The device will restart system clock and the program will jump to 3FEh after startup timer timeout.

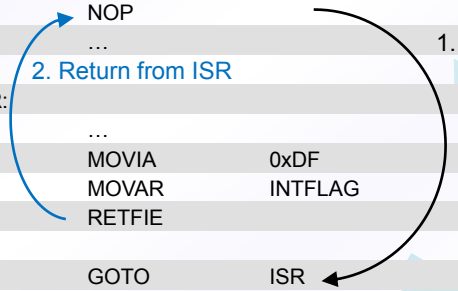
Example 2.6: External IOB0 pin change interrupt

Address	Code			
NA	#include	<8P73B.ASH>		
		…		
n		MOVIA	0xFF	
n+1		MOVAR	IOSTB	;Set Port B as input
n+2		MOVIA	0xA0	
n+3		MOVAR	INTEN	;Enable global & Port B interrupt
n+4		MOVIA	0xDF	
n+5		MOVAR	INTFALG	;Clear PBIF flag(Note1)
n+6		MOVR	PORTB,R	;Update Port B pin status
n+7		MOVIA	0x01	
n+8		MOVAR	INTPB	;Set IOB0 pin change
		…		
		…		
		…		1. IOB0 pin change
				2. Return from ISR
N/A	ISR:			;In this example, ISR define at 0x200
200		…		;User Port B pin change ISR code
200+n		MOVIA	0xDF	
200+n+1		MOVAR	INTFLAG	;Clear PBIF flag(Note1)
200+n+2		RETFIE		
3FE		GOTO	ISR	
3FF		GOTO	START	

Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt save status code is not shown in this example.

Example 2.7: External IOB0 pin change wakeup interrupt

Address	Code			
NA	#include	<8P73B.ASH>		
		…		
n		MOVIA	0xFF	
n+1		MOVAR	IOSTB	;Set Port B as input
n+2		MOVIA	0xA0	
n+3		MOVAR	INTEN	;Enable global & Port B interrupt
n+4		MOVIA	0xDF	
n+5		MOVAR	INTFALG	;Clear PBIF flag(Note1)
n+6		MOVR	PORTB,R	;Update Port B pin status
n+7		MOVIA	0x01	
n+8		MOVAR	INTPB	;Set IOB0 pin change wakeup
n+9		SLEEP		
n+10		NOP		
		…		
N/A	ISR:			;In this example, ISR define at 0x200
200		…		;User Port B pin change wakeup ISR code
200+n		MOVIA	0xDF	
200+n+1		MOVAR	INTFLAG	;Clear PBIF flag(Note1)
200+n+2		RETFIE		
3FE		GOTO	ISR	
3FF		GOTO	START	



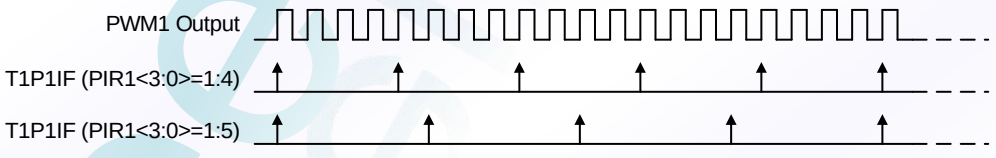
Note : 1. BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).
2. Interrupt save status code is not shown in this example.

2.7.2 Timer1~3 Interrupt Function

2.7.2.1 Timer1 (PWM1) interrupt

At Timer mode, an underflow (00h → FFh) in the TMR1 counter will set the flag bit T1P1IF (INTFLAG<0>). This interrupt can be disabled by clearing T1P1IE bit (INTEN<0>).
At PWM mode, the end of each PWM period cycle to generate an interrupt. The interrupt rate can be adjusted by PIR13:10 (PWM1CON <3:0>).

Figure 2.9: PWM Interrupt Waveform (Normal PWM or Sync PWM mode)



2.7.2.2 Timer2 interrupt

At Timer mode, an underflow (00h → FFh) in the TMR2 counter will set the flag bit T2IF (INTFLAG<1>). This interrupt can be disabled by clearing T2IE bit (INTEN<1>).
At PWM mode, TMR2 is PWM1 duty cycle counter. Not generate an interrupt.

2.7.2.3 Timer3 interrupt

An underflow (00h → FFh) in the TMR3 counter will set the flag bit T3IF (INTFLAG<2>). This interrupt can be disabled by clearing T3IE bit (INTEN<2>).

2.7.3 ADC conversion completion interrupt

When the A/D conversion is completed, the flag bit ADCIF (INTFLAG <6>) will be set. And the ADCIF bit can be cleared by software.
This interrupt can be disabled by clearing ADCIE bit (INTEN<6>).

2.8 Analog to Digital Converter (ADC)

This analog to digital converter has 11 channels 10bits (8+2) resolution. The ADC is controlled by three control register, ADCON1, ADCON2, and ADCON3.

Example 2.8: Analog to Digital Conversion (Channel0 AD conversion)

Address	Code			
NA	#include	<8P73B.ASH>		
		…		
n		BTRSC	ADCON1,ADCEN_B	
n+1		GOTO	$-1	;Make Sure no ADC is processing
n+2		MOVIA	0xBF	
n+3		MOVAR	INTFLAG	;Clear ADCIF flag(Note)
n+4		MOVIA	0x00	
n+5		MOVAR	ADCON1	;Select ADC Channel 0 (IOA0) conversion
n+6		MOVIA	0x03	
n+7		MOVAR	ADCON2	;Set AD conversion rate: System clock / 128
n+8		MOVIA	0x01	
n+9		MOVAR	ADCON3	;Set AN0 analog input
n+10		BSR	ADCON1,ADCEN_B	;ADC conversion start
n+11		BTRSS	INTFLAG,ADCIF_B	
n+12		GOTO	$-1	;Wait AD end of conversion
n+13		MOVR	ADDATH,A	;Read ADC high byte data
n+14		MOVAR	…	
n+15		MOVR	ADDATL,A	;Read ADC low byte data
n+16		MOVAR	…	
		…		

Note : BCR instruction is not recommended for Clear interrupt flag (INTFLAG register).

2.9 Oscillator Configurations

FM8P73B can be operated in five different combinations of oscillator modes. Users can program configuration word (F_{OSC}) to select the appropriate modes. The five different system clock modes are combination of the following oscillators:

- LF: Low Frequency Crystal Oscillator
- XT: Crystal/Resonator Oscillator
- HF: High Frequency Crystal/Resonator Oscillator
- ERC: External Resistor/ Voltage Controlled Oscillator
- IRC: Internal Resistor/Capacitor Oscillator

In LF, XT, or HF modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, XT, or HF modes, the devices can have an external clock source drive the OSCI pin.
The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext), the operating temperature, and the process parameter.
The IRC option offers largest cost savings for timing insensitive applications.

Figure 2.10: HF, XT or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

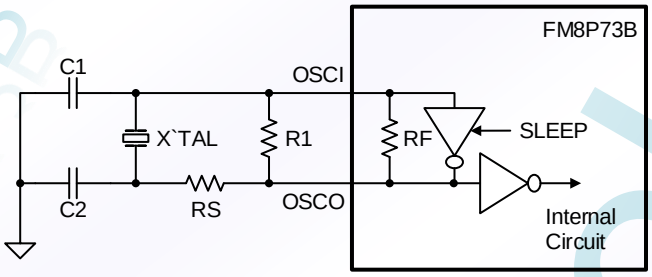


Figure 2.11: HF, XT or LF Oscillator Modes (External Clock Input Operation)

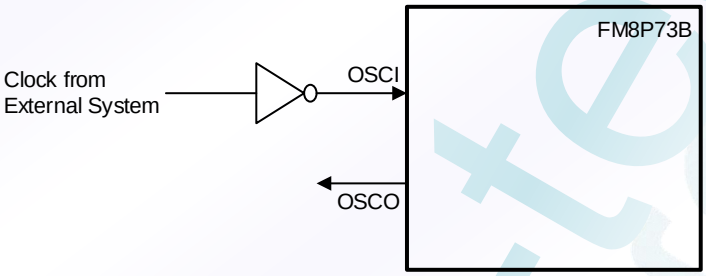
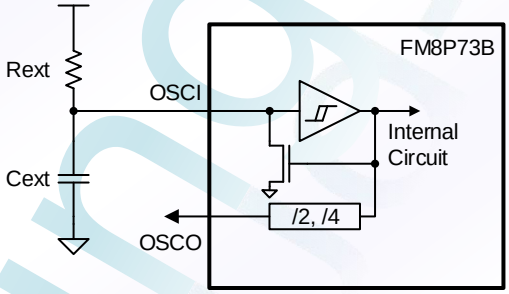


Figure 2.12: ERC (External Resistor Controlled) Oscillator Mode

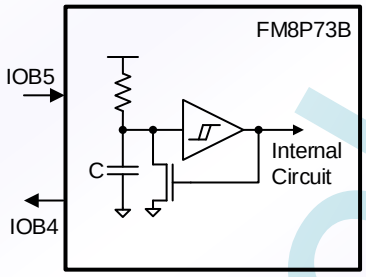


The typical oscillator frequency vs. external resistor is as following table
When Cext = 0.01uf (103)

5V		3V	
Rext	Frequency	Rext	Frequency
4.3M	32 KHz	3.6M	32 KHz
210K	500 KHz	238K	500 KHz
108K	1.0 MHz	116K	1.0 MHz
56K	2.0 MHz	59K	2.0 MHz
30K	4.0 MHz	30K	4.0 MHz
16K	8.0 MHz	16K	8.0 MHz
11K	12.0 MHz	11K	12.0 MHz

Note: Values are provided for design reference only.

Figure 2.13: IRC Oscillator Mode (Internal R, Internal C Oscillator)



2.10 Configuration Words

Table 2.3: Configuration Words

Name	Description
Fosc	Oscillator Selection Bit → IRC(4MHz) mode (default) → ERC mode → HF crystal mode → XT crystal mode → LF crystal mode Note: See Table 2.4 for detail description.
WDTEN	Watchdog Timer Enable Bit → WDT enabled (default) → WDT disabled
LVDT	Low Voltage Detector Selection Bit → LVDT Disable (default) → LVDT = 2.0V → LVDT = 2.3V → LVDT = 3.5V
RSTBIN	IOB3/RSTB Pin Selection Bit → RSTB pin is selected (default) → IOB3 pin is selected
PWRT	Power On Reset time Selection Bit → 20ms is selected (default) → 5ms is selected
OSCD	Instruction Period Selection Bit → four oscillator periods (4T) (default) → two oscillator periods (2T)
OSCOUT	IOB4/OSCO Pin Selection Bit → OSCO pin is selected (default) → IOB4 pin is selected
PROTECT	Code Protection Bit → NO, EPROM code protection off (default) → YES, EPROM code protection on

Table 2.4: Selection of IOB5/OSCI and IOB4/OSCO Pin

Mode of oscillation	IOB5/OSCI	IOB4/OSCO
IRC	Force to IOB5	Force to IOB4
ERC	Force to OSCI	IOB4/OSCO selected by OSCOUT bit
HF, XT, LF	Force to OSCI	Force to OSCO

3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2(1)	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2(1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	00h → ACC	1	Z
CLRR	**R**	Clear R	00h → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2(1)	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2(1)	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$ → dest	1	Z
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC<10:0>	2	-

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
GOTO	**I**	Unconditional branch	I → PC<10:0>	2	-

Note: 1. 2 cycles for skip, else 1 cycle.
2. bit : Bit address within an 8-bit register R
R : Register address (00h to 6Fh)
I : Immediate data
ACC : Accumulator
d : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest : Destination
PC : Program Counter
WDT : Watchdog Timer Counter
GIE : Global interrupt enable bit
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

ADDAR	**Add ACC and R**
Syntax:	ADDAR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	ACC + R → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDAR	**AND ACC and R**
Syntax:	ANDAR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	ACC and R → dest
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDIA	**AND Immediate with ACC**
Syntax:	ANDIA I
Operands:	0 ≤ I ≤ 0xFF
Operation:	ACC AND I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

BCR	**Clear Bit in R**
Syntax:	BCR R, b
Operands:	0 ≤ R ≤ 0x6F 0 ≤ b ≤ 7
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit 'b' in register 'R'.
Cycles:	1

BSR	**Set Bit in R**
Syntax:	BSR R, b
Operands:	0 ≤ R ≤ 0x6F 0 ≤ b ≤ 7
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit 'b' in register 'R'.
Cycles:	1

BTRSC	**Test Bit in R, Skip if Clear**
Syntax:	BTRSC R, b
Operands:	0 ≤ R ≤ 0x6F 0 ≤ b ≤ 7
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit 'b' in register 'R' is 0 then the next instruction is skipped. If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	**Test Bit in R, Skip if Set**
Syntax:	BTRSS R, b
Operands:	0 ≤ R ≤ 0x6F 0 ≤ b ≤ 7
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit 'b' in register 'R' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	**Subroutine Call**
Syntax:	CALL I
Operands:	0 ≤ I ≤ 0x3FF
Operation:	PC + 1 → Top of Stack, I → PC<9:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 10-bit immediate address is loaded into PC bits <9:0>.
Cycles:	2

CLRA	**Clear ACC**
Syntax:	CLRA
Operands:	None
Operation:	00h → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	**Clear R**
Syntax:	CLRR R
Operands:	0 ≤ R ≤ 0x6F
Operation:	00h → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	Clear Watchdog Timer
Syntax:	CLRWDT
Operands:	None
Operation:	00h → WDT; 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$,$\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. The status bits$\overline{TO}$ and $\overline{PD}$ will be set.
Cycles:	1

COMR	Complement R
Syntax:	COMR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	$\overline{R}$ → dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECR	Decrement R
Syntax:	DECR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement of register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	Decrement R, Skip if 0
Syntax:	DECRSZ R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decrement. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a two-cycle instruction.
Cycles:	1/2

GOTO	Unconditional Branch
Syntax:	GOTO I
Operands:	0 ≤ I ≤ 0x3FF
Operation:	I → PC<9:0>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 10-bit immediate value is loaded into PC bits <9:0>.
Cycles:	2

INCR	**Increment R**
Syntax:	INCR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

INCRSZ	**Increment R, Skip if 0**
Syntax:	INCRSZ R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register 'R' are increment. If 'd' is 0 the result is placed in the ACC register. If 'd' is the result is stored back in register 'R'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead and making it a two-cycle instruction.
Cycles:	1/2

IORAR	**OR ACC with R**
Syntax:	IORAR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register 'R'. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

IORIA	**OR Immediate with ACC**
Syntax:	IORIA I
Operands:	0 ≤ I ≤ 0xFF
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

MOVAR	**Move ACC to R**
Syntax:	MOVAR R
Operands:	0 ≤ R ≤ 0x6F
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register 'R'.
Cycles:	1

MOVIA	**Move Immediate to ACC**
Syntax:	MOVIA I
Operands:	0 ≤ I ≤ 0xFF
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate 'I' is loaded into the ACC register. The don't cares will assemble as 0s.
Cycles:	1

MOVR	**Move R**
Syntax:	MOVR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

NOP	**No Operation**
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

RETFIE	**Return from Interrupt, Set 'GIE' Bit**
Syntax:	RETFIE
Operands:	None
Operation:	Top of Stack → PC 1 → GIE
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). The 'GIE' bit is set to 1. This is a two-cycle instruction.
Cycles:	2

RETIA	**Return with Immediate in ACC**
Syntax:	RETIA I
Operands:	0 ≤ I ≤ 0xFF
Operation:	I → ACC; Top of Stack → PC
Status Affected:	None
Description:	The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RETURN	**Return from Subroutine**
Syntax:	RETURN
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RLR	**Rotate Left R through Carry**
Syntax:	RLR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R<7> → C; R<6:0> → dest<7:1>; C → dest<0>
Status Affected:	C
Description:	The contents of register 'R' are rotated left one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RRR	**Rotate Right R through Carry**
Syntax:	RRR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	C → dest<7>; R<7:1> → dest<6:0>; R<0> → C
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

SLEEP	**Enter SLEEP Mode**
Syntax:	SLEEP
Operands:	None
Operation:	00h → WDT; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT is cleared. The processor is put into SLEEP mode.
Cycles:	1

SUBAR	Subtract ACC from R
Syntax:	SUBAR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SWAPR	Swap nibbles in R
Syntax:	SWAPR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	R<3:0> → dest<7:4>; R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

XORAR	Exclusive OR ACC with R
Syntax:	XORAR R, d
Operands:	0 ≤ R ≤ 0x6F d ∈ [0,1]
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	Exclusive OR Immediate with ACC
Syntax:	XORIA I
Operands:	0 ≤ I ≤ 0xFF
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-40℃ to +85℃
Store Temperature	-65℃ to +150℃
DC Supply Voltage (Vdd)	0V to +6.0V
Input Voltage with respect to Ground (Vss)	-0.3V to (Vdd + 0.3)V

5.0 OPERATING CONDITIONS

DC Supply Voltage	+2.2V to +5.5V
Operating Temperature	-40℃ to +85℃

6.0 ELECTRICAL CHARACTERISTICS

6.1 ELECTRICAL CHARACTERISTICS of FM8P73B

Ta=25℃

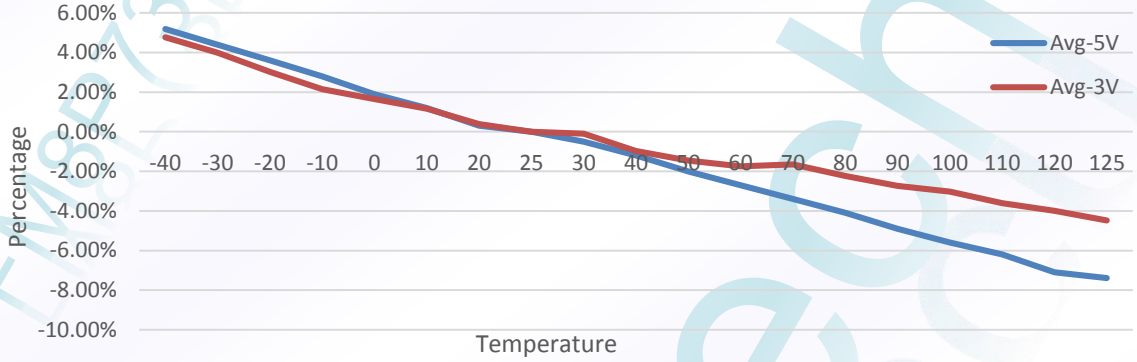
Under Operating Conditions, at four clock instruction cycles and WDT & LVDT are disabled

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
F_{HF}	X'tal oscillation range	HF mode, Vdd=5V, Fcpu=Fosc/2			20	MHz
		HF mode, Vdd=3V, Fcpu=Fosc/2			15	
F_{XT}	X'tal oscillation range	XT mode, Vdd=5V, Fcpu=Fosc/2			10	MHz
		XT mode, Vdd=3V, Fcpu=Fosc/2			10	
F_{LF}	X'tal oscillation range	LF mode, Vdd=5V, Fcpu=Fosc/2			4000	KHZ
		LF mode, Vdd=3V, Fcpu=Fosc/2			1000	
F_{ERC}	RC oscillation range	ERC mode, Vdd=5V, Fcpu=Fosc/2			15	MHz
		ERC mode, Vdd=3V, Fcpu=Fosc/2			7	
F_{IRC}	IRC Calibration range	HV mode, Vdd=5V	-3		+3	%
		LV mode, Vdd=3V	-3		+15	
V_{IH}	Input high voltage	With schmitter				V
		I/O ports	0.7Vdd		Vdd	
		RSTB pin	0.8Vdd		Vdd	
V_{IL}	Input low voltage	With schmitter				V
		I/O ports	Vss		0.2Vdd	
		RSTB pin	Vss		0.2Vdd	
I_{IL}	Input Leakage Current	Vin = 5V, Vdd=5V			1	uA
		Vin = 0V, Vdd=5V			1	
I_{OH}	IO Drive Current	VOH =4.5V, Vdd = 5V		7.5		mA
		VOH =4V, Vdd = 5V		14.5		
I_{OL}	IO Sink Current	VOL =0.5V, Vdd = 5V		13.5		mA
		VOL =0.75V, Vdd = 5V		18.5		
R_{PH}	Pull-high resister	Input pin at Vss, vdd=5V	70	140	210	KΩ
		Input pin at Vss, vdd=3V	140	280	420	
I_{WDT}	WDT current	Vdd=5V		11		uA
		Vdd=3V		2		
T_{WDT}	WDT period	Vdd=3V		22		mS
		Vdd=5V		19		
I_{LVDT}	LVDT current	LVDT = 3.5V, vdd=5V		2.5		uA
		LVDT = 2.3V, vdd=5V		3		
		LVDT = 2.3V, vdd=3V		0.6		
		LVDT = 2.0V, vdd=5V		2.5		
		LVDT = 2.0V, vdd=3V		0.5		
V_{LVDT}	LVDT voltage	LVDT = 3.5V	3.4	3.6	3.8	V
		LVDT = 2.3V	2.2	2.4	2.6	
		LVDT = 2.0V	1.9	2.1	2.3	
V_{AD}	A/D input Voltage		0		Vdd	V
R_{AD}	Resolution				10	Bits
DNL	A/D Differential Non-Linear				2	LSB
INL	A/D Integral Non-Linear				5	LSB

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
I_{ADC}	A/D Operation Current	Vdd = 5V, Fcpu=Fosc/4		500		uA
		Vdd = 3V, Fcpu=Fosc/4		100		
T_{AD}	A/D clock period		8			us
T_{ADC}	A/D Conversion Time			20		T_{AD}
T_{ADCS}	A/D Sampling Time			8		T_{AD}
I_{SB}	Power down current	Sleep mode, Vdd=5V, WDT enable, LVDT off		11		uA
		Sleep mode, Vdd=5V, WDT disable, LVDT off			1	
		Sleep mode, Vdd=3V, WDT enable, LVDT off		2		
		Sleep mode, Vdd=3V, WDT disable, LVDT off			1	
I_{DD1}	Operating current	IRC mode, vdd=5V, 4 clock instruction		0.95		mA
I_{DD2}	Operating current	IRC mode, vdd=5V, 2 clock instruction		1.4		mA
I_{DD3}	Operating current	IRC mode, vdd=3V, 4 clock instruction		0.5		mA
I_{DD4}	Operating current	IRC mode, vdd=3V, 2 clock instruction		0.7		mA
I_{DD5}	Operating current	HF mode, vdd=5V, 4 clock instruction				mA
		20MHz		4		
I_{DD6}	Operating current	HF mode, vdd=5V, 2 clock instruction				mA
		20MHz		5		
I_{DD7}	Operating current	HF mode, vdd=3V, 4 clock instruction				mA
		20MHZ		1.6		
I_{DD8}	Operating current	XT mode, Vdd=5V, 4 clock instruction				
		10MHz		2.3		mA
		4MHz		1.2		
I_{DD9}	Operating current	XT mode, Vdd=5V, 2 clock instruction				mA
		10MHz		3.5		
		4MHz		1.6		
I_{DD10}	Operating current	XT mode, Vdd=3V, 4 clock instruction				mA
		10MHz		1		
		4MHz		0.5		
I_{DD11}	Operating current	XT mode, Vdd=3V, 2 clock instruction				mA
		10MHz		1.4		
		4MHz		0.7		
I_{DD}	Operating current	LF mode, Vdd=5V, 4 clock instruction				uA
		32KHz		32		
I_{DD12}	Operating current	LF mode, Vdd=5V, 2 clock instruction				uA
		32KHz		36		
I_{DD13}	Operating current	LF mode, Vdd=3V, 4 clock instruction				uA
		32KHz		8		
I_{DD14}	Operating current	LF mode, Vdd=3V, 2 clock instruction				uA
		32KHz		10		
V_{PWM}	Operating voltage	HF mode, Clock source = F_{OSC} x2				V
		16MHz	4.3			
		8MHz	2.5			
		4MHz	2.0			

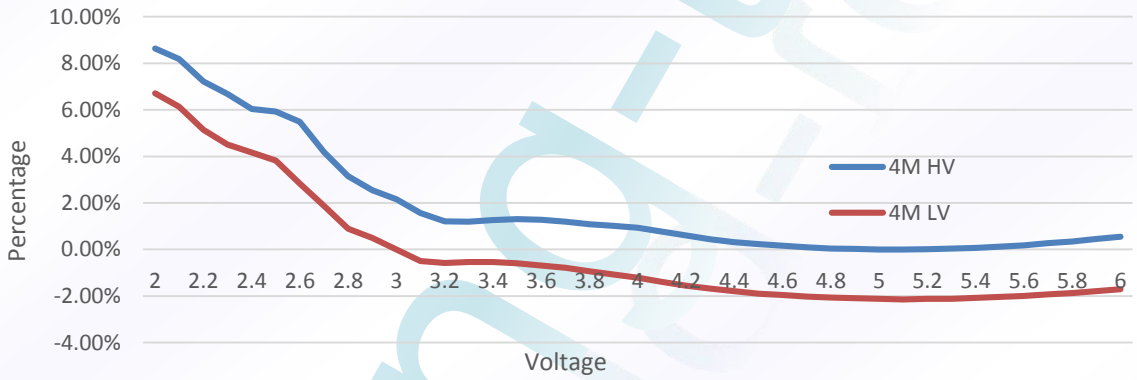
6.2 ELECTRICAL CHARACTERISTICS Charts of FM8P73B

6.2.1 Internal 4MHz RC vs. Temperature



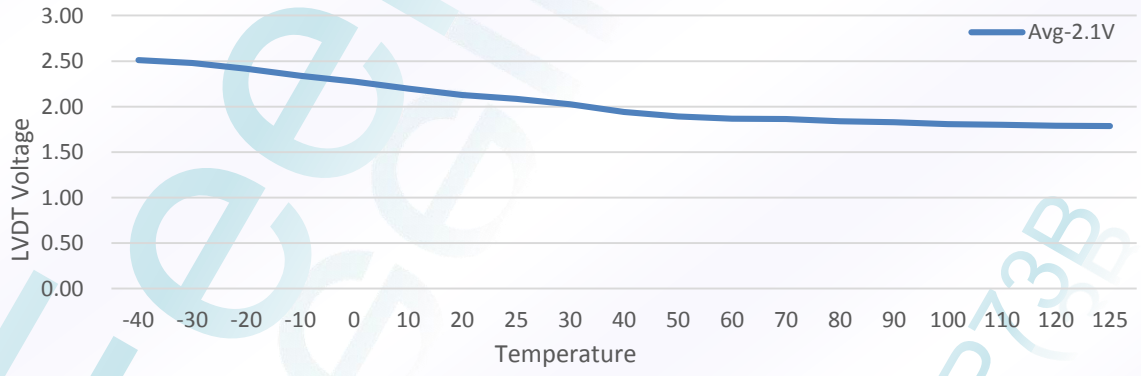
Note: Curves are for design reference only.

6.2.2 Internal 4MHz RC vs. Supply Voltage (Ta=25℃)



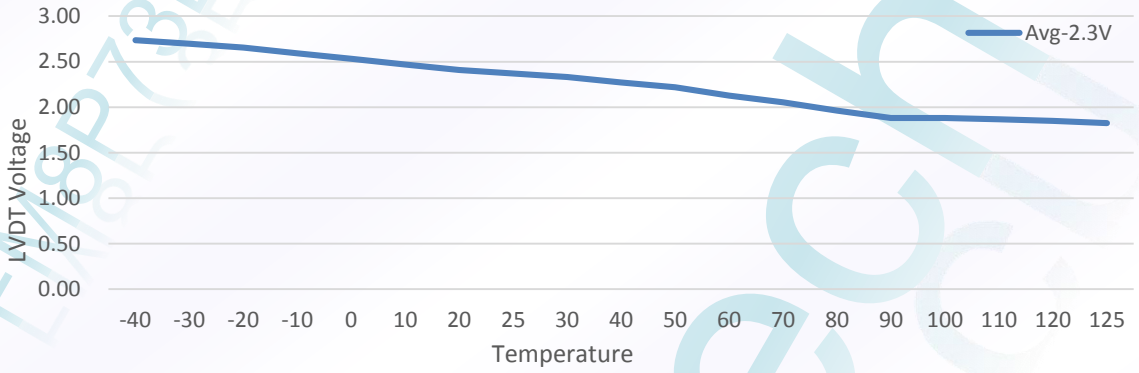
CAUTION: Less than 2.8V will exceed 3% limit.
Note: Curves are for design reference only.

6.2.3 Low Voltage Detect (LVDT=2.1V) vs. Temperature



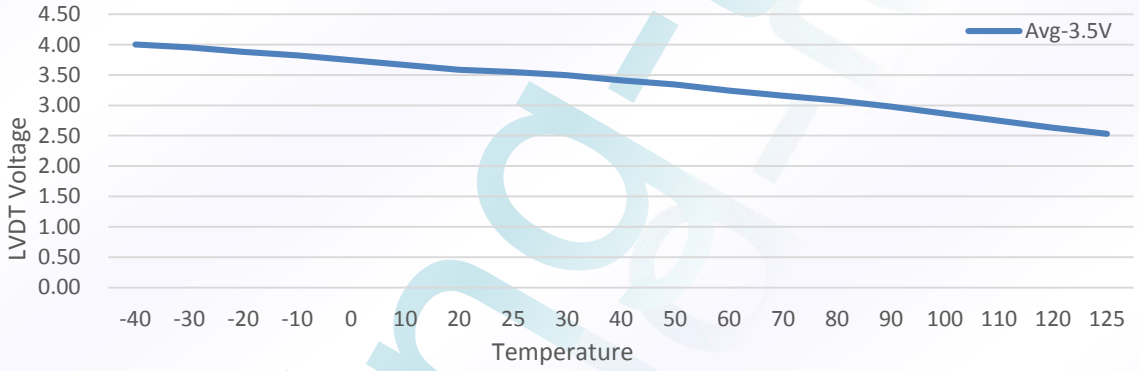
CAUTION: The LVDT 2.1V option can only support temperature range between -40~50℃
Note: Curves are for design reference only.

6.2.4 Low Voltage Detect (LVDT=2.3V) vs. Temperature



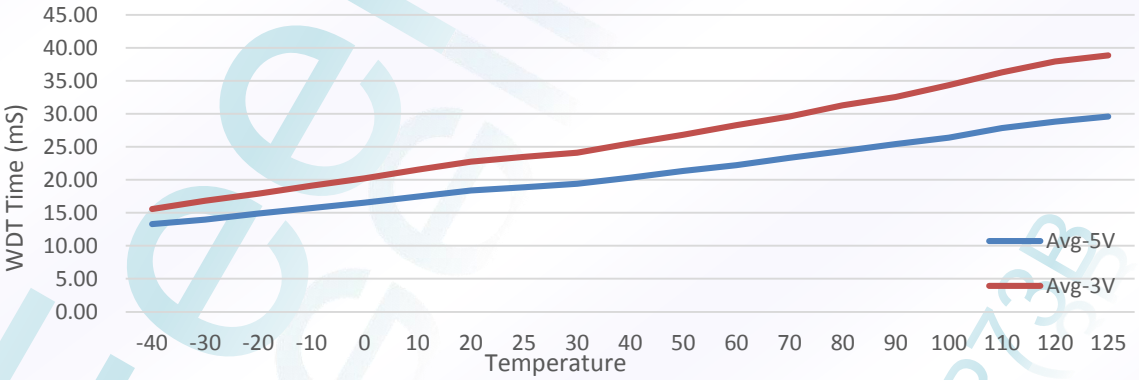
Note: Curves are for design reference only.

6.2.5 Low Voltage Detect (LVDT=3.5V) vs. Temperature



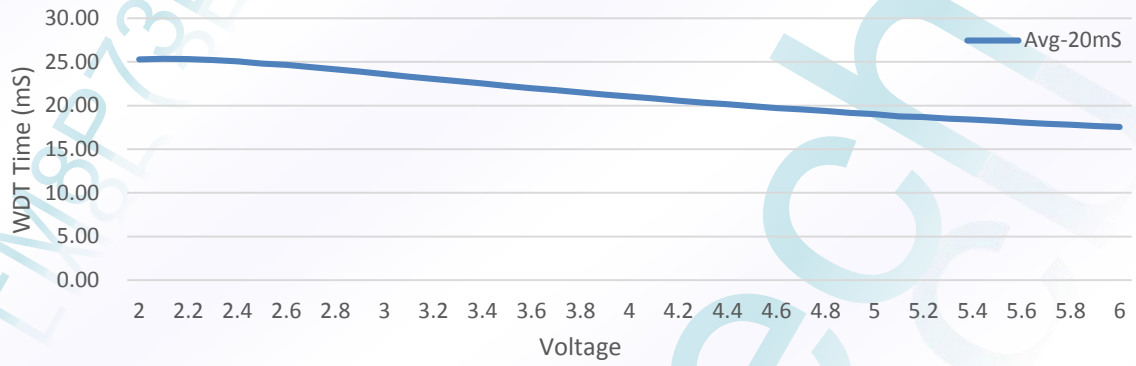
Note: Curves are for design reference only.

6.2.6 WDT 20mS Reset time vs. Temperature



Note: Curves are for design reference only.

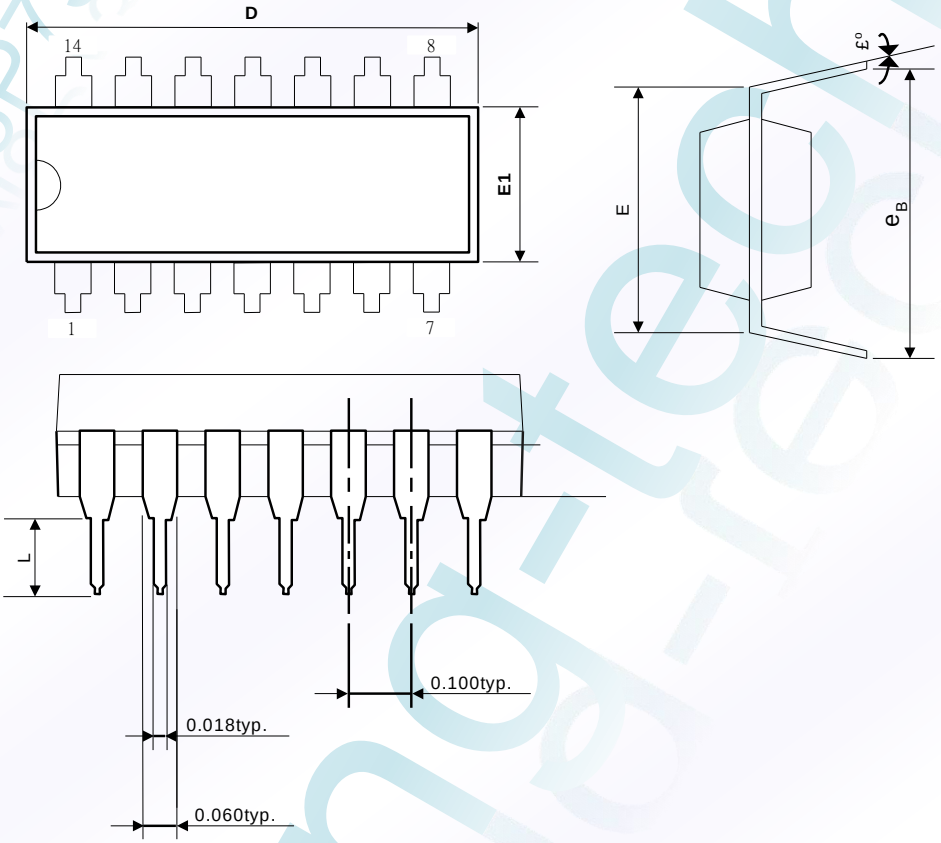
6.2.7 WDT 20mS Reset time vs. Supply Voltage (Ta=25℃)



Note: Curves are for design reference only.

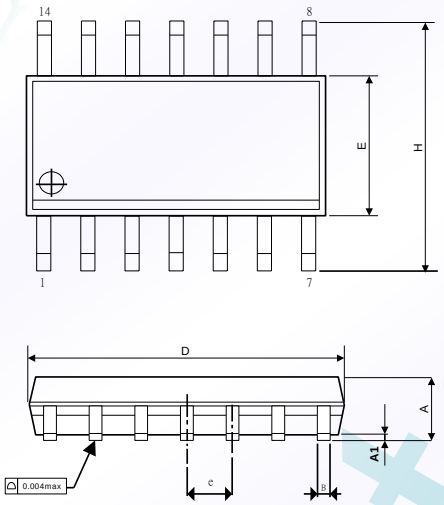
7.0 PACKAGE DIMENSION

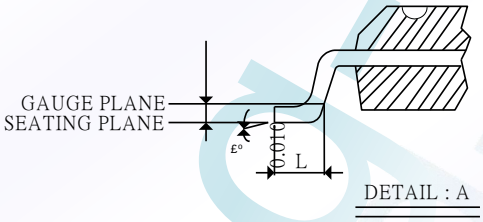
7.1 14-PIN PDIP 300mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

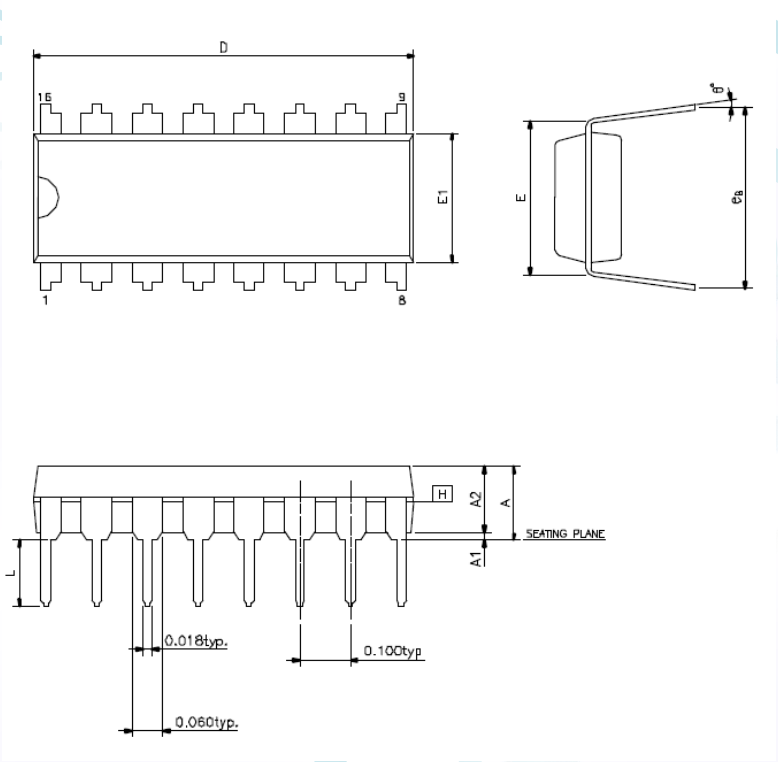
7.2 14-PIN SOP 150mil





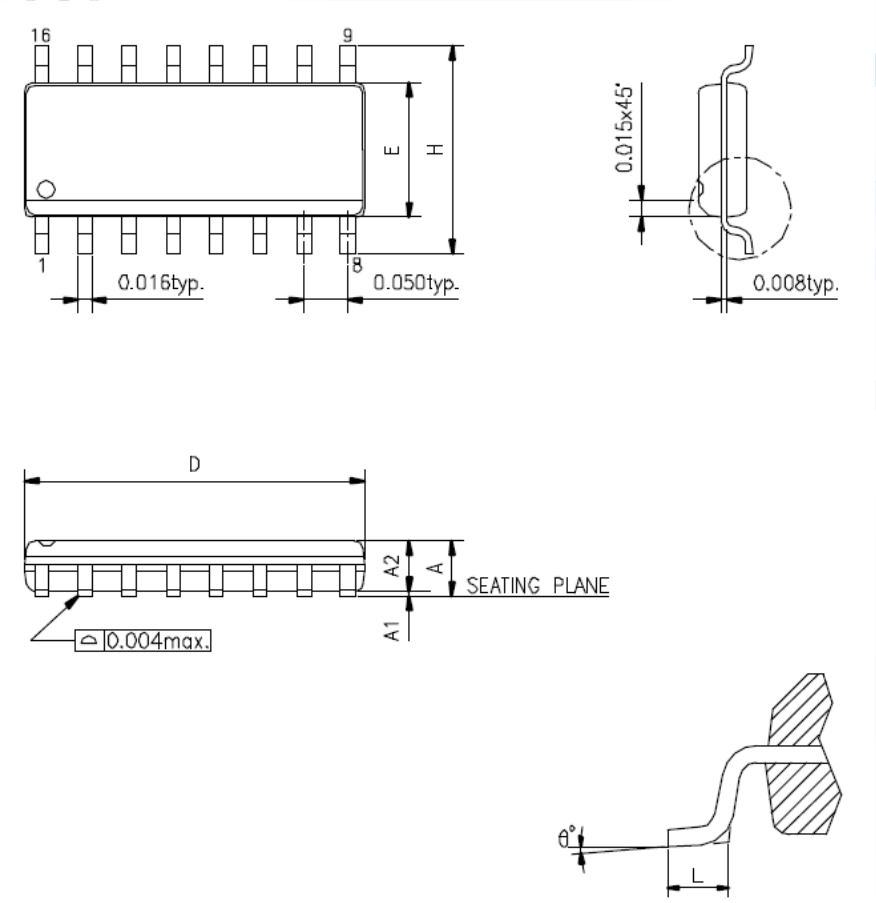
Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.058	0.064	0.068
A1	0.004	-	0.010
B	0.013	0.016	0.020
C	0.0075	0.008	0.0098
D	0.336	0.341	0.344
E	0.150	0.154	0.157
e	-	0.050	-
H	0.228	0.236	0.244
L	0.015	0.025	0.050
θ°	0°	-	8°

7.3 16-PIN PDIP 300mil



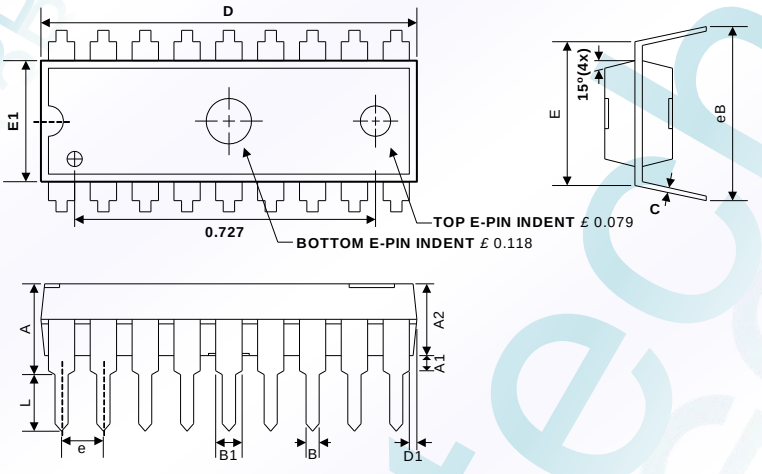
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.4 16-PIN SOP 150mil



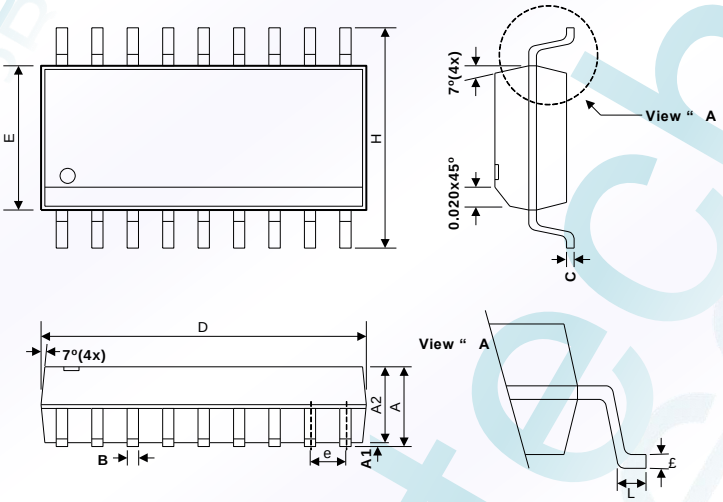
Symbols	Dimension In Inches	
	Min	Max
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0°	8°

7.5 18-PIN PDIP 300mil



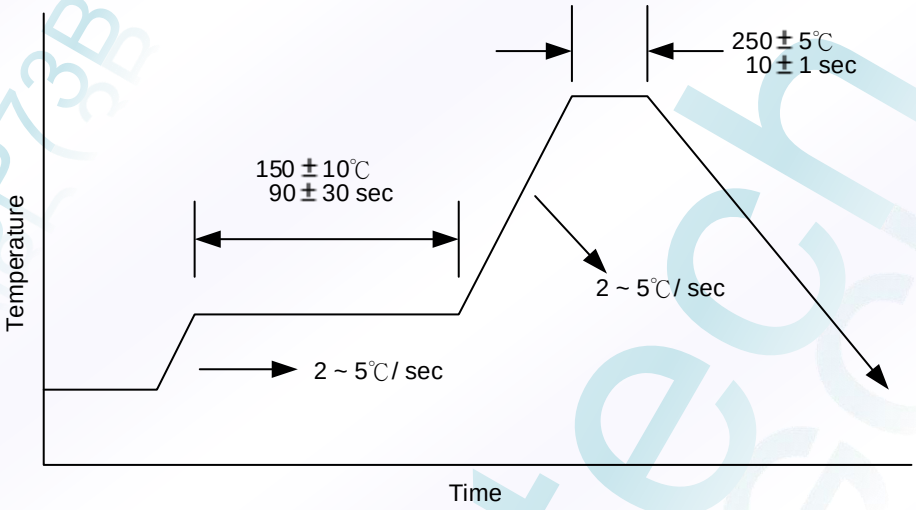
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.180
A1	0.005	-	-
A2	-	0.130	0.140
B	0.014	0.018	0.022
B1	0.050	0.060	0.070
C	0.008	0.010	0.013
D	0.894	0.904	0.910
D1	0.017	0.022	0.027
E	0.300	-	0.325
E1	0.252	0.256	0.262
e	-	0.100	-
L	0.125	-	-

7.6 18-PIN SOP 300mil



Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.093	0.098	0.104
A1	0.04	-	0.012
A2	-	0.091	-
B	0.013	0.016	0.020
C	0.007	0.009	0.011
D	0.447	-	0.463
E	0.291	0.295	0.299
e	-	0.050	-
H	0.394	0.406	0.419
L	0.015	0.032	0.050
θ°	0°	-	8°

8.0 PACKAGE IR Re-flow Soldering Curve



9.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size
FM8P73BAP	PDIP	16	300 mil
FM8P73BAD	SOP	16	150 mil
FM8P73BBP	PDIP	14	300 mil
FM8P73BBD	SOP	14	150 mil
FM8P73BCP	PDIP	18	300 mil
FM8P73BCD	SOP	18	300 mil
FM8P73BDP	PDIP	16	300 mil
FM8P73BDD	SOP	16	150 mil