FM8PC71AM

FTC 8-Bit Micro-Controller With 12-bits ADC

Datasheet R1.1.004
Aug. 7, 2017

Version Control

Version	Date.	Description
R1.0	2014/2/26	Release of prototype
R1.1	2014/5/3	Modified.
R1.1.001	2017/6/23	Update package dimension, and some bit description
R1.1.002	2017/6/27	Update LVDTA,
R1.1.003	2017/8/4	Update DC Characteristics
R1.1.004	2017/8/7	Update reg name： ADCON1/2/3, T0RLD, P0RDLB, P2RDLB, P3RDLB, EFR1, EFR2. Add R-plane Operational Registers Map

Contents

【1】FM8PC71AM REVIEW

1.1 General Description

◆ The **FM8PC71AM** is compatible with FM8PC71AS.
◆ The **FM8PC71AM** enhance operating voltage, Drive ,Sink current and EFT.

1.2 Features

■ **8-bit RISC microprocessor**
- ✧ On chip 4.0K x 14 program OTP Memory.
- ✧ 6 level stack.
- ✧ 128 bytes internal SRAM.
- ✧ Optional Firc/(1,2,4,8,16) MCU clock.
- ✧ MCU can switch to work on External/internal clock.
- ✧ One 8-bits Timer and Four 12-bits counter for PWM output.
- ✧ Watch dog Timer.

■ **System Clock**
- ✧ Internal Oscillator
  - ➢ Internal +/- 2% 16MHz Oscillator.
  - ➢ Internal oscillator 32KHz free run clock for slow/green mode.
- ✧ External crystal Oscillator
  - ➢ One operating Frequency Range of oscillator/Crystal is 32K~16M Hz.
  - ➢ One RC type up to 7MHz.

■ **13+1 I/O ports**
- ✧ High current dive on any GPIO pin: 20mA pin current drive and sink.
- ✧ Each GPIO pin supports high-impedance input, internal pull-ups, open drains output, or CMOS outputs.
- ✧ PA[2] only as input/pull-high pin.

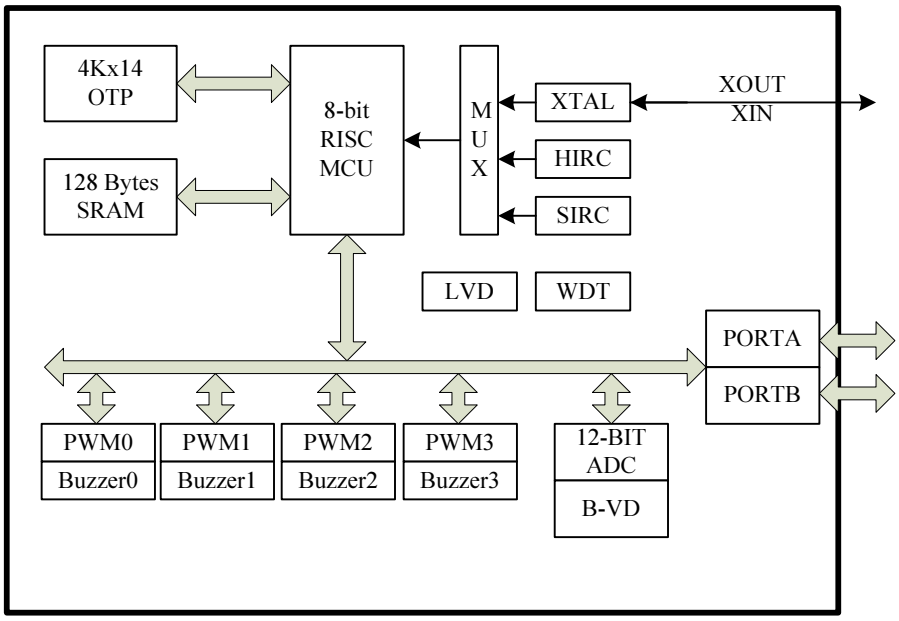
■ **7+14 interrupt sources**
- ✧ Fourteen external interrupts for any GPIO pin.
- ✧ Seven internal interrupts are Timer0, PTM0, PTM1, PTM2, PTM3, CMP, ADC;

■ **5+2 Channel 12-bit ADC/DAC.**
- ✧ Optional Continues or Trigger mode to sample.
- ✧ Support 5 channel external ADC input and an internal VDD/4 and AVSS input.
- ✧ Build in AD reference voltage (VDD, 4V, 3V, 2V) +/- 1%.
- ✧ Support one channel DAC output to PB[3] when ADC disable.

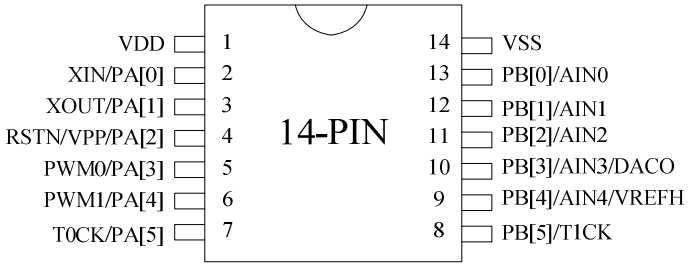
■ **Power Manager**
- ✧ Power on reset (POR) voltage is 2.1V
- ✧ Power down reset (PDR) voltage is 1.8V
- ✧ Four level Low Voltage Detect: LVDT36(3.6V), LVDTA(2.0V), LVDT24(2.4V), LVDT20(2.0V).

■ **Build in PWM(Buzzer) function.**
- ✧ Support 4 channels PWM.
- ✧ PWM0(PA[3]-H, PA[4]-L),PWM2(PA[6]-H,PA[5]-L),PWM3(PA[7]-H,PB[5]-L) can differential output.
- ✧ PWM0(BZ0)/PWM1(BZ1)/PWM2(BZ2)/PWM3(BZ3) **optional** output**.**

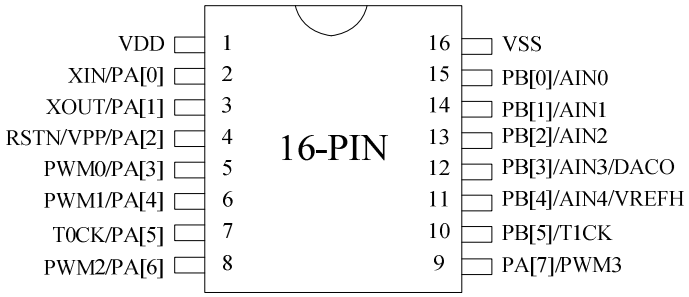
1.3 Block Diagram



1.4 Pin Definitions



FM8PC71AM-A
PDIP/SOP



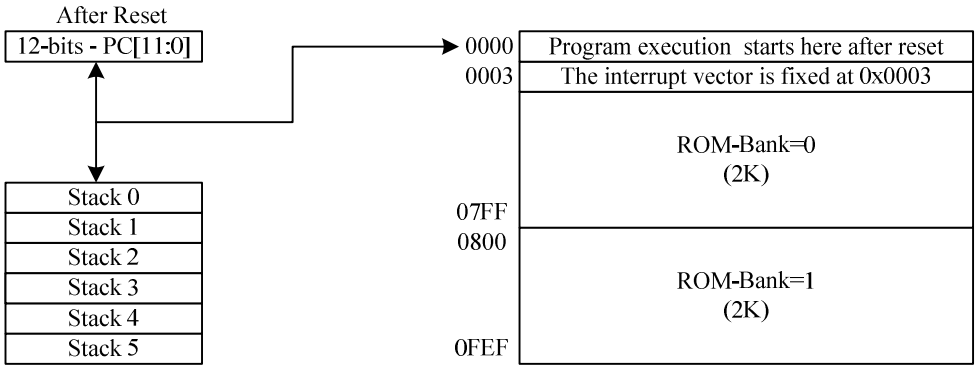
FM8PC71AM-B
PDIP/SOP

1.5 Pin Description

PIN Name	I/O	14-pin P	16-pin S	Description
PA[0] XIN	IO I	2	2	GPIO Port A [0] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Up to 16Mhz ceramic resonator or external clock input when external Crystal enable.
PA[1] XOUT	IO O	3	3	GPIO Port A [1] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Up to 16Mhz ceramic resonator or external clock output when external Crystal enable.
PA[2] VPP RSTN	I I	4	4	GPIO Port A [2] input and a resistive pull-up. (Default is pull-high) Programming voltage supply, VCC for normal operation External reset pin, active low.
PA[3] PWM0	IO O	5	5	GPIO Port A [3] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM0 signal output pin when PWM0 enable.
PA[4] PWM1	IO O	6	6	GPIO Port A [4] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM1 signal output pin when PWM1 enable.
PA[5] T0CK	IO I	7	7	GPIO Port A [5] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. Timer0 or **PWM0~3** external clock input pin
PA[6] PWM2	IO O	--	8	GPIO Port A [6]capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM2 signal output pin when PWM2 enable
PA[7] PWM3	IO O	--	9	GPIO Port A [7] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. PWM3 signal output pin when PWM3 enable
PB[5] T1CK	IO I	8	10	GPIO Port B [5] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. **PWM0~3** external clock input pin
PB[4] AIN4 VREFH	IO I	9	11	GPIO Port B [4] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-4. External high reference voltage input of ADC

PIN Name	I/O	14-pin P	16-pin S	Description
PB[3] AIN3 DACO	IO I O	10	12	GPIO Port B [3] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-3. DAC output
PB[2] AIN2	IO I	11	13	GPIO Port B [2] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-2.
PB[1] AIN1	IO I	12	14	GPIO Port B [1] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. ADC input channel-1.
PB[0] AIN0	IO I	13	15	GPIO Port B [0] capable of sinking up to 20mA/pin, or sinking controlled low or high programmable current. Can also source 20 mA drive current or provide a resistive pull-up, or serve as a high-impedance input. When chip is the power on reset, the PB[0] is pull-high 100K ohm to VDD ADC input channel-0.
VSS	G	14	16	Ground

1.6 Program Memory Mapping



(Address: 0FF0~0FFF Revered for Configuration)

1.7 Memory And Register Mapping

Table 1.7-1 I/O Register Mapping

Address	Description(F-plane)		Address	R-Plane
	RAM-Bank=0	RAM-Bank=1		
00h	INDF			
01h	--			
02h	PCL			
03h	STATUS			
04h	FSR			
05h	PORTA			
06h	PORTB			
07h	PAIE			
08h	PBIE		08h	PAMODE0
09h	PACON		09h	PAMODE1
0Ah	PBCON		0Ah	PBMODE0
0Bh	INTEN		0Bh	PBMODE1
0Ch	INTFLAG			
0Dh	--			
0Eh	TM0			
0Fh	TM0CON			
10h	T0RLD			
11h	WDT			
12h	PCON			
13h	CLKCFG			
14h	PWM0CON			
15h	PWM0CR			
16h	P0TMLB**(read)**/N0**(write)**		**16h**	**N0(read)**
17h	P0RDLB			
18h	P0TRHB			
19h	PWM1CON			
1Ah	PWM1CR			
1Bh	P1TMLB			
1Ch	P1RDLB			
1Dh	P1TRHB			
1Eh	PWM2CON			
1Fh	PWM2CR			
20h	P2TMLB**(read)**/N2**(write)**		**20h**	**N2(read)**
21h	P2RDLB			

Address	Description(F-plane)		Address	R-Plane
	RAM-Bank=0	RAM-Bank=1		
22h	P2TRHB			
23h	PWM3CON			
24h	PWM3CR			
25h	P3TMLB**(read)**/N3**(write)**		**25h**	**N3(read)**
26h	P3RDLB			
27h	P3TRHB			
28h	ADCON1		28h	ADCON3
29h	ADCON2			
30h	ADCHB**(read)**/DACR1LB**(write)**			
31h	ADCLB**(read)**/DACR1HB**(write)**			
32~34h	General Purpose Registers 3 bytes			
35h	EFR1			
36h	EFR2			
37h	CMPCON1			
38h	CMPCON2			
39h	DACR2LB			
3Ah	DACR2HB			
3B~3Fh	(Revered)			
40h | 7Fh	64 bytes	64 bytes		

*Accessed by IOST/IOSTR instruction

*The R-plane Registers are loaded with the contents of the ACC register by executing the IOST instruction. By executing the IOSTR instruction, user read these registers

1.8 Register bit Mapping

TABLE 1.8-1: F-plane Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (R/W)	**INDF**	**Uses contents of FSR to address data memory (not a physical register)**							
01h (R/W)	Revered	--							
02h (R/W)	PCL	Low order 8 bits of PC							
03h (R/W)	STATUS	--	--	--	/TO	/PD	Z	DC	C
04h (R/W)	FSR	Indirect data memory address pointer							
05h (r/w)	PORTA	PA[7:0]							
06h (r/w)	PORTB	--	--	PB[5:0]					
07h (r/w)	PAIE	PAIE7	PAIE6	PAIE5	PAIE4	PAIE3	PAIE2	PAIE1	PAIE0
08h (r/w)	PBIE	--	--	PBIE5	PBIE4	PBIE3	PBIE2	PBIE1	PBIE0
09h (r/w)	PACON	PACON7	PACON6	PACON5	PACON4	PACON3	PACON2	PACON1	PACON0
0Ah (r/w)	PBCON	--	--	PBCON5	PBCON4	PBCON3	PBCON2	PBCON1	PBCON0
0BH(R/W)	INTEN	GIE	--	--	--	--	--	--	TM0IE
0Ch (R/W)	INTFLAG	PBIF	PAIF	--	--	--	--	--	TM0IF
0Dh(R/W)	--	--			--	--	--	--	--
0Eh(R/W)	TM0	8-bit real time clock/counter							
0Fh(R/W)	TM0CON	TM0EN	--	TM0PS[2:0]			TM0CKS[1:0]		--
10h(R/W)	T0RLD	T0RLD7	T0RLD6	T0RLD5	T0RLD4	T0RLD3	T0RLD2	T0RLD1	T0RLD0
11h(R/W)	WDT	WDTE	WDTSL	WDTPS2	WDTPS1	WDTPS0	LVRSL	--	--

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
12h(R/W)	PCON	SUSPD	GRN_MD	LVDIS	RSTSL1	RSTSL0	LVDT36	LVDT24	LVDT20
13h(R**/W**)	CLKCFG	SELCLK2	SELCLK1	SELCLK0	CLKSW	SIRCEN	INCODS	EXOSEN	IRCEN
14h(R/w)	PWM0CON	P0INTSL	P0DT2	P0DT1	P0DT0	P0CKS2	P0CKS1	P0CKS0	--
15h(R/w)	PWM0CR	PWM0EN	P0OUTS	P0TPS[2:0]			P0TMEN	P0TMIE	P0TMIF
16h(R)	P0TMLB	P0TM7	P0TM6	P0TM5	P0TM4	P0TM3	P0TM2	P0TM1	P0TM0
16h(W)	N0	N0[7:0]							
17h(R/W)	P0RDLB	P0TRD7	P0TRD6	P0TRD5	P0TRD4	P0TRD3	P0TRD2	P0TRD1	P0TRD0
18h(R/W)	P0TRHB	P0TM11	P0TM10	P0TM9	P0TM8	P0TRD11	P0TRD10	P0TRD9	P0TRD8
19h(R/W)	PWM1CON	P1INTSL	P1DT2	P1DT1	P1DT0	P1CKS2	P1CKS1	P1CKS0	--
1Ah(R/W)	PWM1CR	PWM1EN	P1OUTS	P1TPS[2:0]			P1TMEN	P1TMIE	P1TMIF
1Bh(R)	P1TMLB	P1TM7	P1TM6	P1TM5	P1TM4	P1TM3	P1TM2	P1TM1	P1TM0
1Ch(R/W)	P1RDLB	P1TRD7	P1TRD6	P1TRD5	P1TRD4	P1TRD3	P1TRD2	P1TRD1	P1TRD0
1Dh(R/W)	P1TRHB	P1TM11	P1TM10	P1TM9	P1TM8	P1TRD11	P1TRD10	P1TRD9	P1TRD8
1Eh(R/W)	PWM2CON	P2INTSL	P2DT2	P2DT1	P2DT0	P2CKS2	P2CKS1	P2CKS0	--
1Fh(R/W)	PWM2CR	PWM2EN	P2OUTS	P2TPS[2:0]			P2TMEN	P2TMIE	P2TMIF
20h(R)	P2TMLB	P2TM7	P2TM6	P2TM5	P2TM4	P2TM3	P2TM2	P2TM1	P2TM0
20h(W)	N2	N2[7:0]							
21h(R/W)	P2RDLB	P2TRD7	P2TRD6	P2TRD5	P2TRD4	P2TRD3	P2TRD2	P2TRD1	P2TRD0
22h (R/W)	P2TRHB	P2TM11	P2TM10	P2TM9	P2TM8	P2TRD11	P2TRD10	P2TRD9	P2TRD8
23h(R/W)	PWM3CON	P3INTSL	P3DT2	P3DT1	P3DT0	P3CKS2	P3CKS1	P3CKS0	-
24h(R/W)	PWM3CR	PWM3EN	P3OUTS	P3TPS[2:0]			P3TMEN	P3TMIE	P3TMIF
25h(R)	P3TMLB	P3TM7	P3TM6	P3TM5	P3TM4	P3TM3	P3TM2	P3TM1	P3TM0
25h(W)	N3	N3[7:0]							
26h(R/W)	P3RDLB	P3TRD7	P3TRD6	P3TRD5	P3TRD4	P3TRD3	P3TRD2	P3TRD1	P3TRD0
27h(R/W)	P3TRHB	P3TM11	P3TM10	P3TM9	P3TM8	P3TRD11	P3TRD10	P3TRD9	P3TRD8
28h(R/W)	ADCON1	ADCEN	ADCST	CHSL2	CHSL1	CHSL0	--	ADCSR1	ADCSR0
29h(R/W)	ADCON2	ADCIE	ADCIF	SVERFH	ADCNT	**DACEN**	ADCTMS	SELVER1	SELVER0
30h(R)	ADCHB	ADCB[11]	ADCB[10]	ADCB[9]	ADCB[8]	ADCB[7]	ADCB[6]	ADCB[5]	ADCB[4]
31h(R)	ADCLB	--	--	--	--	ADCB[3]	ADCB[2]	ADCB[1]	ADCB[0]
30h(W)	DACR1LB	DACR1 [7:0]							
31h(W)	DACR1HB					DACR1[11:8]			
32h(R/W)	GPR1	General Purpose Register bytes 1							
33h(R/W)	GPR2	General Purpose Register bytes 2							
34h(R/W)	GPR3	General Purpose Register bytes 3							
35h(R/W)	EFR1	ROMBK	RAMBK	FRP	SPSEL	BZ3	BZ2	BZ1	BZ0
36h(R/W)	EFR2	ATSW	SIGN	LVDTA	SPB34EN	--	--	--	--
37h**(R/W)**	CMPCON1	CMPEN	COP1	CMPIE1	CMPRIF1	CMPFIF1	CMPCS[2:0]		
38h**(R/W)**	CMPCON2	CMPINT1	COP2	CMPIE2	CMPRIF2	CMPFIF2	CMPINT2	TOGGLE[1:0]	
39h**(R/W)**	DACR2LB	DACR2[7:0]							
3Ah**(R/W)**	DACR2HB					DACR2[11:8]			

Legend: - = unimplemented, read as '0',

TABLE 1.8-2: R-plane Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
I/O PAD Mode									
08h (r/w)	PAMODE0	PAM0[7:0]							
09h (r/w)	PAMODE1	PAM1[7:0]							
0Ah (r/w)	PBMODE0	--	--	PBM0[5:0]					
0Bh (r/w)	PBMODE1	--	--	PBM1[5:0]					
PWM Counter									
16h(r)	**N0**	N0[7:0]							
20h(r)	**N2**	N2[7:0]							
25h(r)	**N3**	N3[7:0]							
ADC									
28h (r/w)	ADCON3	ADCTEST	--						

Note : R-Plane Register Accessed by IOST/IOSTR instruction

1.9 Table of Optional configuration

<table>
<tr><th>Config Name</th><th>Description</th><th>Default</th></tr>
<tr><td>SELXOUT[1:0]</td><td>Select IRC output Clock
<table>
<tr><td>SLEXOUT [1:0]</td><td>Frequency</td></tr>
<tr><td>2’b11</td><td>Firc = 16Mhz</td></tr>
<tr><td>2’b10</td><td>Firc/2 = 8Mhz</td></tr>
<tr><td>2’b01</td><td>Firc/4 = 4Mhz</td></tr>
<tr><td>2’b00</td><td>Firc /8 = 2Mhz</td></tr>
</table></td><td>2b11</td></tr>
<tr><td>SLEXCLK</td><td>Select External Clock
<table>
<tr><td>SLEXCLK [1:0]</td><td>External clock source</td></tr>
<tr><td>2’b11</td><td>Use internal IRC</td></tr>
<tr><td>2’b10</td><td>Select external OSC</td></tr>
<tr><td>2’b01</td><td>Select external RC</td></tr>
<tr><td>2’b00</td><td>Select external crystal</td></tr>
</table></td><td>2’b11</td></tr>
<tr><td>SelCpuClk[2:0]</td><td>Select Fcpu = (Fosc or FIRC)/N clock
<table>
<tr><td>SelCpuClk[2:0]</td><td>Fcpu</td></tr>
<tr><td>3’b111</td><td>1MHz</td></tr>
<tr><td>3’b011</td><td>2MHz</td></tr>
<tr><td>3’b010</td><td>4MHz</td></tr>
<tr><td>3’b001</td><td>8Mhz</td></tr>
<tr><td>--</td><td>--</td></tr>
</table></td><td>3’b111</td></tr>
<tr><td>INSWDY</td><td>Internal clock switch to external clock delay time
1 = 128us delay
0 = 4ms delay</td><td>1’b1</td></tr>
<tr><td>WDTSEL</td><td>Watch dog time out select
WDTSEL[1:0] : 2’b00 = 128 ms
2’b01 = 512 ms
2’b10 = 8 ms
2’b11 = 32 ms</td><td>2’b11</td></tr>
<tr><td>XTAL32KENB</td><td>When SLEXCLK=2’b00
1 : 16M~500K Crystal
0 : 500K~32Khz Crystal</td><td>1’b1</td></tr>
<tr><td>selPor</td><td>Power on reset extend timing
SelPor[1:0] : 2’b00 = 660us
2’b01 = 4 ms
2’b10 = 8 ms
2’b11 = 16 ms</td><td>11</td></tr>
<tr><td>PROTECT</td><td>1: No protect ROM code
0: Protect ROM code</td><td>1→ no protect</td></tr>
</table>

【2】Macro-Controller UNIT

2.1 Indirect Addressing Define

The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly(FSR="0") will read 0x00.Writing to the INDF register indirectly results in a no-operation.
The bits 6~0 of FSR register can be select up to 128 registers by accessed. (address 00~7fh).

Address 00H: Indirect Addressing Register (INDF)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Address 04H: File select Register(FSR)

Bits	7	6	5	4	3	2	1	0
Name	File select register to define address in indirect addressing mode only 7 bits							
Read/Write	**R**	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example: How to used instruction at Indirect addressing
(1) Write AA data to Register (address=8'h7Fh)

```
MOVIA    7Fh
MOVAR    FSR        ;  Register address pointer is 7Fh
MOVIA    AAh
MOVAR    INDF       ; Move  data = AAh to address = 7Fh register
```

(2) Read register(7Fh) to ACC

```
MOVIA    7Fh
MOVAR    FSR        ;  Register address pointer is 7Fh
MOVR     INDF,A     ; Move  contents of register(7Fh) to ACC
```

2.2 Program Counter least significant 8 bits

A special computed GOTO is accomplished by adding an offset to the program counter (ADDAR PCR,R). When doing a table read using this method, care should be taken if the table location crosses a PCL memory boundary (256-word block).

Address 02H: Low bytes of Program Counter(PCL)

Bits	7	6	5	4	3	2	1	0
Name	Uses contents of FSR to address data memory							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Example: Create table

```
        MOVR   TABLECNT,A
        CALL    TABLE1
        .
        .
TABLE1  : ADDAR   PCL,R        ;  PCL = TABLECNT
        RETIA     00h          ; TABLECNT=0
        RETIA     01H          ; TABLECNT=1
        RETIA     02H          ; TABLECNT=2
        RETIA     02H          ; TABLECNT=3
```

2.3 Status Register

This register contains the arithmetic status of the ALU, the RESET status.
If the STAUTS Register the destination for an instruction the affects the Z, DC or C bits, then the write to these three bits disabled. These bits are set or cleared according to the logic. Furthermore, the /TO and /PD bits are not writable.

Address 03H: Status Register(STATUS)

Bits	7	6	5	4	3	2	1	0
Name	Revered	Revered	Revered	/TO	/PD	Z	DC	C
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[4] : /TO
WDT overflow flag bit.
1 = After power on or by the CLRWDT or SLEEP instruction.
0 = A watch-dog time overflow.

Bit[3] : /PD
Power down flag flag.
1 = After power on or by the CLRWDT instruction.
0 = By the SLEEP instruction.

Bit[2] : Z
Zero flag
1 = The result of a logic operation is zero.
0 = The result of a logic operation is not zero.

Bit[1] : DC
Auxiliary carry flag or borrow flag
ADDAR, ADDIA
1 = A carry from the 4th low order bit of the result occurred.
0 = A carry from the 4th low order bit of the result did not occur.
SUBAR, SUBIA
1 = A borrow from the 4th low order bit of the result did not occur.
0 = A borrow from the 4th low order bit of the result occurred.

Bit[0] : C
Carry flag or borrow flag.
ADDAR, ADDIA, RLR
1 = A carry occurred.
0 = A Carry did not occur.
SUBAR, ADDIA, RRR
1 = A borrow did not occurred.
0 = A borrow occurred.

2.4 General Purpose I/O ports

Ports A are 8 bits I/O register. Ports B are 6 bits I/O register, each bit can also selected as an external interrupt source for the microcontroller.
***Figure* 2-4.1** shows a diagram of a GPIO port pin.
Refer **TABLE 2.4.3-1**, each pin can be independently configured as high-impedance inputs, inputs with internal pull-ups, open drain outputs, or traditional outputs.
After reset, all GPIO data and controlled mode register is cleared, so the GPIO pins are as input mode.

2.4.1 PortA, PortB data define

Address 05H: Port A(PORTA)

Bits	7	6	5	4	3	2	1	0
Name	PA[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PA[7:0] data input/Ouput
1 = Port pin is logic HIGH
0 = Port pin is logic LOW

Address 06H: Port B(PORTB)

Bits	7	6	5	4	3	2	1	0
Name	--	--	PB[5:0]					
Read/Write	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0]: PB[5:0] data input/output
1 = Port pin is logic HIGH
0 = Port pin is logic LOW

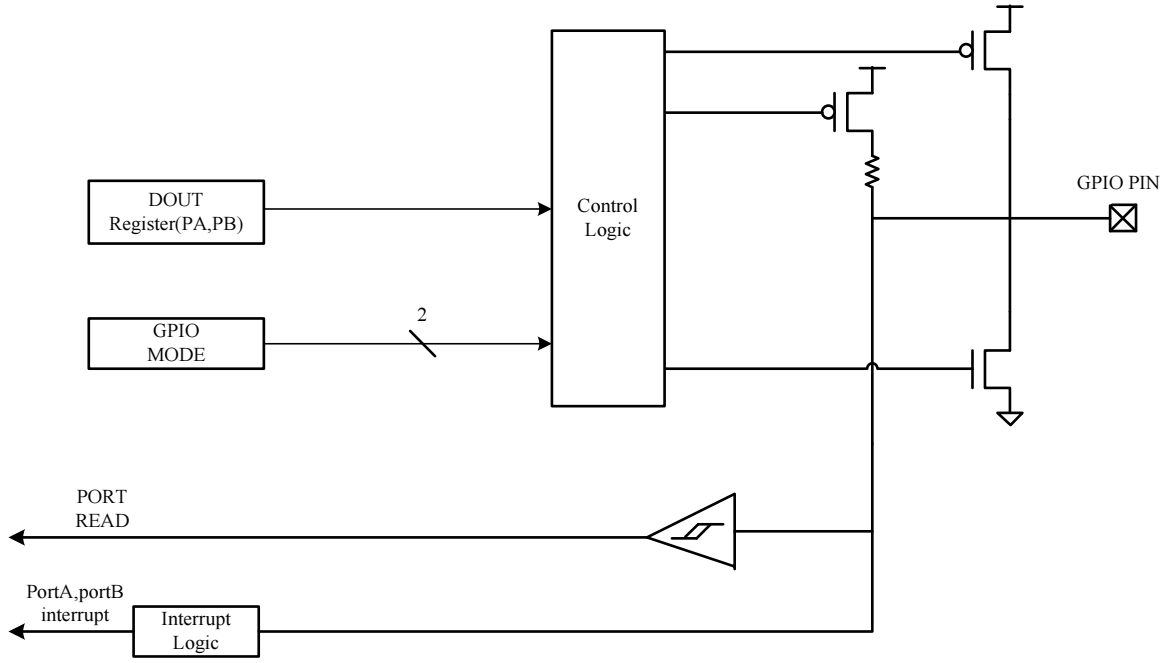


Figure 2.4-1 Block diagram of GPIO Port

2.4.2 PortA, PortB Interrupt define

Address 07H: Port A Interrupt Control Register(PAIE)

Bits	7	6	5	4	3	2	1	0
Name	PAIE7	PAIE6	PAIE5	PAIE4	PAIE3	PAIE2	PAIE1	PAIE0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PAIE7
PA[7] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[6] : PAIE6
PA[6] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[5] : PAIE5
PA[5] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[4] : PAIE4
PA[4] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[3] : PAIE3
PA[3] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[2] : PAIE2
PA[2] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : PAIE1
PA[1] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : PAIE0
PA[0] interrupt enable bit.
1 = Enable.
0 = Disable.

Address 08H: Port B Interrupt Control Register(PBIE)

Bits	7	6	5	4	3	2	1	0
Name	--	--	PBIE5	PBIE4	PBIE3	PBIE2	PBIE1	PBIE0
Read/Write	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[5] : PBIE5
PB[5] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[4] : PBIE4
PB[4] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[3] : PBIE3
PB[3] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[2] : PBIE2
PB[2] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[1] : PBIE1
PB[1] interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : PBIE0
PB[0] interrupt enable bit.
1 = Enable.
0 = Disable.

Address 09H: Port A Wake-Up Control Register(PACON)

Bits	7	6	5	4	3	2	1	0
Name	PACON7	PACON6	PACON5	PACON4	PACON3	PACON2	PACON1	PACON0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PACON7
PA[7] control bit.
1 = PA[7] Pin-changed to interrupt.
0 = PA[7] falling edge to interrupt.

Bit[6] : PACON6
PA[6] control bit.
1 = PA[6] Pin-changed to interrupt.
0 = PA[6] falling edge to interrupt.

Bit[5] : PACON5
PA[5] control bit.
1 = PA[5] Pin-changed to interrupt.
0 = PA[5] falling edge to interrupt.

Bit[4] : PACON4
PA[4] control bit.
1 = PA[4] Pin-changed to interrupt.
0 = PA[4] falling edge to interrupt.

Bit[3] : PACON3
PA[3] control bit.
1 = PA[3] Pin-changed to interrupt.
0 = PA[3] falling edge to interrupt.

Bit[2] : PACON2
PA[2] control bit.
1 = PA[2] Pin-changed to interrupt.
0 = PA[2] falling edge to interrupt.

Bit[1] : PACON1
PB[1] control bit.
1 = PA[1] Pin-changed to interrupt.
0 = PA[1] falling edge to interrupt.

Bit[0] : PACON0
PA[0] control bit.
1 = PA[0] Pin-changed to interrupt.
0 = PA[0] falling edge to interrupt

Address 0AH: Port B Wake-Up Control Register(PACON)

Bits	7	6	5	4	3	2	1	0
Name	--	--	PBCON5	PBCON4	PBCON3	PBCON2	PBCON1	PBCON0
Read/Write	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[5] : PBCON5
PB[5] control bit.
1 = PB[5] Pin-changed to interrupt.
0 = PB[5] falling edge to interrupt.

Bit[4] : PBCON4
PB[4] control bit.
1 = PB[4] Pin-changed to interrupt.
0 = PB[4] falling edge to interrupt.

Bit[3] : PBCON3
PB[3] control bit.
1 = PB[3] Pin-changed to interrupt.
0 = PB[3] falling edge to interrupt.

Bit[2] : PBCON2
PB[2] control bit.
1 = PB[2] Pin-changed to interrupt.
0 = PB[2] falling edge to interrupt.

Bit[1] : PBCON1
PB[1] control bit.
1 = PB[1] Pin-changed to interrupt.
0 = PB[1] falling edge to interrupt.

Bit[0] : PBCON0
PB[0] control bit.
1 = PB[0] Pin-changed to interrupt.
0 = PB[0] falling edge to interrupt

2.4.3 PortA, PortB Mode define

Address 08H: Port A Mode0 Control Register(PAMODE0)

Bits	7	6	5	4	3	2	1	0
Name	PAM0[7]	PAM0[6]	PAM0[5]	PAM0[4]	PAM0[3]	PAM0[2]	PAM0[1]	PAM0[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PA [7:0] Mode0

1 = Port pin Mode 0 is logic HIGH
0 = Port pin Mode 0 is logic LOW

Address 09H: Port A Mode1 Control Register(PAMODE1)

Bits	7	6	5	4	3	2	1	0
Name	PAM1[7]	PAM1[6]	PAM1[5]	PAM1[4]	PAM1[3]	PAM1[2]	PAM1[1]	PAM1[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PA [7:0] Mode 1

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 1 is logic LOW

Note: PA[2] default is pull high

Address 0AH: Port B Mode1 Control Register(PBMODE0)

Bits	7	6	5	4	3	2	1	0
Name	--	--	PBM0[5]	PBM0[4]	PBM0[3]	PBM0[2]	PBM0[1]	PAM0[0]
Read/Write	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PB [5:0] Mode 0

1 = Port pin Mode 0 is logic HIGH
0 = Port pin Mode 0 is logic LOW

Address 0BH: Port B Mode1 Control Register(PBMODE1)

Bits	7	6	5	4	3	2	1	0
Name	--	--	PBM1[5]	PBM1[4]	PBM1[3]	PBM1[2]	PBM1[1]	PBM1[0]
Read/Write	--	--	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7:0] : PB [5:0] Mode 1

1 = Port pin Mode 1 is logic HIGH
0 = Port pin Mode 1 is logic LOW

Note: When chip is power on reset (VDD < POR), the PB[0] is pull-high mode(pull high 100K).
When chip is after power on reset (VDD > POR), the PB[0] is input mode.

Each pin of PORTA, PORTB mode is define by as follows **TABLE 2.4.3-1:**

TABLE 2.4.3-1 Port A and B Output control truth Table

Data register	Mode1	Mode0	Output Drive Strength
1	0	0	HI-z (Input mode)
0			
1	0	1	Normal Drive (20mA**)**
0			Sink (20mA)
1	1	0	Resistive(100KΩ)
0			Sink (20mA)
1	1	1	Normal Drive (20mA**)**
0			Sink (20mA)

2.5 Watchdog Timer(WDT)

The Watchdog Timer (WDT) is a free running on chip RC oscillator which does not require any external components. So the WDT will still run into GREEN mode. During normal operation or in GREEN mode, a WDT time-out will cause base on Configuration option to the device reset.

Configuration WDTSEL[1:0]	VDD=5V~2.4V SIRC = 32Khz, WDT Time out
2'b11	32 ms
2'b10	8 ms
2'b01	512 ms
2'b00	128 ms

The CLRWDT instruction clears the WDT, if assigned to the WDT, and prevents it from timing out and generating a device reset.
The WDT can be disabled by clearing the control bit WDTE(11h-7). The WDT has a normal time-out period of 32ms (without precaler). When the SLEEP instruction executes, the MCU will be reset or go next instruction on WDT time-out.
The prescaler of WDT refers **Table2.5-1**.
The block diagram of WDT shows in ***Figure* 2.5-2**.

Address 11H: Watchdog Timer(WDT)

Bits	7	6	5	4	3	2	1	0
Name	WDTE	WDTSL	WDTPS[2:0]			LVRSL	--	--
Read/Write	R/W	R/W	R/W			R/W	--	--
Default	1	1	0	0	0	0	0	0

Bit[7] : WDTE
Watch-Dog timer enable.
1 = Enable.
0 = Disable.
Bit[6] : WDTSL
Watch-dog timer out selects.
1 = If Watch-dog timer out, the Device be reset. (PC = 0000h)
0 = If Watch-dog timer out, Device be wake up and PC = PC+1. (GRN_MD bit in 12h register be clear)

Bit[5:3] : WDTPS[2:0]
WDT Prescaler, please refer **Table 2.5-1**.

WDTPS[2:0]	WDT time out(config = 32ms)
3'b000	32ms*1 = 32 ms
3'b001	32ms*2 = 64 ms
3'b010	32ms *4 = 128 ms
3'b011	32ms *8 = 256 ms
3'b100	32ms *16 = 512 ms
3'b101	32ms *32 = 1024 ms
3'b110	32ms *64 = 2048 ms
3'b111	32ms *128 = 4096 ms

TABLE 2.6-1 WDT Prescaler

Bit[2] : LVRSL
LVR select.
1 = When Device is in green mode, the LVR signal can wake up to normal mode(PC=PC+1).
0 = When Device is in green mode, the LVR signal will be reset chip(PC=0x000).

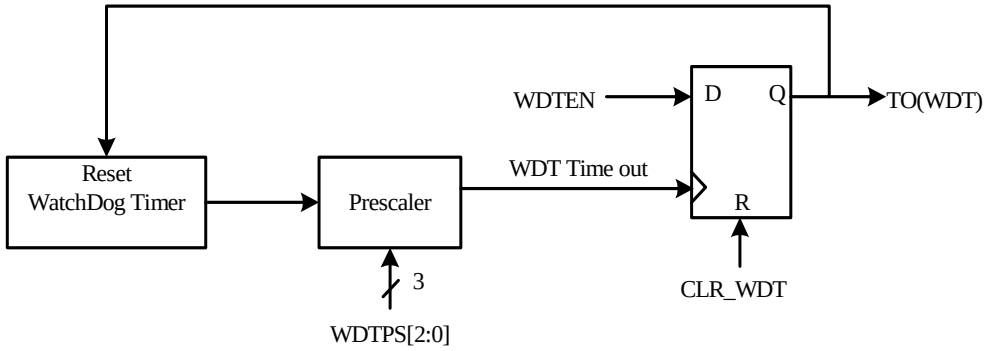


Figure **2.5-2 Block Diagram of WDT**

【3】Power and Reset Management

There are Four cases of reset on MCU controller chip. These cases of reset occurrence are listed below.

1. Power On/Down Reset (normal mode)
   - ◆ POR (VDD ≤ 2.1V), PDR (VDD ≤ 1.8V)
2. Brown out reset
   - ◆ LVDT20 (VDD ≤ LVR1 ==2.0V for > 100ns)
   - ◆ LVDT24 (VDD ≤ LVR2 ==2.4V for > 100ns)
   - ◆ LVDT36 (VDD ≤ LVR3 ==3.6V for > 100ns)
3. Watchdog Reset
   - ◆ WDR (Watch Dog time out)
4. External Reset
   - ◆ EXTR (External Reset PA[2] Low active)
5. Power down Reset (sleep mode)
   - ◆ PDRS (VDD ≤ 1.3V)

If the POR, PDR, PDRS, WDR, LVDT20, LVDT24, EXR or PDRS occurs, the chip will enter reset status. The following events take place on reset status.

- ◆ All registers are reset to their default values expect status registers.
- ◆ The status register (03h) is reset to their default value only for POR/PDR.
- ◆ After reset status, program counter begins at address 0x0000

PORN is asserted when VDD voltage to the device is upper approximately 2.4V (see *Figure* 3.0-1).

Address 12H: Power Control Register (PCON)

Bits	7	6	5	4	3	2	1	0
Name	SUSPD	GRN_MD	LVDIS	RSTSL[1:0]		LVDT36	LVDT24	LVDT20
Read/Write	R/W	R/W	R/W	R/W	R/W	R	R	R
Default	0	0	0	0	0	0	0	0

Bit][7] : SUSPD

F/W force system to go into suspend mode.
1 = Suspend mode.
0 = The other operation mode.

Bit][6:5] : GRN_MD,LVDIS

{GRN_MD,LVDIS}	Description
2'b00	Normal Mode(SUSPEND=0), and All LVD36, LVDT20, LVDT24 circuit are enable
2'b01	First switch Fcpu clock is Fsirc. Slow Mode(SUSPEND=0), and All LVD36, LVDT20, LVDT24 circuit are disable Fcpu enable (Fcpu = Fsirc),
2'b10	Green Mode(SUSPEND=0), and All LVD36, LVDT20, LVDT24 circuit are enable Fcpu Disable.
2'b11	Green Mode(SUSPEND=0), and All LVD36, LVDT20, LVDT24 circuit are disable Fcpu Disable.

Bit[4:3] : RSTSL[1:0]*

RSTSL[1:0]	Description
2'b00	POR, WDR can reset system chip.
2'b01	POR, WDR, LVDT2.0 (VDD<= 2.0V) can reset system chip
2'b10	POR, WDR, LVDT24 (VDD<= 2.4V) can reset system chip
2'b11	POR, WDR, EXR can reset system chip.

*POR, PDR, PDRS occurs, the **RSTSL[1:0] bits** can be reset to default value.

*WDR, LVDT24, LVDT2.0 or EXR occurs, the **RSTSL[1:0] bits** can't be reset to default value.

Bit[2] : LVDT36 (Read only)

Low Voltage(3.6V) detect signal.
1 = VDD voltage >= 3.6V.; 0 = VDD voltage < 3.6 V

Bit[1] : LVDT24(Read only)

Low Voltage(2.4V) detect signal.
1 = VDD voltage >= 2.4V.
0 = VDD voltage < 2.4V

Bit[0] : LVDT20(Read only)

Low Voltage(2.0V) detect signal.
1 = VDD voltage >= 2.0V.
0 = VDD voltage < 2.0V

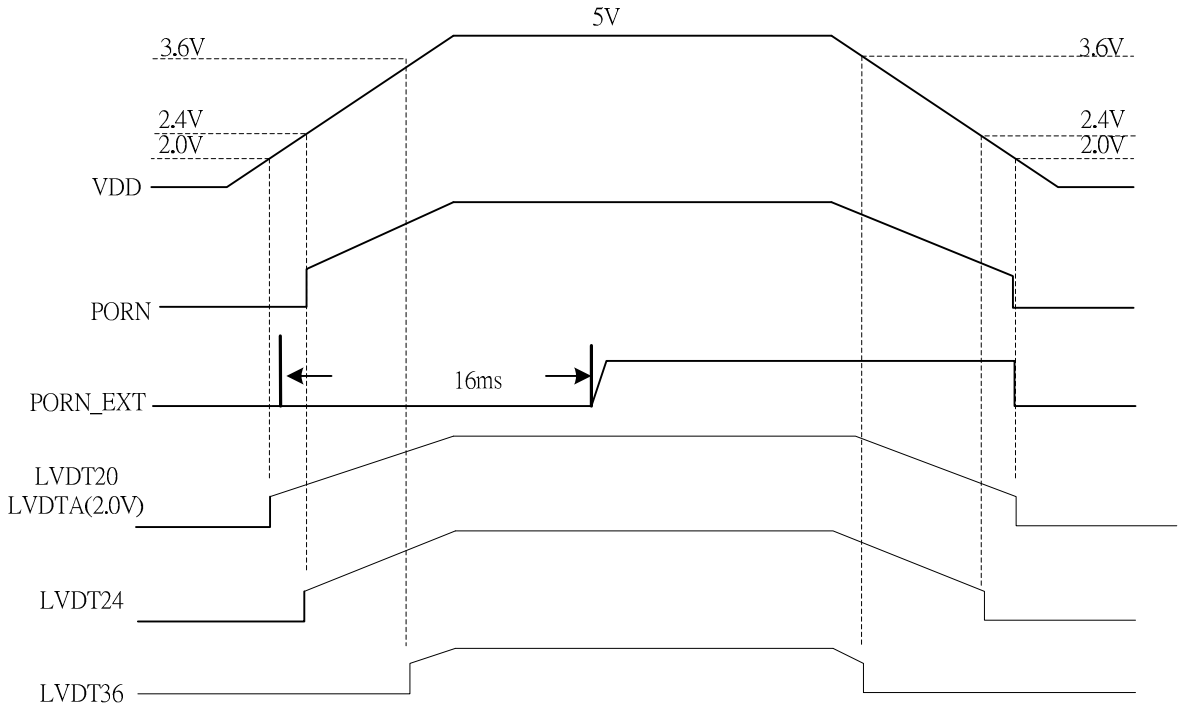


Figure 3.0-1 Power on Reset and LVDT20, LVDTA(2.0V), LVDT24, LVDT36 Timing

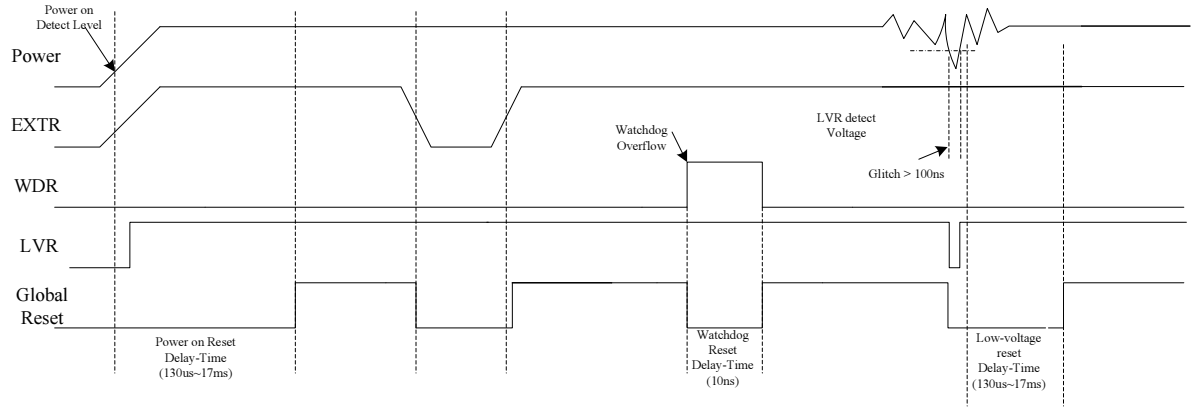


Figure 3.0-2 Global Timing

【4】Clock Control

The MCU operation frequency rang is as following: (Fcpu is MCU clock)
(1) VDD > 2.0 V → Fcpu ≦ 16Mhz

(Note: When MCU is Power on, the Fcpu is set 1/2/4/8 Mhz by configuration selection.
When MCU is after power on reset, the Fcpu can be switch to 16Mhz by program.)

Address 13H: Clock configuration (CLKCFG)

Bits	7	6	5	4	3	2	1	0
Name	SELCLK[2:0]			CLKSW	SIRCEN	INCODS	EXOSEN	IRCEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	0	1

Bit[7:5] : SELCLK[2:0]
Select MCU switch-clock. (FIRC=16Mhz)

SELCLK[2:0]	Select clock(Fsel)
3'b000	(FOSC or FIRC)/1
3'b001	(FOSC or FIRC)/2
3'b010	(FOSC or FIRC)/4
3'b011	(FOSC or FIRC)/8
3'b100	(FOSC or FIRC)/16
3'b101	FSIRC

Bit[4] : CLKSW
CPU clock switch signal
1 = CPU clock start to switch from Ffig clock to Fsel clock.
0 = CPU clock start to switch from Fsel clock to Ffig clock.

Note: If ATSW bit is '1', and LVDTA bit is '0', the CPU clock will be forced to Ffig.

Bit[3] : SIRCEN
Slow IRC Enable
1 = Enable SIRC.
0 = Disable SIRC.

Bit[2] : INCODS
Internal clock output disable.
1 = Disable internal IRC clock output.
0 = Enable internal IRC clock output. The IRC clock is driven output to XOUT pin.

Bit[1] : EXOSEN
External Oscillator Enable.
1 = Enable the external oscillator. The Fcpu clock is switch to external clock(Fosc) from FIRC clock.
0 = Disable Oscillator Enable.

Bit[0] : IRCEN
Internal clock enable.
1 = Enable internal clock
0 = Disable internal clock.

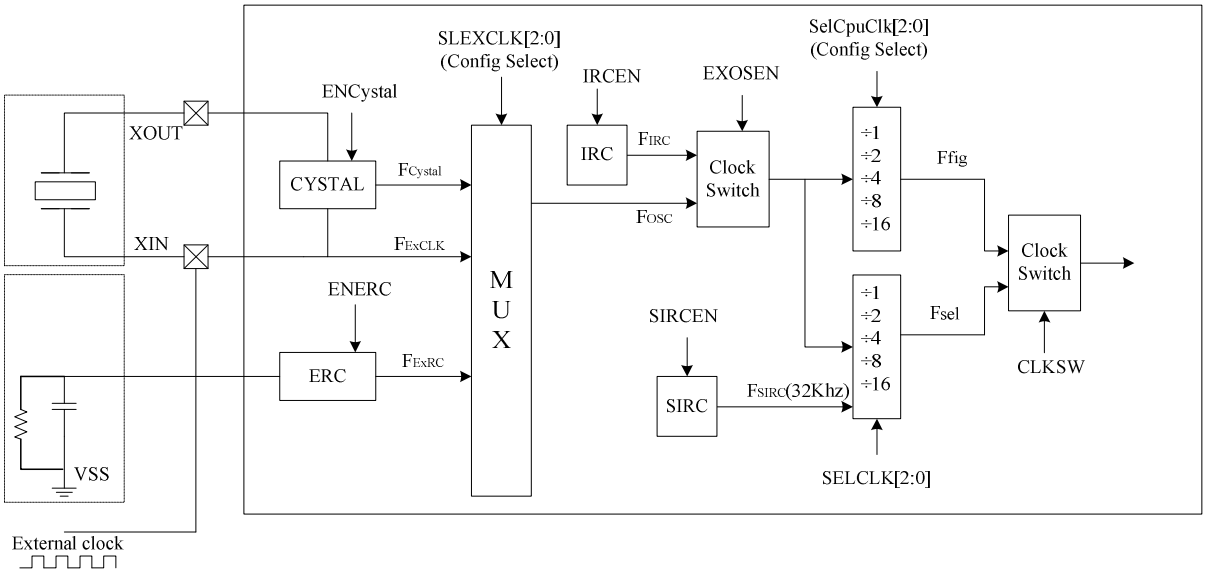
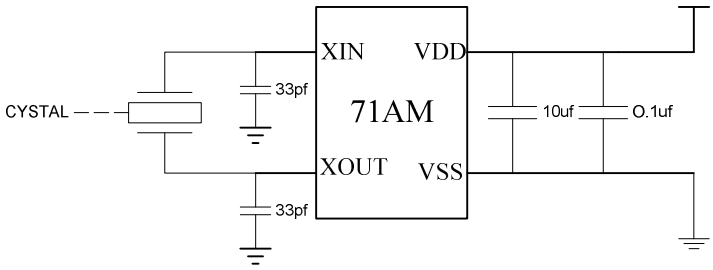


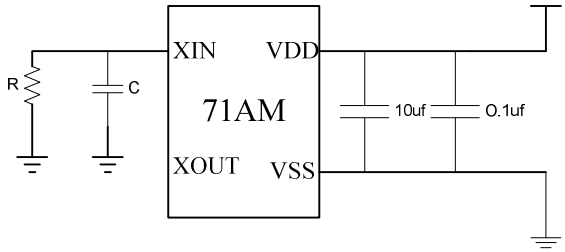
Figure 4.0-1 Clock Switch Block diagram

4.1 Crystal/RC/OSC connect

- Crystal (High/Low frequency)



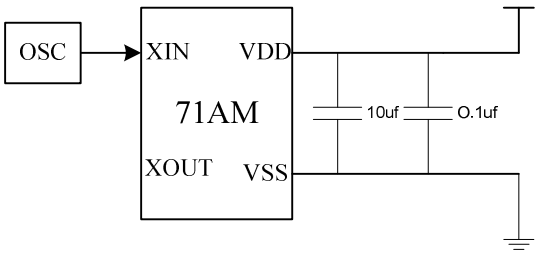
- **RC**



T = 90ns + (0.65 * R * C) ns

T 爲時間 , R 爲電阻 , C 爲電容 , R 需大於 2K

- **External clock**



Note: (1) ENCystal = (SLEXCLK[1:0] == 2'b00)&EXOSEN
(2) ENERC = (SLEXCLK[1:0] == 2'b01)&EXOSEN

Example: Clock Switch demo code (MCU clock is 1Mhz when selCpuClk == 3'b111)
Switch MCU clock from Ffig to Fsel, and then need return to default clock and then switch to **32**Khz

```
BCR     CLKCFG , SELCLK2_B
BSR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B
                                    //  Select clock is     Fsel  (FIRC/8)
BSR     CLKCFG,CLKSW                //  Fcpu is switch to Fsel

            .
            .
BCR     CLKCFG, CLKSW               //   Fcpu switch to Ffig.
BSR     CLKCFG , SELCLK2_B
BCR     CLKCFG , SELCLK1_B
BSR     CLKCFG , SELCLK0_B          //  Select clock is   Fsel  (FSIRC)

BSR     CLKCFG,CLKSW                //   Fcpu is switch to  FSIRC 32KHz(Now Fcpu = 32Khz)
```

【5】System Operating Mode

5.1 Overview

The FM8PC71AM support a versatile low-power operation mode as bellows:

(1) Normal Mode.
(2) Slow Mode.
(3) Green Mode.
(4) Suspend Mode

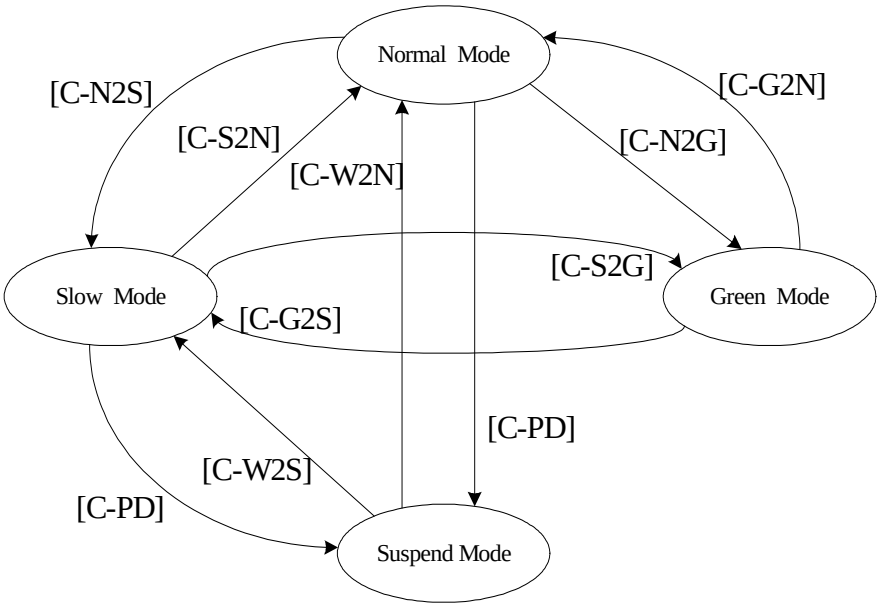


Figure 5.1-1 System Switch Mode Block diagram

Condition Description for System switch mode :

[C-PD] : Normal mode or Slow mode into Power down condition.

Example:

```
Sleep                    // Sleep instruction
NOP
NOP
```

[C-W2N] : Suspend mode wakeup to Normal mode condition.
(1) **PA,PB** wakeup interrupt.
(2) External Reset occurs.

Note : If system is from Normal mode to suspend mode, the system will be from suspend mode to normal mode when wakeup interrupt occurs.

[C-W2S] : Suspend mode wakeup to Slow mode condition.
(1) **PA,PB** wakeup interrupt.
(2) External Reset occurs.

Note : If system is from Slow mode to suspend mode, the system will be from suspend mode to Slow mode when wakeup interrupt occurs.

[C-N2S] : Normal mode into Slow mode condition.
First, the firmware needs to switch CPU clock, the CPU clock will be from FIRC/FOSC to FSIRC.
Next, set LVDIS (Reg.12h.5) bit to 1

Example code:

```
BSR    CLKCFG, SELCLK2_B          // set Fsel = FSIRC (SELCLK=3'b101)
BCR    CLKCFG, SELCLK1_B
BSR    CLKCFG, SELCLK0_B
BSR    CLKCFG, CLKSW_B            // switch CPU clock
NOP

BSR    PCON, LVDIS_B
```

[C-S2N] : Slow mode into normal mode condition.
When the firmware switches CPU clock from FSIRC to FIRC/FOSC and sets LVDIS (Reg.12h.5) bit to 0.

Example code:

```
BCR    PCON, LVDIS_B
BCR    CLKCFG, CLKSW_B            // switch CPU clock
```

[C-N2G] : Normal mode into Green mode condition.
Green mode is sort into two types. Their difference is one disables all LVD36, LVD24, LVD20 and internal high IRC, and another not.

Example code for enabling all low voltage detect and internal high IRC:

```
BSR    PCON,GREEN_MD_B        //set GREEN_MD bit to 1
NOP
NOP
```

Example code for disabling all low voltage detect and internal high IRC :

```
MOVIA   0b01100000            //set GREEN_MD and LVDIS bit to 1 at the same time
MOVAR   PCON
NOP
NOP
```

[C-G2N] : Green mode into normal mode condition.
(1) PA,PB wakeup interrupt.
(2) external Reset occurs.
(3) WDT time out wakeup. (PC=0000h or PC=PC+1)
(4) PWM timers time out interrupt **using T0CK/T1CK**.

[C-S2G] : Slow mode into Green mode condition.
Slow mode only can be changed into the Green mode that disable all low voltage detect, because Slow mode always disable low voltage detect. Set GREEN_MD (Reg.12h.6) bit to 1 and enter Green mode.

Example:

```
BSR    PCON, GREEN_MD_B
NOP
NOP
```

[C-G2S] : Green mode into Slow mode condition.
(1) PA,PB wakeup interrupt.
(2) LVR or external Reset occurs.
(3) WDT time out wakeup. (PC=0000h or PC=PC+1)
(4) PWM timers time out interrupt **using T0CK/T1CK**.

Note : If system is from Slow mode to Green mode, the system will be from Green mode to Slow mode when wakeup interrupt occurs.

Operating Mode Description

MODE / Module	Normal Mode	Slow Mode	Green Mode	Suspend Mode (Power down Mode)
FOSC	Running (EXOSEN =1)	Disable or enable (by EXOSEN)	Disable (EXOSEN = 0 or 1)	Disable (EXOSEN = 0 or 1)
FIRC	Running (IRCEN = 1)	**Disable**	Disable	Disable
FSIRC	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Running (SIRCEN = 1)	Disable (SIRCEN = **1**)
WDT	Running **(WDTE = 1)**	Running **(WDTE = 1)**	Running **(WDTE = 1)**	Disable
Internal Interrupt	All enable	All enable	All enable	All enable
External Interrupt	All enable	All enable	All enable	All enable
Wakeup even	--	--	**PA,PB** interrupt Timer, WDT time output, Reset	**PA,PB** interrupt Reset
Sleep instruction	non	non	non	Run
{Green,LVDIS} (In Reg-12h)	2'b00	2'b01	2'b10,2'b11	2'bxx
PC of MCU	Work	Work	Stop	Stop
Clock of MCU	FOSC or FIRC	FSIRC	Non clock	Non clock

【6】PWM Description

6.0 PWM/Buzzer Overview

The PWM0 modules is pulse modulator combined with 12-bit generator. The FM8PC71AM supports two channels PWM0(PA[3])/PWM1 output. The PWM output timing is as follow Figure 8-1.

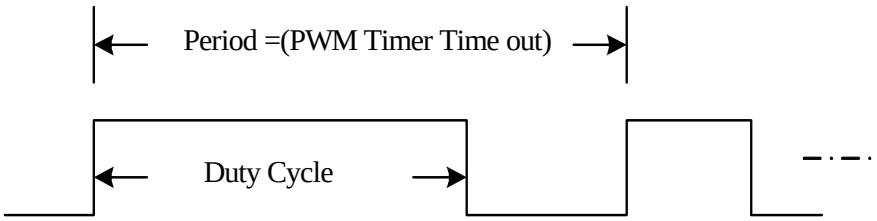


Figure 6-1 PWM Timing

Duty cycle is define by as following:

Duty Cycle = ((TMRLD) == PWM counter);

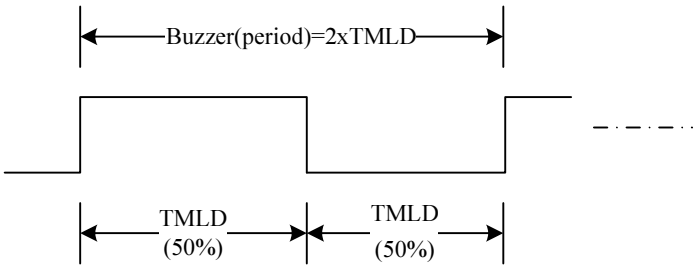


Figure 6-2 Buzzer Timing

Buzzer(Period) = 2 X((TMLD+1)== PWM counter)

Period calibrated :

(A) As **PWM mode** : (PWMXEN=1,PXTMEN=1, **BZX=0**):

Period = (PWM counter == $2^{Timer-bits}$) * (Tp0ck)

Example : P0DT[2:0] = 3'b000 (select 8-bit counter) ,
P0CKS[2:0] = 3'b001 (Fp0ck /2)
P0TPS[2:0] = 3'b001(Fp0ck = FIRC)
Period = 2^8 * 2 * 1/ FIRC = 256 * 2 * 62.5ns = 32 us

(B) As **Timer mode** : (PWMXEN=0,PXTMEN=1, **BZX=0**):

Period = (PWM counter == **(**TMRLD**+1)**) * (Tp0ck)

Example : Fcpu = 1MHz
P0DT[2:0] = 3'b101 (select 10-bit counter) ,
P0TPS[2:0] = 3'b000 (Fp0ck)
P0CKS[2:0] = 3'b000 (Fp0ck = Fcpu) and TMRLD= 3E**7** h

Timer Time out = **(**3E**7+1)** * 1/ Fp0ck = 1000 * 1/ Fcpu = 1000 * 1us = 1ms

(C) As Buzzer mode: (PWMXEN=0, PXTMEN=1, **BZX=1**)

Period = 2*(PWM counter == (TMRLD+1)) * (Tp0ck)

Example: Fcpu = 1MHz
P0DT[2:0] = 3'b101 (select 10-bit counter) ,
P0TPS[2:0] = 3'b000 (Fp0ck)
P0CKS[2:0] = 3'b000 (Fp0ck = Fcpu) and TMRLD= 3E7 h

Buzzer period = 2* (3E7+1) * 1/ Fp0ck = 2* 1000 * 1/ Fcpu = 2000 * 1us = 2ms (0.5KHz)

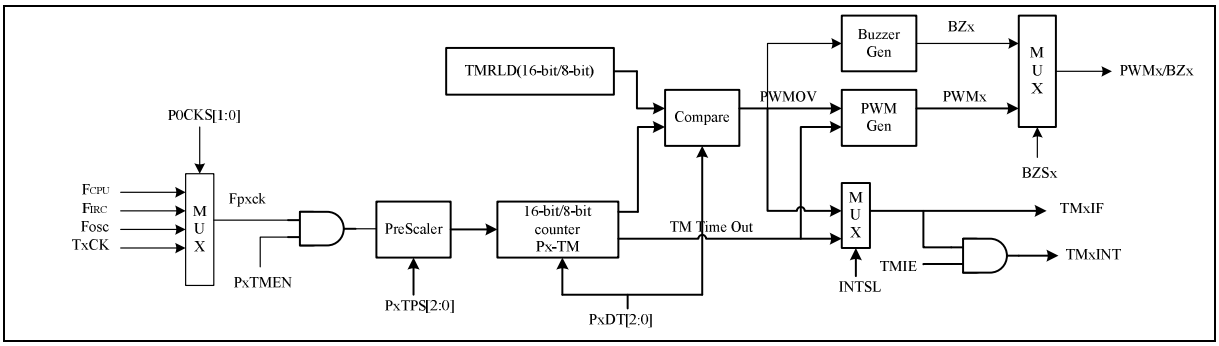


Figure 6-3 PWM Block diagram

6.1 PWM0 Register

Address 14H: PWM0 configuration Register(PWM0CON)

Bits	7	6	5	4	3	2	1	0
Name	P0INTSL	P0DT[2:0]			P0CKS[2:0]			--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P0INTSL

PWM0 interrupt selection.
1 = Select interrupt for PWM0 overflow.
0 = Select interrupt for PWM0 timer time out.

Bit[6:4] :P0DT[2:0]

PWM0 Duty Range.

P0DT [2:0],	PWM0 Duty Range		PWM0 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-3 PWM0 Duty Range

Bit[3:1] : P0CKS

PWM0 Timer clock select.

P0CKS[2:0]	Clock select (Fp0ck)
3'b000	FCPU/(N0+1)
3'b001	FIRC (16Mhz)/(N0+1)
3'b010	FOSC/(N0+1)
3'b011	T0CK/(N0+1)
3'b100	T1CK/(N0+1)
3'b101	PA[3] drive Low PA[4] drive Low
3'b110	PA[3] duty drive High base on Fp0ck = FIRC/N0 PA[4] duty drive Low base on Fp0ck = FIRC/N0
3'b111	PA[3] drive High PA[4] drive High

Note : N0 Rang 0~255

Address 15H: PWM0 Control Register (PWM0CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM0EN	P0OUTS	P0TPS[2:0]			P0TMEN	P0TMIE	P0TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM0EN

PWM0 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P0OUTS

PWM0 Duty Cycle pulse output select.
1 = PWM0 Duty Cycle pulse output is low.
0 = PWM0 Duty Cycle pulse output is high.

Bit[5:3] : P0TPS[2:0]

PWM0 Timer prescaler, as follow Table 8-4:

P0TPS [2:0]	PWM0 MODE (Fp0ck)
3'b000	PWM0 Timer clock select is Fp0ck
3'b001	PWM0 Timer clock select is Fp0ck /2
3'b010	PWM0 Timer clock select is Fp0ck /4
3'b011	PWM0 Timer clock select is Fp0ck /8
3'b100	PWM0 Timer clock select is Fp0ck /16
3'b101	PWM0 Timer clock select is Fp0ck /32
3'b110	PWM0 Timer clock select is Fp0ck /64
3'b111	PWM0 Timer clock select is Fp0ck /128

Table 8-4 PWM0 Timer clock select

Bit[2] : P0TMEN

PWM0 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P0TMIE

PWM0 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P0TMIF

PWM0 Timer overflow flag bit.
1 = PWM0 Timer overflow has occurred, write 0 clear flag.
0 = PWM0 Timer overflow has not occurred yet.

Address 16H: PWM0 Timer Low byte value Register (P0TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM[7:0]/							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0
Name	N0[7:0]							
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Bit[7:0] : P0TM[7:0]
PWM0 Timer Low byte read Only

Bit[7:0] : N0[7:0]
Divider parameter by (N0+1) for Fcpu/Firc/fosc write only, **read by IOSTR.**

Address 16H: PWM0 Timer Divider parameter Register (N0)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**N0[7:0]**							
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**

Read only by IOSTR instruction

Bit[7:0] : N0[7:0]
Divider parameter by (N0+1) for Fcpu/Firc/fosc Read only

Address 17H: PWM0 Timer compared or overflow reload Low byte value Register (P0RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P0TRD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TRD**[7:0]**
PWM0 Timer compared or overflow reload Low byte

Address 18H: PWM0 Timer and Reload High-nibble bits Register(P0TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P0TM [11:8]				P0TRD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P0TM[11:8]
PWM0 Timer high-nibble bits

Bit[3:0] : P0TRD **[11:8]**
PWM0 Timer compared or overflow reload high-nibble bits.

6.2 PWM1 Registers

Address 19H: PWM1 configuration Register(PWM1CON)

Bits	7	6	5	4	3	2	1	0
Name	P1INTSL	P1DT[2:0]			P1CKS[2:0]			--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P1INTSL

PWM1 interrupt selection.
1 = Select interrupt for PWM1 overflow.
0 = Select interrupt for PWM1 timer time out.

Bit[6:4] :P0DT[2:0]

PWM1 Duty Range.

P1DT [2:0],	PWM1 Duty Range		PWM1 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-3 PWM1 Duty Range

Bit[3:1] : P1CKS[2:0]

PWM1 Timer clock select.

P1CKS[2:0]	Clock select (Fp1ck)
3'b000	FCPU
3'b001	FIRC (16Mhz)
3'b010	FOSC
3'b011	T0CK
3'b100	T1CK

Address 1AH: PWM1 Control Register (PWM1CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM1EN	P1OUTS	P1TPS[2:0]			P1TMEN	P1TMIE	P1TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM1EN

PWM1 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P1OUTS

PWM1 Duty Cycle pulse output select.
1 = PWM1 Duty Cycle pulse output is low.
0 = PWM1 Duty Cycle pulse output is high.

Bit[5:3] : P1TPS[2:0]

PWM1 Timer prescaler, as follow Table 6-5:

P1TPS [2:0]	PWM1 MODE
3'b000	PWM1 Timer clock select is Fp1ck
3'b001	PWM1 Timer clock select is Fp1ck /2
3'b010	PWM1 Timer clock select is Fp1ck /4
3'b011	PWM1 Timer clock select is Fp1ck /8
3'b100	PWM1 Timer clock select is Fp1ck /16
3'b101	PWM1 Timer clock select is Fp1ck /32
3'b110	PWM1 Timer clock select is Fp1ck /64
3'b111	PWM1 Timer clock select is Fp1ck /128

Table 6-4 PWM1 Timer clock select

Bit[2] : P1TMEN

PWM1 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P1TMIE

PWM1 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P1TMIF

PWM1 Timer overflow flag bit.
1 = PWM1 Timer overflow has occurred, write 0 clear flag.
0 = PWM1 Timer overflow has not occurred yet.

Address 1BH: PWM1 Timer Low byte value Register (P1TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P0TM[7:0]

PWM1 Timer Low byte

Address 1CH: PWM1 Timer compared or overflow reload Low byte value Register (P1RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P1TRD [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P1TRD **[7:0]**
PWM1 Timer compared or overflow reload Low byte

Address 1DH: PWM1 Timer and High-nibble bits Register(P1TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P1TM [11:8]				P1TRD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P1TM[11:8]
PWM1 Timer high-nibble bits

Bit[3:0] : P1TRD **[11:8]**
PWM1 Timer compared or overflow reload high-nibble bits.

6.3 PWM2 Registers

Address 1EH: PWM2 configuration Register(PWM2CON)

Bits	7	6	5	4	3	2	1	0
Name	P2INTSL	P2DT[2:0]			P2CKS[1:0]			--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P2INTSL

PWM2 interrupt selection.
1 = Select interrupt for PWM2 overflow.
0 = Select interrupt for PWM2 timer time out.

Bit[6:4] :P2DT[2:0]

PWM2 Duty Range.

P2DT[[2:0],	PWM2 Duty Range		PWM2 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-5 PWM2 Duty Range

Bit[3:1] : P2CKS[2:0]

PWM2 Timer clock select.

P2CKS[2:0]	Clock select (Fp2ck)
3'b000	FCPU/(N2+1)
3'b001	FIRC (16Mhz)/(N2+1)
3'b010	FOSC/(N2+1)
3'b011	T0CK/(N2+1)
3'b100	T1CK/(N2+1)
3'b101	PA[6] drive Low PA[5] drive Low
3'b110	PA[6] duty drive High base on Fp2ck = FIRC/(N2+1) PA[5] duty drive Low base on Fp2ck = FIRC/(N2+1)
3'b111	PA[6] drive High PA[5] drive High

Address 1FH: PWM2 Control Register (PWM2CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM2EN	P2OUTS	P2TPS[2:0]			P2TMEN	P2TMIE	P2TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM2EN

PWM1 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P2OUTS

PWM1 Duty Cycle pulse output select.
1 = PWM2 Duty Cycle pulse output is low.
0 = PWM2 Duty Cycle pulse output is high.

Bit[5:3] : P2TPS[2:0]

PWM2 Timer prescaler, as follow Table 6-5:

P2TPS [2:0]	PWM1 MODE
3'b000	PWM2 Timer clock select is Fp2ck
3'b001	PWM2 Timer clock select is Fp2ck /2
3'b010	PWM2 Timer clock select is Fp2ck /4
3'b011	PWM2 Timer clock select is Fp2ck /8
3'b100	PWM2 Timer clock select is Fp2ck /16
3'b101	PWM2 Timer clock select is Fp2ck /32
3'b110	PWM2 Timer clock select is Fp2ck /64
3'b111	PWM2 Timer clock select is Fp2ck /128

Table 6-6 PWM2 Timer clock select

Bit[2] : P2TMEN

PWM2 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P2TMIE

PWM1 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P2TMIF

PWM1 Timer overflow flag bit.
1 = PWM1 Timer overflow has occurred, write 0 clear flag.
0 = PWM1 Timer overflow has not occurred yet.

Address 20H: PWM2 Timer Low byte value Register (P2TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P2TM[7:0]/							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0
Name	N2[7:0]							
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Bit[7:0] : P2TM[7:0]
PWM2 Timer Low byte read only
Bit[7:0] : N2[7:0]
Divider parameter by (N2+1) for Fcpu/Firc/fosc write only, **read by IOSTR.**

Address 20H: PWM2 Timer Divider parameter Register (N2)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**N2[7:0]**							
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**

Read only by IOSTR instruction

Bit[7:0] : N2[7:0]
Divider parameter by (N2+1) for Fcpu/Firc/fosc Read only

Address 21H: PWM2 Timer compared or overflow reload Low byte value Register (P2RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P2TRD [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P2TRD **[7:0]**
PWM2 Timer compared or overflow reload Low byte

Address 22H: PWM2 Timer and reload High-nibble bits Register(P2TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P2TM [11:8]				P2TRD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P2TM[11:8]
PWM2 Timer high-nibble bits

Bit[3:0] : P2TRD **[11:8]**
PWM2 Timer compared or overflow reload high-nibble bits.

6.3 PWM3 Registers

Address 23H: PWM3 configuration Register(PWM3CON)

Bits	7	6	5	4	3	2	1	0
Name	P3INTSL	P3DT[2:0]			P3CKS[1:0]			--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	0	0	0	0	0

Bit[7] : P3INTSL

PWM3 interrupt selection.
1 = Select interrupt for PWM3 overflow.
0 = Select interrupt for PWM3 timer time out.

Bit[6:4] :P3DT[2:0]

PWM3 Duty Range.

P1DT[2:0],	PWM3 Duty Range		PWM3 Timer bits
	High pulse	Low Pulse	
3'b000	1~15	15~1	4 bits
3'b001	1~31	31~1	5 bits
3'b010	1~63	63~1	6 bits
3'b011	1~255	255~1	8 bits
3'b100	1~511	511~1	9 bits
3'b101	1~1023	1023~1	10 bits
3'b110	1~2047	2047~1	11 bits
3'b111	1~4095	4095~1	12 bits

TABLE 6-7 PWM3 Duty Range

Bit[3:1] : P3CKS[2:0]

PWM3 Timer clock select.

P3CKS[2:0]	Clock select (Fp3ck)
3'b000	FCPU/(N3+1)
3'b001	FIRC/(N3+1) (16Mhz)
3'b010	FOSC/(N3+1)
3'b011	T0CK/(N3+1)
3'b100	T1CK/(N3+1)
3'b101	PA[7] drive Low PB[5] drive Low
3'b110	PA[7] duty drive High base on Fp3ck = FIRC/(N3+1) PB[5] duty drive Low base on Fp3ck = FIRC/(N3+1)
3'b111	PA[7] drive High PB[5] drive High

Address 24H: PWM3 Control Register (PWM3CR)

Bits	7	6	5	4	3	2	1	0
Name	PWM3EN	P3OUTS	P3CKSL[2:0]			P3TMEN	P3TMIE	P3TMIF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : PWM3EN

PWM3 module enable.
1 = PWM mode.
0 = Timer mode.

Bit[6] : P1OUTS

PWM3 Duty Cycle pulse output select.
1 = PWM3 Duty Cycle pulse output is low.
0 = PWM3 Duty Cycle pulse output is high.

Bit[5:3] : P3CLKS[2:0]

PWM3 Timer prescaler, as follow Table 6-5:

P1CKSL [2:0]	PWM1 MODE
3'b000	PWM3 Timer clock select is Fp3ck
3'b001	PWM3 Timer clock select is Fp3ck /2
3'b010	PWM3 Timer clock select is Fp3ck /4
3'b011	PWM3 Timer clock select is Fp3ck /8
3'b100	PWM3 Timer clock select is Fp3ck /16
3'b101	PWM3 Timer clock select is Fp3ck /32
3'b110	PWM3 Timer clock select is Fp3ck /64
3'b111	PWM3 Timer clock select is Fp3ck /128

Table 6-4 PWM0 Timer clock select

Bit[2] : P3TMEN

PWM3 Timer enable bit.
1 = Enable.
0 = Disable.

Bit[1] : P3TMIE

PWM3 Timer overflow interrupt bit.
1 = Enable interrupt.
0 = Disable interrupt.

Bit[0] : P3TMIF

PWM3 Timer overflow flag bit.
1 = PWM3 Timer overflow has occurred, write 0 clear flag.
0 = PWM3 Timer overflow has not occurred yet.

Address 25H: PWM3Timer Low byte value Register (P3TMLB)

Bits	7	6	5	4	3	2	1	0
Name	P3TM[7:0]/							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0
Name	N3[7:0]							
Default	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Bit[7:0] : P3TM[7:0]
PWM3 Timer Low byte read only

Bit[7:0] :N3[7:0]
Divider parameter by (N3+1) for Fcpu/Firc/fosc write only, **read by IOSTR.**

Address 25H: PWM3 Timer Divider parameter Register (N3)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	**N3[7:0]**							
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**

Read only by IOSTR instruction

Bit[7:0] : N3[7:0]
Divider parameter by (N3+1) for Fcpu/Firc/fosc Read only

Address 26H: PWM3 Timer compared or overflow reload Low byte value Register (P3RDLB)

Bits	7	6	5	4	3	2	1	0
Name	P3TRD [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : P3TRD **[7:0]**
PWM3 Timer compared or overflow reload Low byte

Address 27H: PWM3 Timer and reload High-nibble bits Register(P3TRHB)

Bits	7	6	5	4	3	2	1	0
Name	P3TM [11:8]				P3TRD [11:8]			
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:4] : P3TM[11:8]
PWM3 Timer high-nibble bits

Bit[3:0] : P3TRD **[11:8]**
PWM3 Timer compared or overflow reload high-nibble bits.

6.4 PWM Code Example

```
// pwm clock source F0ck = Fcpu(4MHz)
        BCR     PWM0CON,P0CKS2_B
        BCR     PWM0CON,P0CKS1_B
        BCR     PWM0CON,P0CKS0_B
 // pwm clock source F0ck/32 Hz
        BSR     PWM0CR,P0TPS2_B             // F0ck  =  4/32  Mhz  =  125 Khz  ;
        BCR     PWM0CR,P0TPS1_B
        BSR     PWM0CR,P0TPS0_B
```

(A) 4~8-bits PWM

```
 // pwm duty range   6bits( Rang  0~63)
        BCR     PWM0CON,P0DT2_B
        BSR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B

        MOVIA   00fh                    //  Load initial value 7~0 bits
        MOVAR   P0RDLB                  //  Duty Cycle  =  15  (1/F0ck)  clock s

// enable pwm
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B                ;  First Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

(B) 9~12-bits PWM

```
 // pwm duty range   12bits( Rang  0~4095)
        BSR     PWM0CON,P0DT2_B
        BSR     PWM0CON,P0DT1_B
        BSR     PWM0CON,P0DT0_B

        MOVIA   00fh                    //  Load initial value Low byte 7~0 bits
        MOVAR   P0RDLB                  //
        MOVIA   00h                     //  Load initial value High byte 11~8 bits
        MOVAR   P0RDHB                  //  Duty Cycle  =  15  (1/F0ck)  clock s

  // enable pwm
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B                ;  First Set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B
```

(C)4bits PWM chage to 9bits PWM

```
// pwm period= 4bits (Range 0~15)
        BCR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B

       MOVIA    00fh                  //  Set low byte initial value
       MOVAR   P0RDLB                 //

  // pwm Enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B              //  First set PWM0EN_B
        BSR     PWM0CR, P0TMEN_B


// pwm 9 bits Rang
        MOVIA    00fh                  //   Set low byte  initial value
        MOVAR    P0RDLB                ;
        MOVIA    00h                   //    Set High  byte  initial value
        MOVAR    P0RDHB

        BSR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B
```

(D) 9bits PWM updated reload value

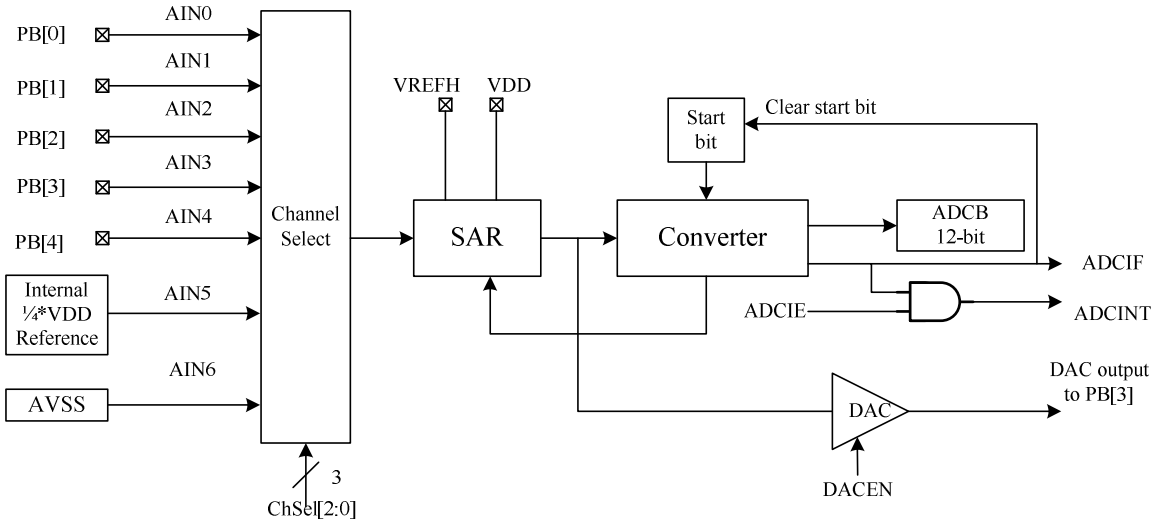
```
// pwm  duty range (Range 0~511)
        BSR     PWM0CON,P0DT2_B
        BCR     PWM0CON,P0DT1_B
        BCR     PWM0CON,P0DT0_B
      // Load   reload value
       MOVIA    007h                  //  Set low byte  initial value
        MOVAR   P0RDLB                ;
        MOVIA    00h                   ;// Set High  byte  initial value
        MOVAR   P0RDHB


  // pwm Enable
        BSR     PWM0CR,P0TMIE_B
        BSR     PWM0CR, PWM0EN_B              //First  Set  PWM0EN_B
        BSR     PWM0CR, P0TMEN_B


 //Updated reload value
        MOVIA    02Ch                  //   Set low byte  initial value
        MOVAR    P0RDLB                ;
        MOVIA    001h                  //  Set High  byte  initial value
```

【7】5+2 Channel Analog to Digital (ADC)

Build In ADC module supports 7 channel(PB[0]~PB[3],PA[0],PA[1],PA[3]) and one internal channel ¼ VDD reference that can be use for auxiliary input and battery monitor. The ADC module converts an input voltage to a 12-bit digital code.



7.1 ADC Registers

Address 28H: ADC Control_1 Register(ADCON1)

Bits	7	6	5	4	3	2	1	0
Name	ADCEN	ADCST	CHSEL[2:0]			Revered	ADCSR[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCEN

ADC module enable bit.
1 = Enable ADC.
0 = Disable ADC.

Bit[6] : ADCST

1 = Start to ADC sample, when ADC conversion has been completed, this start be clear to 0 by H/W.
0 = Stop.

Bit[5:2] : CHSEL[2:0]

ADC input channel select bit, as follows Table9-1

CHSEL[2:0]	Input Channel
3'b000	PB[0] (AIN0)
3'b001	PB[1] (AIN1)
3'b010	PB[2] (AIN2)
3'b011	PB[3] (AIN3)
3'b100	PB[4] (AIN4)
3'b101	Internal VDD/4 (AIN5)
3'b110	Internal AVSS (AIN6)
3'b111	Revered

Table 9-1 ADC input channel select

Bit[2] : Revered

Bit[1:0] : ADCSR[1:0]

ADC clock selection.(Fadc ≦ 2Mhz)
2'b00 : ADC clock is Fcpu/8.
2'b01 : ADC clock is Fcpu/4.
2'b10 : ADC clock is Fcpu/2.
2'b11 : ADC clock is Fcpu.

Address 29H: ADC Control_2 Register(ADCON2)

Bits	7	6	5	4	3	2	1	0
Name	ADCIE	ADCIF	SVREFH	ADCNT	DACEN	ADCTMS	SELVER[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : ADCIE

ADC interrupt Enable bit .
1 = Enable.
0 = Disable.

Bit[6] : ADCIF

ADC conversion has been completed interrupt flag.
1 = ADC conversion has been completed, write 0 clear flag.
0 = ADC conversion has been not completed yet.

Bit[5] : SVREFH

Select VREFH from external or internal voltage.
1 = External voltage(VREFH == PB[4] pin) base on bit[3].
0 = Internal voltage(VREFH == Internal reference voltage Table9-2).

Bit[4] : ADCNT

ADC sample mode.
1 = ADC continues mode.
0 = Trigger mode base on ADCST bit.

Bit[3] : DACEN

DAC output enable (and Reg-29h ADCTest=1).
1 = Enable DAC output to PB[3]
0 = Disable DAC output.

Bit[2] : ADCTMS

ADC convert Timing.
1 = Fixed convert timing.
0 = Non-Fixed convert timing.

Bit[1:0] : SELVER[1:0]

ADC internal VERFH voltage selection.

SELVER[1:0]	VREFH
2'b00	VDD
2'b01	4V
2'b10	3V
2'b11	2V

Table 9-2 ADC internal VERFH voltage selection

Address 28H: ADCControl-3 Register (ADCON3)

Bits	7	6	5	4	3	2	1	0
Name	ADCTEST	--	--	--	--	--		
Read/Write	R/W	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Accessed by IOST/IOSTR instruction

Bit[7] : ADCTEST
1 : ADC Disable and Enable DAC output PB[3] When DACOEN bit is set 1.
0 : ADC enable

Address 30H: ADC High byte Register(ADCHB/DACR1LB)

Bits	7	6	5	4	3	2	1	0
Name	ADCB[11:4]/ DACR1[7:0]							
Read/Write	R/W							
Default	0	0	0	0	0	0	0	0

Bit[7:0] :

	Bit[7:0]
ADCEN=1 DACEN=0 ADCTEST=0	ADCB[11:4] is high byte of ADC Read only
ADCEN=1 DACEN=1 ADCTEST=1	DACR1 [7:0] is Low byte of DAC Write only

Address 31H: ADC Low byte Register (ADCLB/DACR1HB)

Bits	7~4	3~0
Name	Revered	ADCB[3:0]/ DACR1[11:8]
Read/Write	--	R/W
Default	0	0

Bit[3:0] :

	Bit[3:0]
ADCEN=1 DACEN=0 ADCTEST=0	ADCB[3:0] is high byte of ADC Read only
ADCEN=1 DACEN=1 ADCTEST=1	DACR1 [11:8] is High byte of DAC Write only

【8】Enhance Function of 71AM

8.1 Address 32~34H: General purpose Register (GPR)

Bits	7	6	5	4	3	2	1	0
Name	General purpose Register							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

32h~34H is general purpose register for RAMBK=0/1

8.2 Address 35H: Enhance Functional Register-1(EFR1)

Bits	7	6	5	4	3	2	1	0
Name	ROMBK	RAMBK	FRP	SPSEL	BZ3	BZ2	BZ1	BZ0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	0	0	0

Bit[7] : ROMBK

1: select Program ROM is Bank 1. (PC=0x800~0xFFF)
0: select Program ROM is Bank 0. (PC=0x000~0x7FF)

Bit[6] : RAMBK

1 = Select RAM bank-1
0 = Select RAM bank-0

Bit[5] : FRP

1: The other bit of GPIO updated from register (PA/PB register) for BSR/BCR instruction
0: The other bit of GPIO updated from PIN(GPIO) for BSR/BCR instruction.

Bit][4] : SPSEL

Slow IRC clock selection

1: Slow IRC Clock don't vary with VDD
0: Slow IRC Clock vary with VDD

Bit[3] : BZ3

Buzzer3 output select
1: select buzzer3 output to PA [7] (PWMEN3=0).
0: select PWM3 output to PA [7] (PWMEN3=1).

Bit[2 : BZ2

Buzzer2 output select
1: select buzzer2 output to PA [6] (PWMEN2=0).
0: select PWM2 output to PA [6] (PWMEN2=1).

Bit [1]: BZ1

Buzzer1 output select
1: select buzzer1output to PA [4] (PWMEN1=0).
0: select PWM1 output to PA [4] (PWMEN1=1).

Bit [0]: BZ0

Buzzer0 output select
1: select buzzer0 output to PA [3] (PWMEN0=0).
0: select PWM0 output to PA [3] (PWMEN0=1).

8.3 Address 36H: Enhance Functional Register-2(EFR2)

Bits	7	6	5	4	3	2	1	0
Name	ATSW	SIGN	LVDTA	SPB34EN	--	--	--	--
Read/Write	R/W	R/W	R	R/W	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit[7] : ATSW (ICE not support)

Automatic switch clock function control bit:
1 = Enable auto clock switch Fcpu to Ffig clock when VDD < 2V (LVDTA bit is '0').
0 = Disable auto clock switch, the CPU clock source defined by CLKSW bit.

Bit[6] : SIGN

AS {CMPEN,Toggle[1] == 2'b11} enable auto increment/decrease of PWM3 Please refer Table 8-2.
1 => COP2 = **0** P3TMRLD= P3TMRLD -1; COP2=**1** P3TMRLD= P3TMRLD+1;
0 => COP2 = 1 P3TMRLD= P3TMRLD-1; COP2=0 P3TMRLD= P3TMRLD +1;

Bit[5] : LVDTA (ICE not support)

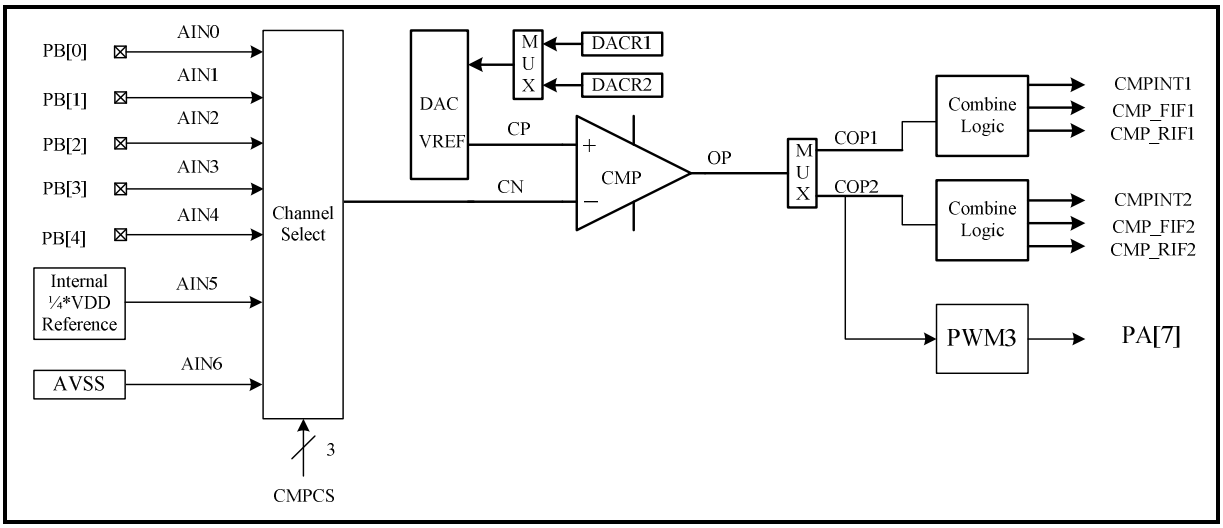
Low voltage detect status for Automatic Switch clock function
1: VDD >= 2.0V, if ATSW bit is '1', the CPU clock source defined by CLKSW bit.
0: VDD < 2.0V, if ATSW bit is '1', the CPU clock source is forced to Ffig.

Bit[4] : SPB34EN (ICE not support)

Short PB [3] and PB [4] pin enable
1: Short Enable
0: Short Disable

8.4 Voltage Comparator

The FM8PC71AM build in one Low-offset voltage comparator.
The comparator input/output are sharing with GPIO pin and the block diagram as follow:



Address 37H: Comparator control Register-1(CMPCON1)

Bits	7	6	5	4	3	2	1	0
Name	CMPEN	COP1	CMPIE1	CMPRIF1	CMPFIF1	CMPCS [2:0]		
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : CMPEN
Comparator enable/Disable.
1 = Enable.
0 = Disable.

Bit[6] : COP1
Comparator output signal of DACR1.
1 = CP > CN
0 = CP < CN

Bit[5] : CMPIE1
Comparator Interrupt enable bit.
1 = Enable Comparator Interrupt of DACR1.
0 = Disable Comparator Interrupt of DACR1

Bit[4] : CMPRIF1
CMPPIF is interrupt flag of DACR1, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR1 is raising (CP>CN).

Bit[3] : CMPFIF1
CMPFIF is interrupt flag of DACR1, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR1 is falling (CP<CN).

Bit[2:0] : CMPCS[2:0]

CMPCS [2:0]	Input Channel
3'b000	CN=PB [0] (AIN0)
3'b001	CN=PB [1] (AIN1)
3'b010	CN=PB [2] (AIN2)
3'b011	CN=PB [3] (AIN3)
3'b100	CN=PB [4] (AIN4)
3'b101	Internal CN=VDD/4 (AIN5)
3'b110	Internal CN=AVSS (AIN6)
3'b111	Revered

Table 8-1 CMP input channel select

Address 38H: Comparator control Register-2(CMPCON2)

Bits	7	6	5	4	3	2	1	0
Name	CMPINT1	COP2	CMPIE2	CMPRIF2	CMPFIF2	CMPINT2	TOGSEL [1:0]	
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : CMPINT1
1 = CMPINT1 Pin-Change to interrupt.
0 = CMPINT1 falling edge to interrupt.

Bit[6] : COP2
Comparator output signal of DACR2.
1 = CP > CN
0 = CP < CN

Bit[5] : CMPIE2
Comparator Interrupt of DACR2 enable bit.
1 = Enable Comparator Interrupt of DACR2.
0 = Disable Comparator Interrupt of DACR2

Bit[4] : CMPRIF2
CMPPIF2 is interrupt of DACR2 flag, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR2 is raising (CP>CN).

Bit[3] : CMPFIF2
CMPFIF2 is interrupt flag of DACR2, write 0 clear flag.
1 = Interrupt occurrence when Comparator output of DACR2 is falling (CP<CN).

Bit[2] : CMPINT2
1 = CMPINT2 Pin-Change to interrupt.
0 = CMPINT2 falling edge to interrupt.

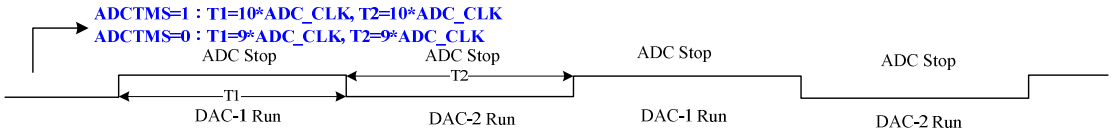
Bit[1:0] : TOGSEL[1:0]

ADC and CMP toggle operation selection. **(As Table 8-2)**

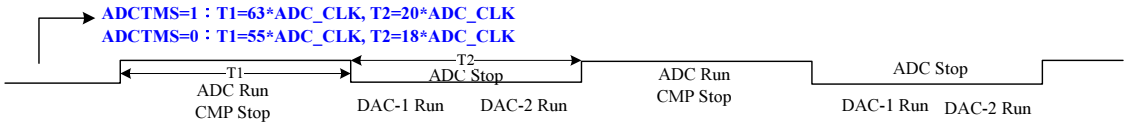
ADCEN	DACEN	ADCTEST	CMPEN	Toggle [1:0]	Functional Description
1	0	0	0	2'b00	ADC is real operation mode **TMD-0**
1	1	1	0	2'b00	DAC is real operation mode **TMD-1**
1	0	1	1	2'b00	The DAC-1(DACR1) and DAC-2(DACR2) is toggle operation mode **TMD-2**
1	0	1	1	2'b01	The ADC and DAC-1(DACR1) and DAC-2(DACR2) is toggle operation mode **TMD-3**
1	0	1	1	2'b10	The ADC and DAC-2(DACR2) with PWM3 module is toggle operation mode (SIGN =0 COP2 =1 P3TMRLD =P3TMRLD+1 COP2 =0 P3TMRLD =P3TMRLD-1, SIGN =1 COP2 =1 P3TMRLD =P3TMRLD-1 COP2 =**0** P3TMRLD =P3TMRLD+1) **TMD-4**
1	0	1	1	2'b11	The ADC and CMP DAC-1(DACR1) and DAC-2(DACR2) with PWM3 is toggle operation module (SIGN =0 COP2 = 1 P3TMRLD =P3TMRLD+1 COP2 =0 P3TMRLD =P3TMRLD-1, SIGN =1 COP2 =1 P3TMRLD =P3TMRLD-1 COP2 =0 P3TMRLD =P3TMRLD+1) **TMD-5**

The operation Mode **Table 8-2**

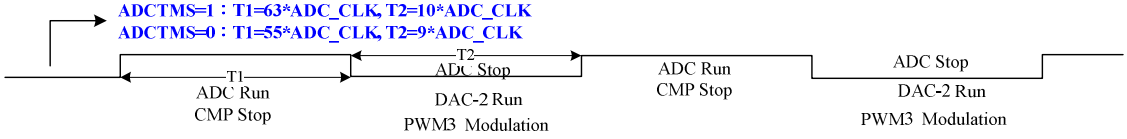
TMD-2



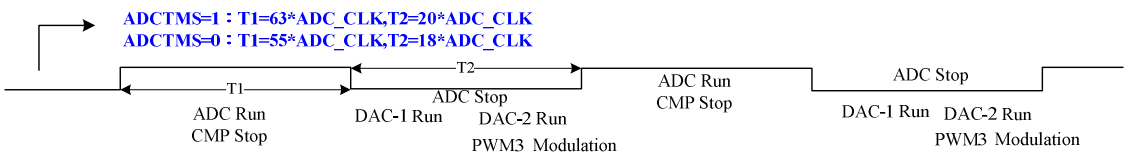
TMD-3



TMD-4



TMD-5



Address 39H: DAC Low Byte Register-2(DACR2LB)

Bits	7	6	5	4	3	2	1	0
Name	DACR2[7:0]							
Read/Write	R/W	R /W	R/W	R /W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : DACR2[7:0]

DACR2 Low byte data.

Address 3AH: DAC High byte Register-2(DACR2HB)

Bits	7~4	3~0
Name	Revered	DACR2[11:8]
Read/Write	--	R/W
Default	0	0

Bit[3:0] : DACR2[11:8]

DACR2 High Byte Data

8.5 Timer0

The Timer0 is an 8 bits Timer/Counter. The Timer0 can operate as either a timer or an interrupt event counter. The Timer0 block diagram is as show in Figure 2.6-1.

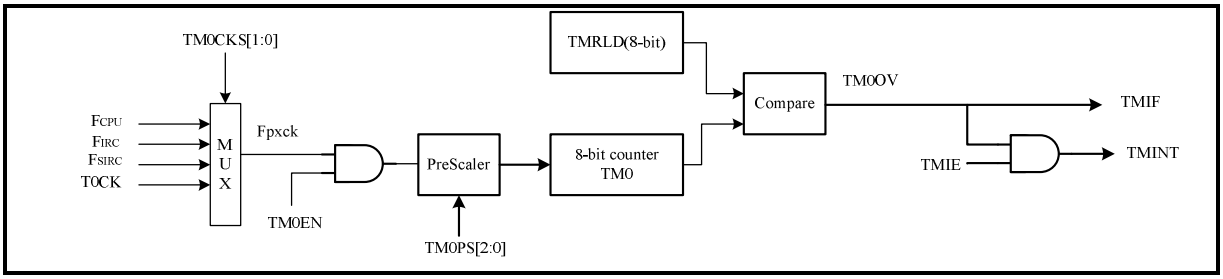


Figure 2.6-1 Block Diagram of Timer0

Address 0FH: TM0 Control Register (TM0CON)

Bits	7	6	5	4	3	2	1	0
Name	TM0EN	--	TM0PS[2:0]			TM0CKS[1:0]		--
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] :TM0EN
TM0 module enable.
1 = Enable.
0 = Disable.
Bit[6] : Revered
Bit[5:3] : TM0PS[2:0]
TM0 Timer prescaler, as follow Table 8-4:

TM0PS [2:0]	TM0 MODE
3'b000	TM0 Timer clock select is FT0ck /2
3'b001	TM0 Timer clock select is FT0ck /4
3'b010	TM0 Timer clock select is FT0ck /8
3'b011	TM0 Timer clock select is FT0ck /16
3'b100	TM0 Timer clock select is FT0ck /32
3'b101	TM0 Timer clock select is FT0ck /64
3'b110	TM0 Timer clock select is FT0ck /128
3'b111	TM0 Timer clock select is FT0ck /256

Table 8-4 TM0 Timer clock select
Bit[2:1] :TM0CKS[1:0]
TM0 Timer clock select.

TM0CKS[1:0]	Clock select (FT0ck)
2'b00	FCPU
2'b01	FIRC (16Mhz)
2'b10	Fsirc
2'b11	T0CK (External clock)

Address 0EH: Timer0 value Register (TM0)

Bits	7	6	5	4	3	2	1	0
Name	P0TM[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit[7:0] : TM0[7:0]
Timer 0 counter value.

Address 10H: Timer0 compared or overflow reload byte value Register (T0RLD)

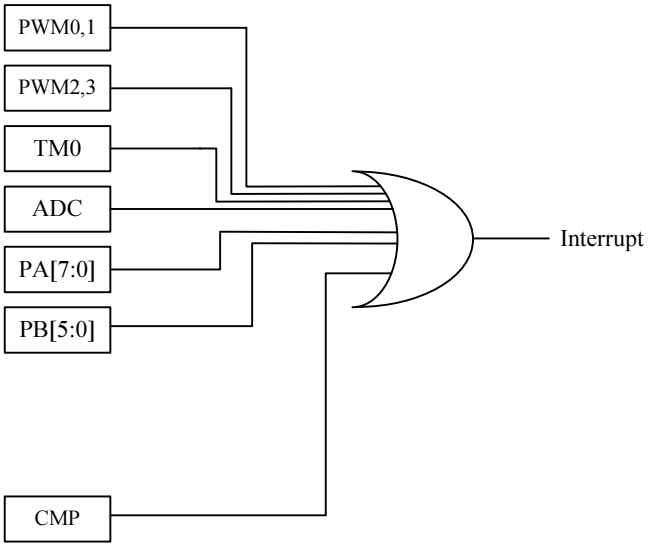
Bits	7	6	5	4	3	2	1	0
Name	T0RLD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit[7:0] : T0RLD[7:0]
Timer0 compared or overflow reload byte

【9】Interrupt

The FM8PC71AM has interrupt as following:
(1) PWM0 ,PWM1,PWM2 and PWM3 interrupt.
(2) TM0 Timer interrupt.
(3) PA[7:0] and PB[5:0] external interrupt.
(4) ADC sample completed interrupt.
(5) Raising and falling of CMP interrupt.

The FM8PC71AM reset vector is fixed at **0x0000h** and
the interrupt vector is at **0x0003h.**
A global interrupt enable bit, GIE(Reg.0Bh-7), enable(if set) all un-masked interrupts or disables(if cleared) all interrupts. Individual interrupts can be enable/disable through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.
The interrupt priority is decided by customer firmware control.



Interrupt Block Diagram

9.1 Interrupt Registers

Address 0BH: Interrupt Mask Register(INTEN)

Bits	7	6	5	4	3	2	1	0
Name	GIE	--	--	--	--	--	--	TM0IE
Read/Write	R/W	--	--	--	--	--	--	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] : GIE

Global Interrupt enable bit.
1 = Enable.
0 = Disable.

Bit[0] : TM0IE

Timer 0 Interrupt enable bit.
1 = Enable.
0 = Disable.

Address 0CH: Interrupt Flag Register(INTFLAG)

Bits	7	6	5	4	3	2	1	0
Name	PBIF	PAIF	--	--	--	--	--	TM0IF
Read/Write	R/W	R/W	--	--	--	--	--	R/W
Default	0	0	0	0	0	0	0	0

Bit[7] :PBIF

Port B interrupt flag, write 0 clear flag.
1 = Interrupt occurrence of PortB.

Bit[6] :PAIF

Port A interrupt flag, write 0 clear flag.
1 = Interrupt occurrence of PorA.

Bit[0] :TM0IF

Timer0 interrupt flag, write 0 clear flag.
1= Timer 0 Timer out and interrupt occurrence.

【10】Instruction Set

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	R, bit	Clear bit in R	0 → R<b>	1	-
BSR	R, bit	Set bit in R	1 → R<b>	1	-
BTRSC	R, bit	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2 (1)	-
BTRSS	R, bit	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2 (1)	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
RETURN		Return from subroutine	Top of Stack → PC	2	-
RETFIE		Return from interrupt, set GIE bit	Top of Stack → PC, 1 → GIE	2	-
CLRA		Clear ACC	00h → ACC	1	Z
IOST	R	Load R-plane register	ACC → R-plane register	1	-
IOSTR	R	Read R-plane register	R-plane register → ACC		
CLRR	R	Clear R	00h → R	1	Z
MOVAR	R	Move ACC to R	ACC → R	1	-
MOVR	R, d	Move R	R → dest	1	Z
DECR	R, d	Decrement R	R - 1 → dest	1	Z
DECRSZ	R, d	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2 (1)	-
INCR	R, d	Increment R	R + 1 → dest	1	Z
INCRSZ	R, d	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2 (1)	-
ADDAR	R, d	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	R, d	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ADCAR	R, d	Add ACC and R with carry	R + ACC + C → dest	1	C, DC, Z
SBCAR	R, d	Subtract ACC from R with Carry	R + $\overline{ACC}$ + C → dest	1	C, DC, Z
ANDAR	R, d	AND ACC with R	ACC and R → dest	1	Z
IORAR	R, d	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	R, d	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	R, d	Complement R	$\overline{R}$ → dest	1	Z
RLR	R, d	Rotate left f through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	R, d	Rotate right f through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	R, d	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	I	Move Immediate to ACC	I → ACC	1	-
ADDIA	I	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	I	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
ANDIA I	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA I	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA I	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA I	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL I	Call subroutine	PC + 1 → Top of Stack, I → PC	2	-
GOTO I	Unconditional branch	I → PC	2	-

Note : 1. 2 cycles for skip, else 1 cycle(one Fcpu clock)

2. bit : Bit address within an 8-bit register R
R : Register address (00h to 7Fh)
I : Immediate data
ACC : Accumulator
D : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
Dest : Destination
PC : Program Counter
PCHBUF : High Byte Buffer of Program Counter
WDT : Watchdog Timer Counter
GIE : Global interrupt enable bit
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

【11】Absolute Maximum Ratings

Parameter	Conditions	Values		Unit
		min.	max.	
Ambient Operating Temperature	-	-40	85	℃
Storage Temperature	-	-40	150	℃
DC Supply Voltage	-	2.1	5.5	V
Supply Current	-	-	-	mA
Voltage on all GPIO pin	Respect to VSS	-0.3	VDD+0.3V	V

【12】DC Characteristics

12.1 General (Operating Temperature = 0 to 70 ℃)

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP	MAX	
VDD	Operating Voltage	--	2.1		5.5	V
I_{dd1}	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=16MHz		2.8		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=2.1V,No GPIO loading IRC Operating, FCPU=16MHz		1.3		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading IRC Operating , FCPU=1MHz		1		mA
	Normal Mode Operating Current Typical = (Disable ADC)	Vdd=2.1V,No GPIO loading IRC Operating, FCPU=1MHz		480		uA
I_{dd2}	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading SIRC Operating, FCPU=32KHz		650		uA
	Slow Mode Operating Current Typical = (Disable ADC)	Vdd=2.4V,No GPIO loading SIRC Operating, FCPU=32KHz		300		uA
I_{dd3}	Green Mode Operating Current (Enable LVDT watch Dog Enable) Typical = (Disable ADC)	Vdd=5V~2.1V,No GPIO loading WDT = 32ms wake up=320us SIRC Operating ,FCPU=Disable	110	--	500	uA
	Green Mode Operating Current (Disable LVDT watch Dog Enable) Typical (Disable ADC,LVD)	Vdd=5~2.1V,No GPIO loading WDT = 32ms wake up=320us SIRC Operating ,FCPU=disable	30	--	350	uA
I_{dd4}	Suspend Mode Current Typical = (Disable ADC)	Vdd=5V,No GPIO loading @25 ℃		1		uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd=3V,No GPIO loading @25 ℃		0.3		uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd=4.5V,No GPIO loading @85 ℃				uA
	Suspend Mode Current Typical = (Disable ADC)	Vdd<=4.2V,No GPIO loading @85 ℃				uA
V_{LVDT}	Low Voltage Detect	VDT36, △=150mV @25 ℃	3.6-△	3.6	3.6+△	V

Symbol	Parameter	Conditions	Values			Unit
			MIN.	TYP	MAX	
		VDT30, △=150mV @25 ℃	3.0-△	3.0	3.0+△	V
		VDT24, △=150mV @25 ℃	2.4-△	2.4	2.4+△	V
		VDT20 , △=150mV @25 ℃	2.0-△	2.0	2.0+△	V
V_{POR}	Power Reset	VDD from 0V to 5V(POR)			2.1V	V
		VDD from 5V to 0V(PDR)	1.8			V
F_{CPU}	MCU work frequency	25 ℃, VDD > 1.8V			16	MHz
						MHz
F_{IRC}	Internal high RC frequency	VDD=5V, 25 ℃, F_{IRC}=16Mhz △ = 16 * (2 %)	16 - △	16	16+△	MHz
		VDD=2.2~5V, @25 ℃ F_{IRC} = 16Mhz △ = 16 * (2 %)	16 - △	16	16+△	MHz
F_{SIRC}	Internal Slow RC frequency	VDD=2.2~5V, @25 ℃ △ = 32 * (10 %)	32 -△	32	32+△	KHz
T_{POREXT}	Power on reset Timing	SELPOR = 2'b11 (16ms) VDD =5V	13		19	mS
		SELPOR = 2'b11 (16ms) VDD =3V	13		19	mS
$C_{cyrstal}$	External crystal capacitance	Fcrystal = 16Mhz (XIN pin connect, XOUT no connect)		33		pF
		Fcrystal = 32Khz (XIN, XOUT pin connect)		33		pF
V_{INREFH}	Internal Reference High	V_{INREFH} = 4V (Vdd=5V, 25 ℃) △ = 4V * (1.0%)	4-△	4	4+△	V
		V_{INREFH} = 3V (Vdd=5V, 25 ℃) △ = 3V * (1.0 %)	3-△	3	3+△	V
		V_{INREFH} = 2V (Vdd=5V, 25 ℃) △ = 2V * (1.0 %)	2-△	2	2+△	V

12.2 GPIO Interface

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
V_{IR}	Input Voltage Range on all GPIO pin	Respect to VSS	-0.3	VDD+0.3	V
V_{up1}	GPIO Pull-up Resistor	VDD=5~3V	90	110	KΩ
V_{OL}	Output Low Voltage(Sink)	VDD=5~3V, I_{OL}=20mA	-	0.2	V
		VDD=3~2.4V, I_{OL}=18mA		0.25	V
V_{OH}	Output High Voltage(Drive)	VDD=5~3V, I_{OH}=20mA VDD=3V~2.4V, I_{OH}=19mA	VDD-0.4V	-	V
V_{IL}	Input Low Voltage	VDD=5V (All GPIO input)		VDD*0.3	V
		VDD=4V (All GPIO input)		VDD*0.3	V
		VDD=2.2V (All GPIO input)		VDD*0.3	V
V_{IH}	Input High Voltage	VDD=5V (All GPIO input)	VDD*0.7		V
		VDD=4V (All GPIO input)	VDD*0.7		V
		VDD=2.2V (All GPIO input)	VDD*0.7		V
V_{IL2}	Input Low Voltage	Reset Pin			V
V_{PH_vpp}	VPP Pull High Voltage	VDD=5V (VPP output)	3.5V	--	V
		VDD=4V (VPP output)	2.6V	--	V
		VDD=2.4V (VPP output)	1.4V	--	V

12.3 ADC specification

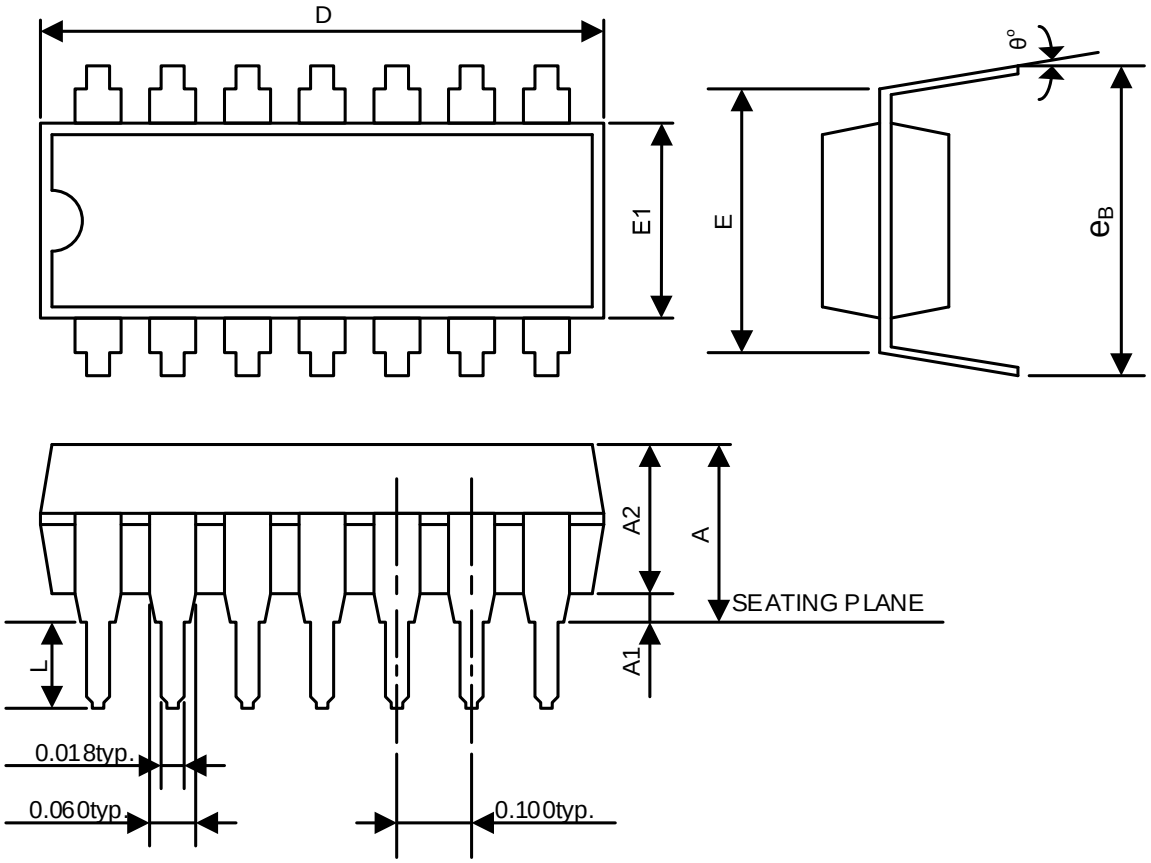
Symbol	Parameter	Conditions	Values			Unit
			min.	Typ.	max.	
ADCSR	ADC sample Rate	-			32	KHz
DNL	Differential Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			±0.65	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			±0.23	LSB
INL	Integral Nonlinearity	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			±2.5	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			±1.0	LSB
GE	Gain Error	Resolution = 12 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			--	LSB
		Resolution = 10 bit VDD=5.0V, VREFH = 3.3V FADCSR=64K			--	LSB
ADCRL	ADC Resolution Typical = bit	VDD=5.0V, VREFH = 3.3V FADCSR=64K	8	10	12	bit

12.4 CMP specification

Symbol	Parameter	Conditions	Values			Unit
			min.	Typ.	max.	
V_{IO}	Input offset voltage	VDD=5V~2.1V		+/-10		mV
V_{ICM}	Input common mode voltage	VDD=5V~2.1V	0		VDD	V

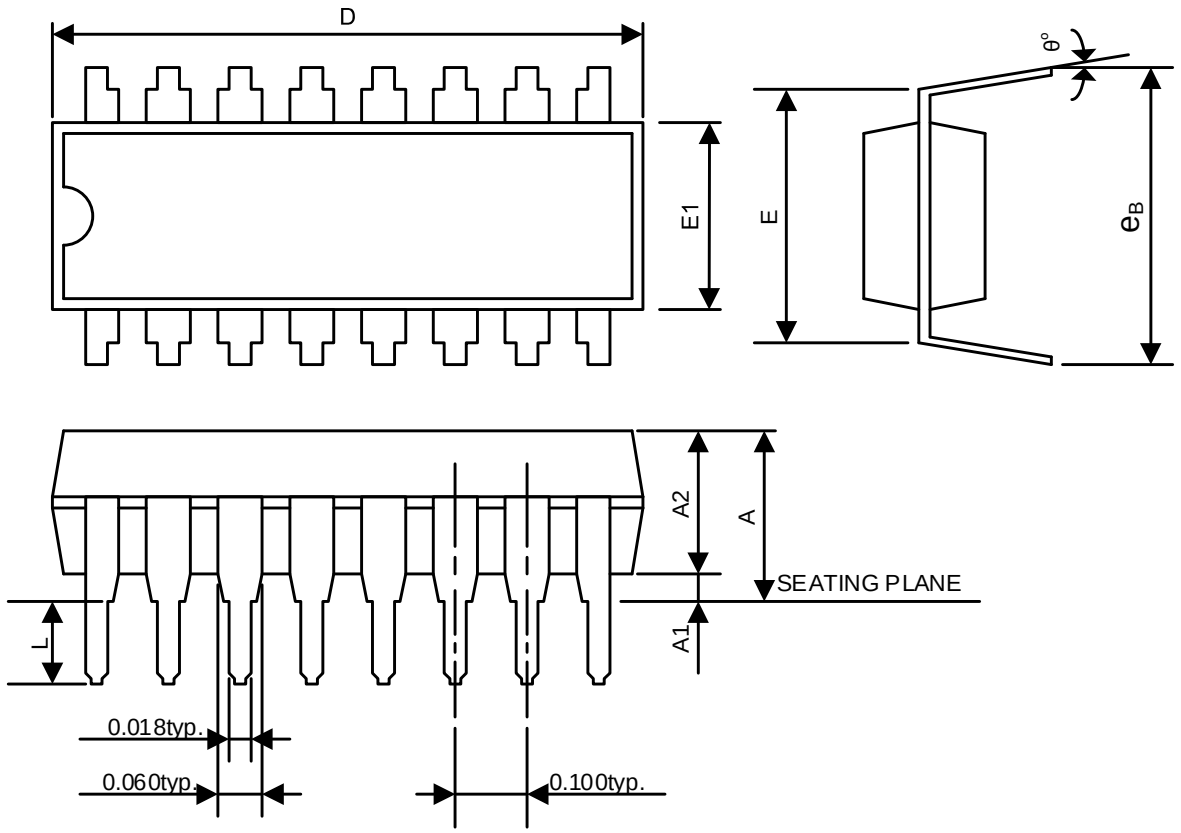
【13】Package Diagram

13.1 14-PIN PDIP



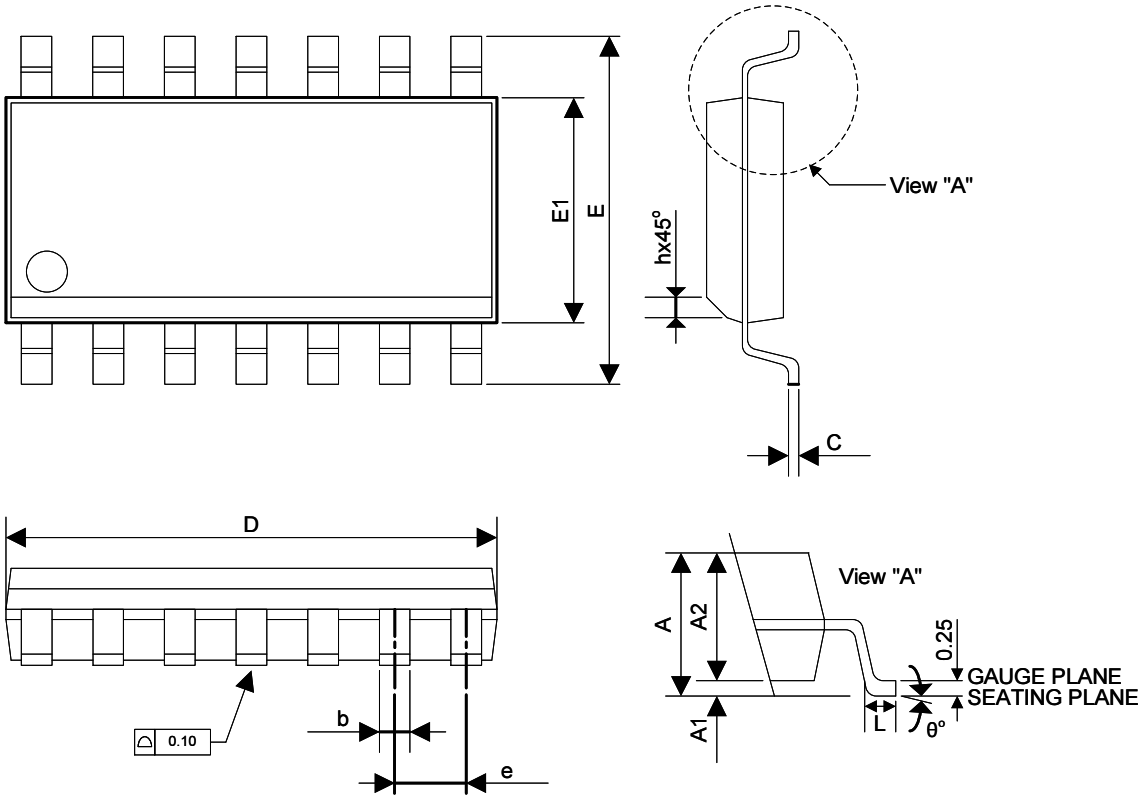
Symbols	Dimension in Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.735	0.750	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

13.2 16-PIN PDIP



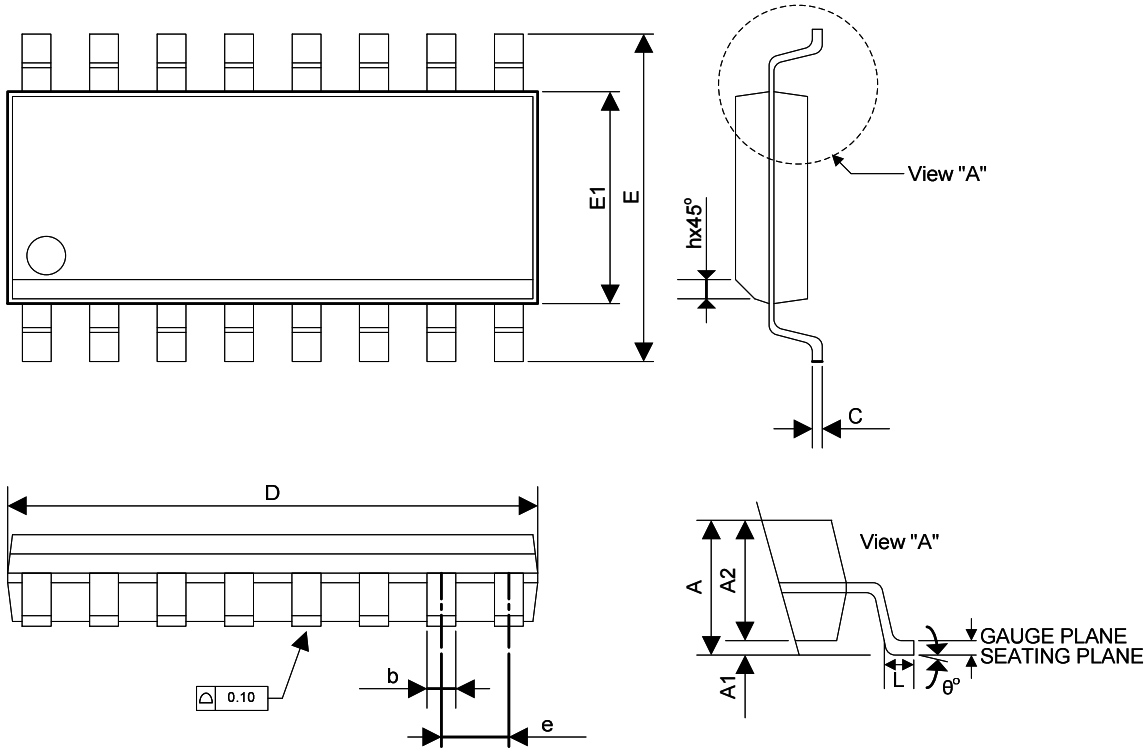
Symbols	Dimension in Inches		
	Min	Nom	Max
A	-	-	0.172
A1	0.015	-	0.038
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

13.3 14-PIN SOP 150mil



Symbols	Dimension in MM		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
C	0.10	-	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
H	0.25		0.50
θ	0^o	-	8^o

13.4 16-PIN SOP 150mil



Symbols	Dimension in MM		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	-	1.27
H	0.25	-	0.50
θ	0^o	-	8^o

【14】ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size	MOQ	MSL	Sample Stock
FM8PC71AMBEP	PDIP	16	300mil	3,000EA/Tube	3	Call sales
FM8PC71AMBED	SOP	16	150mil	3,000EA/Tube 3,000EA/Reel	3	Call sales
FM8PC71AMAEP	PDIP	14	300mil	3,000EA/Tube	3	Call sales
FM8PC71AMAED	SOP	14	150mil	3,000EA/Tube 3,000EA/Reel	3	Call sales