芯海科技
CHIPSEA
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CS32F035/F036 DATASHEET

32-bit ARM® M0-based MCU

REV 1.4

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Revision History

Reversion	Description	Date
1.0	First edition	2020-7-18
1.1	New model CS32F035K6U6	2020-12-31
1.2	Change in CS32F036K6U7 package thickness	2021-3-5
1.3	And package introduction	2021-8-17
1.4	Add model cs32f035f6p7 Delete the tape packing model in the order information	2021-8-30

Table of contents

1 Introduction

The CS32F035/F036 is a series of 32-bit ARM® Cortex®-M0 based microcontroller including CS32F035 and CS32F036, ranging from 20 to 32 pins with 32KB Flash and 4KB of SRAM. The maximum operating frequency is 48MHz. The CS32F035/F036 offer standard communication inerfaces (SPI, USART, I2C), one 12-bit SAR ADC, five 16-bit timers and one advanced-PWM timer.

The CS32F035/F036 can operate in the temperature range of -40 to 85℃ or -40 to 105℃ and power supply range of 2.0 to 5.5V.

The CS32F035/F036 offer a set of low-power modes, saving power for different applicaions.

The CS32F035/F036 microcontrollers are suitable for different applications, such as Smart Appliance, mobile device, consumer electronics, industrial applications, and GPS device.

2 Features

- Core
  - 32-bit ARM® Cortex® -M0
  - up to 48MHz
- Memories
  - 32KB program flash
  - 192B data flash
  - 4KB SRAM with parity check
- Clocks
  - 8MHz internal RC oscillator(HRC), ±1%@typ
  - 14MHz internal RC oscillator(HRC14), ±1%@typ
  - 40KHz internal RC oscillator(LRC), ±10%@typ
  - 4~32MHz external high speed crystal oscillator(HXT)
  - Internal x2,x3,..,x16 Phase-locked loop(PLL), up to 48MHz
- Operation environment
  - VDD power supply: 2.0 to 5.5V
  - VDDA power supply: 2.0 to 5.5V
  - Temperature range: -40 to 85℃ or -40 to 105℃
- BOOT mode
  - Support boot from program flash
  - Support boot from system memory
  - Support boot from SRAM
- Power management
  - Low-power modes: sleep, deepsleep1, deepsleep2, powerdown
  - Power-on/power-down reset (POR/PDR)
  - Low voltage detector (LVD)
- I/Os
  - 27 I/Os up to 48MHz
  - All I/Os can be mapped to external interrupt vectors
- ADC
  - One 12-bit ADC
  - Conversion time is up to 1uS
  - Up to 10 external input channels
  - Operation voltage range: 2.4 to 5.5V
  - Input signal range: 0~5.5V
- Timers
  - One advanced 16-bit timer for 6 channels PWM output
  - Fore general purpose 16-bit timers
  - One basic 16-bit timer
  - One free watchdog timer (FWDT): 8-bit prescaler and 12-bit downcounter
  - One window watchdog timer (WWDT): 7-bit downcounter

  - One SysTick timer: 24-bit downcounter
- DMA
  - Five channels
  - Support peripherals: SPIx, I2Cx, USARTx, TIMx, ADC
- Inerrupt and events
  - Up to 32 maskable interrupt channels
  - Four priority levels
  - Sixteen external interrupt lines
- SPI
  - Onr SPI
  - 3-bit predivider suppport 8 kinds of frequency
  - Frame size can be configed to 4 to 16 bits
- USART
  - Two USARTs
  - Support: ISO7816, LIN, IrDA mode
  - Support auto baudrate detection
  - Can wakeup from deepsleep1 and deepsleep2
- I2C
  - One I2C with master or slave mode
  - Support: standard mode (up to 100k bit/s), Fast mode (up to 400k bit/s),
  - Support: 7-bit and 10-bit addressing modes
- CRC unit
- Serial wire debug (SWD)
- Packages
  - TSSOP20
  - QFN28
  - QFN32
  - LQFP32

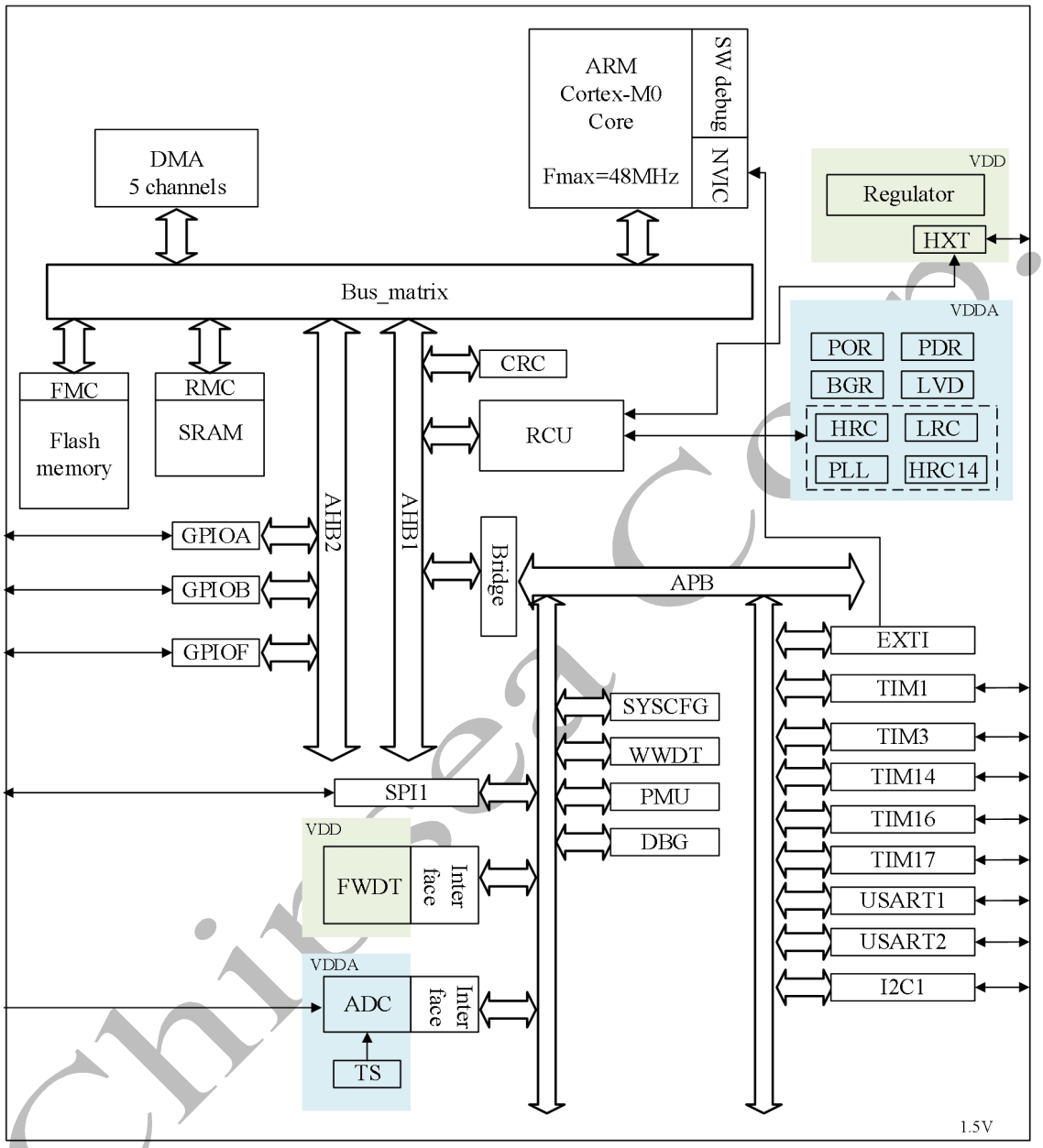
3 Configuration

The package of CS32F035/F036 serial include: TSSOP20, QFN28, QFN32, LQFP32.

CS32F035/F036 serial

Configured device		CS32F035	CS32F036			
		K6Ux	F6Px	G6Ux	K6Ux	K6Tx
Flash（Kbytes）		32	32	32	32	32
SRAM（Kbytes）		4	4	4	4	4
Timers	16-bit Advanced	1				
	16-bit General purpose	4				
	FWDT	1				
	WWDT	1				
	SysTick	1				
Communication interfaces	SPI	1	1	1	1	1
	I2C	1	1	1	1	1
	USART	2	2	2	2	2
ADC	Unit	1				
	Ext. channel	10		9		10
	Int. channel	2				
I/O		27	15	23	27	25
Operating voltage		2~5.5V				
Operating temperature		Ambient operation temperature: -40~85^{0}C /-40~105^{0}C Junction temperature: -40~105^{0}C /-40~125^{0}C				
Packing Type		QFN32 (4×4×0.75-e=0.40)	TSSOP20	QFN28 (4×4×0.55-e=0.50)	QFN32 (5×5×0.75-e=0.50)	LQFP32

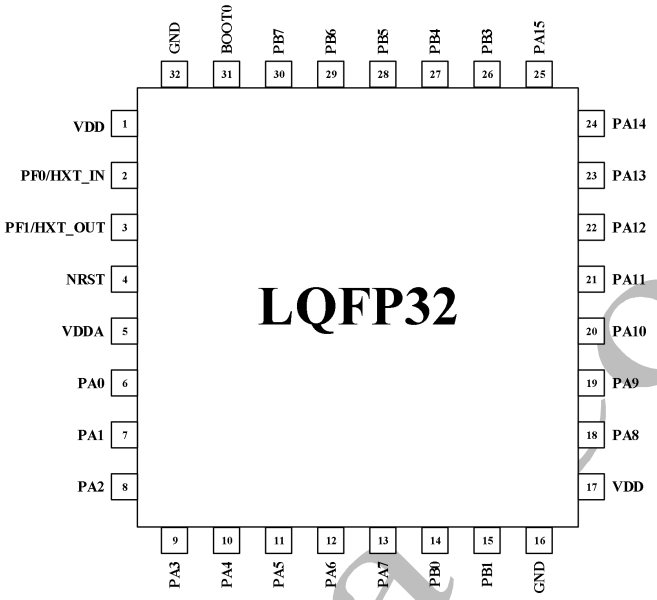
Figure 1 Block diagram



4 Pin description

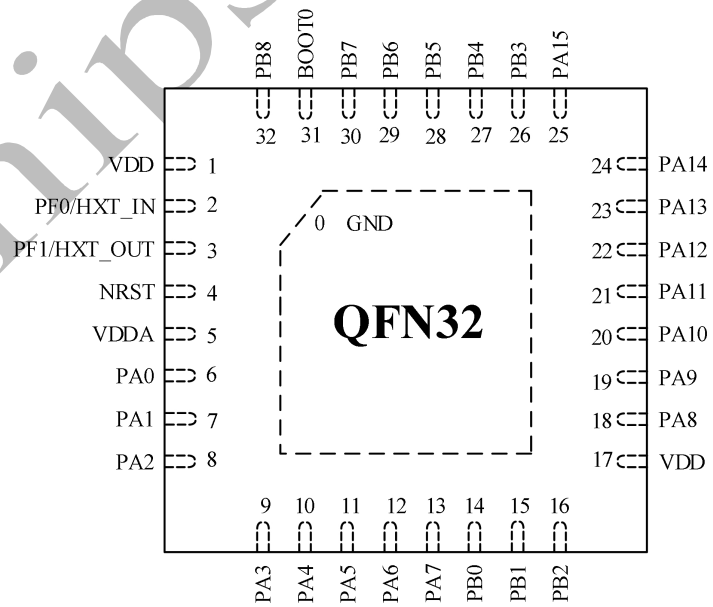
4.1 LQFP32

Figure 2 Top view of LQFP32



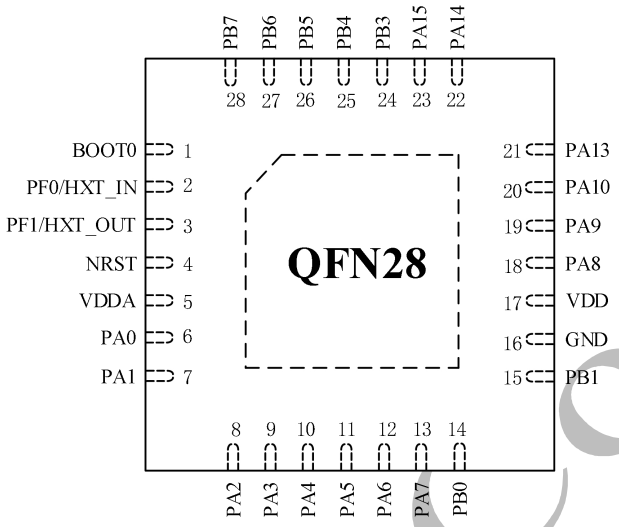
4.2 QFN32

Figure 3 Top view of QFN32



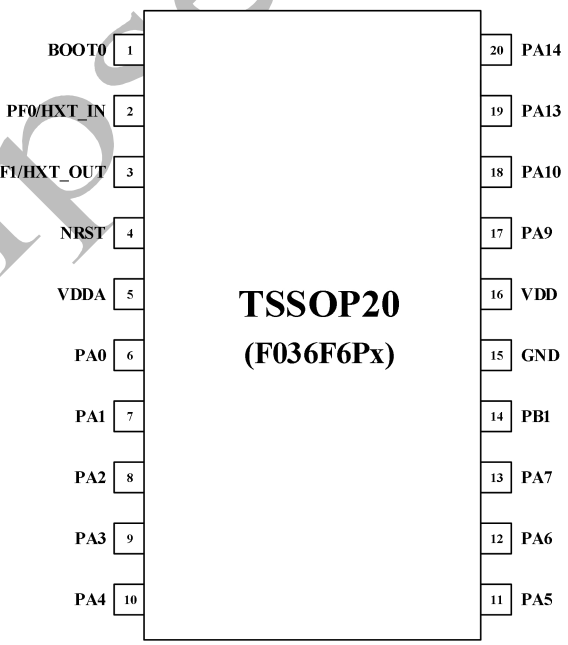
4.3 QFN28

Figure 4 Top view of QFN28



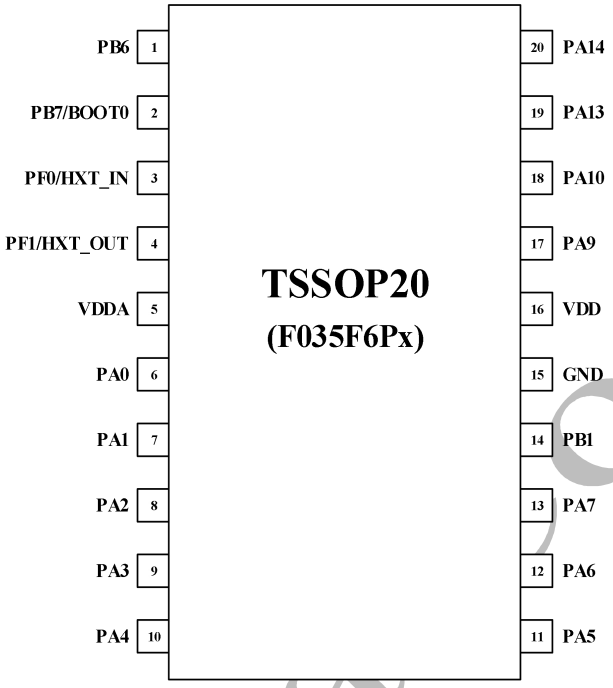
4.4 TSSOP20（CS32F036F6Px）

Figure 5 Top view of TSSOP20



4.5 TSSOP20（CS32F035F6Px）

Figure 6 Top view of TSSOP20



4.6 Pin description

Pin description part1

Pin No.				Pin name	Type	Description	
LQFP32	QFN32	QFN28	TSSOP20			Multiplexed funcions	Special functions
2	2	2	2	PF0/HXT_IN (PF0)	I/O	-	HXT_IN
3	3	3	3	PF1/HXT_OUT (PF1)	I/O	-	HXT_OUT
4	4	4	4	NRST	I/O	Reset input / internal reset output, with weak pull-up resistor（active low）	
5	5	5	5	VDDA	S	Analog power supply	
6	6	6	6	PA0	I/O	USART2_CTS	ADC_IN0, WKUP1
7	7	7	7	PA1	I/O	EVENTOUT, USART2_RTS	ADC_IN1
8	8	8	8	PA2	I/O	USART2_TX	ADC_IN2
9	9	9	9	PA3	I/O	USART2_RX	ADC_IN3
10	10	10	10	PA4	I/O	SPI1_NSS, TIM14_CH1, USART2_CK	ADC_IN4
11	11	11	11	PA5	I/O	SPI1_SCK	ADC_IN5
12	12	12	12	PA6	I/O	SPI1_MISO,	ADC_IN6

						TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	
13	13	13	13	PA7	I/O	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
14	14	14		PB0	I/O	TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
15	15	15	14	PB1	I/O	TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
	16			PB2	I/O	-	-
16		16	15	GND	S	Ground	
17	17	17	16	VDD	S	Digital power supply	
18	18	18		PA8	I/O	USART1_CK, TIM1_CH1, EVENTOUT, CKO	-
19	19	19	17	PA9	I/O	USART1_TX, TIM1_CH2, I2C1_SCL, CKO	I2C. support Fast mode Plus
20	20	20	18	PA10	I/O	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA	I2C. support Fast mode Plus
21	21			PA11	I/O	USART1_CTS, TIM1_CH4, EVENTOUT	-
22	22			PA12	I/O	USART1_RTS, TIM1_ETR, EVENTOUT	-
23	23	21	19	PA13 (SWDIO) (1)	I/O	IR_OUT, SWDIO	-
24	24	22	20	PA14 (SWCLK) (1)	I/O	USART2_TX, SWCLK	-
25	25	23		PA15	I/O	SPI1_NSS, EVENTOUT, USART2_RX	-
26	26	24		PB3	I/O	SPI1_SCK, EVENTOUT	-
27	27	25		PB4	I/O	SPI1_MISO, TIM3_CH1, EVENTOUT	-
28	28	26		PB5	I/O	SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
29	29	27		PB6	I/O	I2C1_SCL, USART1_TX, TIM16_CH1N	I2C. support Fast mode Plus

30	30	28		PB7	I/O	I2C1_SDA, USART1_RX, TIM17_CH1N	I2C. support Fast mode Plus
31	31	1	1	BOOT0	I	Boot memory selection	
	32			PB8	I/O	I2C1_SCL, TIM16_CH1	
32	0			GND	S	Ground	
1	1			VDD	S	Digital power supply	

Note
(1) After reset, these pins will be configured as SWDIO and SWCLK. Meanwhile, the internal pull-up of the SWDIO pin and the internal pull-down of the SWCLK pin will open.

Pin description part2

Pin NO.		Pin name	Type	描述	
QFN32	TSSOP20			Multiplexed funcions	Special functions
2	3	PF0/HXT_IN (PF0)	I/O	-	HXT_IN
3	4	PF1/HXT_OUT (PF1)	I/O	-	HXT_OUT
4		NRST	I/O	Reset input / internal reset output, with weak pull-up resistor（active low）	
5	5	VDDA	S	Analog power supply	
6	6	PA0	I/O	USART2_CTS	ADC_IN0, WKUP1
7	7	PA1	I/O	EVENTOUT, USART2_RTS	ADC_IN1
8	8	PA2	I/O	USART2_TX	ADC_IN2
9	9	PA3	I/O	USART2_RX	ADC_IN3
10	10	PA4	I/O	SPI1_NSS, TIM14_CH1, USART2_CK	ADC_IN4
11	11	PA5	I/O	SPI1_SCK	ADC_IN5
12	12	PA6	I/O	SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6
13	13	PA7	I/O	SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
14		PB0	I/O	TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
15	14	PB1	I/O	TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
16		PB2	I/O	-	-
	15	GND	S	Ground	

17	16	VDD	S	Digital power supply	
18		PA8	I/O	USART1_CK, TIM1_CH1, EVENTOUT, CKO	-
19	17	PA9	I/O	USART1_TX, TIM1_CH2, I2C1_SCL, CKO	I2C. support Fast mode Plus
20	18	PA10	I/O	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA	I2C. support Fast mode Plus
21		PA11	I/O	USART1_CTS, TIM1_CH4, EVENTOUT	-
22		PA12	I/O	USART1_RTS, TIM1_ETR, EVENTOUT	-
23	19	PA13 (SWDIO) (1)	I/O	IR_OUT, SWDIO	-
24	20	PA14 (SWCLK) (1)	I/O	USART2_TX, SWCLK	-
25		PA15	I/O	SPI1_NSS, EVENTOUT, USART2_RX	-
26		PB3	I/O	SPI1_SCK, EVENTOUT	-
27		PB4	I/O	SPI1_MISO, TIM3_CH1, EVENTOUT	-
28		PB5	I/O	SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
29	1	PB6	I/O	I2C1_SCL, USART1_TX, TIM16_CH1N	I2C. support Fast mode Plus
30	2	PB7	I/O	I2C1_SDA, USART1_RX, TIM17_CH1N	I2C. support Fast mode Plus
31		BOOT0	I	Boot memory selection	
32		PB8	I/O	I2C1_SCL, TIM16_CH1	
0		GND	S	Ground	
1		VDD	S	Digital power supply	

Note
(2) After reset, these pins will be configured as SWDIO and SWCLK. Meanwhile, the internal pull-up of the SWDIO pin and the internal pull-down of the SWCLK pin will open.

5 I/O Multiplexing

5.1 PORT A multiplexed functions

PORT A multiplexed functions

Pin number	Multiplexed function 0	Multiplexed function 1	Multiplexed function 2	Multiplexed function 3	Multiplexed function 4	Multiplexed function 5	Multiplexed function 6	Multiplexed function 7
PA0		USART2_CTS						
PA1	EVENTOUT	USART2_RTS						
PA2		USART2_RX						
PA3		USART2_TX						
PA4	SPI1_NSS	USART2_CK			TIM14_CH1			
PA5	SPI1_SCK,							
PA6	SPI1_MISO,	TIM3_CH1	TIM1_BKIN			TIM16_CH1	EVENTOUT	
PA7	SPI1_MOSI,	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	
PA8	CKO	USART1_CK	TIM1_CH1	EVENTOUT				
PA9		USART1_TX	TIM1_CH2		I2C1_SCL	CKO		
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3		I2C1_SDA			
PA11	EVENTOUT	USART1_CTS	TIM1_CH4					
PA12	EVENTOUT	USART1_RTS	TIM1_ETR					
PA13	SWDIO	IR_OUT						
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS,	USART2_RX	TIM2_CH1_ETR	EVENTOUT				

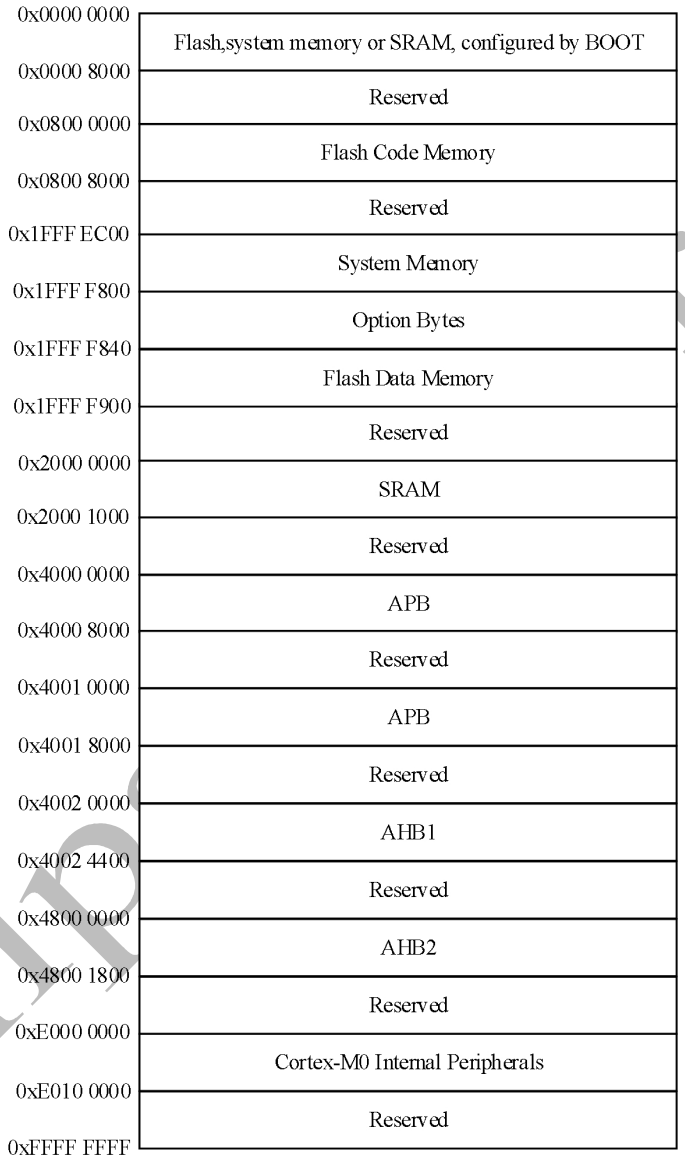
5.2 PORT B multiplexed functions

PORT B multiplexed functions

Pin number	Multiplexed function 0	Multiplexed function 1	Multiplexed function 2	Multiplexed function 3	Multiplexed function 4	Multiplexed function 5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N			
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N			
PB2						
PB3	SPI1_SCK,	EVENTOUT				
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT			
PB5	SPI1_MOSI,	TIM3_CH2	TIM16_BKIN	I2C1_SMBA		
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N			
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N			
PB8		I2C1_SCL	TIM16_CH1			

6 Memory

Figure 6 Memory mapping



Memory mapping table

Memory		Start address	Size
Flash, system memory or SRAM, congfigured by BOOT		0x0000 0000	32Kbytes
Program flash		0x0800 0000	32Kbytes
System memory		0x1FFF EC00	3Kbytes
Option Bytes		0x1FFF F800	64bytes
Data flase		0x1FFF F840	192bytes
SRAM		0x2000 0000	4Kbytes
APB	Reserved	0x4000 0000	1Kbytes
	TIM3	0x4000 0400	1Kbytes
	Reserved	0x4000 0800	2Kbytes
	TIM6	0x4000 1000	1Kbytes
	TIM7	0x4000 1400	-
	Reserved	0x4000 1800	2Kbytes
	TIM14	0x4000 2000	1Kbytes
	Reserved	0x4000 2400	1Kbytes
	Reserved	0x4000 2800	1Kbytes
	WWDT	0x4000 2C00	1Kbytes
	FWDT	0x4000 3000	1Kbytes
	Reserved	0x4000 3400	1Kbytes
	SPI2	0x4000 3800	1Kbytes
	Reserved	0x4000 3C00	2Kbytes
	USART2	0x4000 4400	1Kbytes
	Reserved	0x4000 4800	-
	Reserved	0x4000 4C00	-
	Reserved	0x4000 5000	-
	I2C1	0x4000 5400	1Kbytes
	Reserved	0x4000 5800	1Kbytes
	Reserved	0x4000 5C00	5Kbytes
	PMU	0x4000 7000	1Kbytes
	Reserved	0x4000 7400	3Kbytes
	SYSCFG	0x4001 0000	1Kbytes
	EXTI	0x4001 0400	1Kbytes
	Reserved	0x4001 0800	3Kbytes
	Reserved	0x4001 1400	1Kbytes
	Reserved	0x4001 1800	1Kbytes
	Reserved	0x4001 1C00	1Kbytes

	Reserved	0x4001 2000	1Kbytes
	ADC	0x4001 2400	1Kbytes
	Reserved	0x4001 2800	1Kbytes
	TIM1	0x4001 2C00	1Kbytes
	SPI1	0x4001 3000	1Kbytes
	Reserved	0x4001 3400	1Kbytes
	USART1	0x4001 3800	1Kbytes
	Reserved	0x4001 3C00	1Kbytes
	Reserved	0x4001 4000	1Kbytes
	TIM16	0x4001 4400	1Kbytes
	TIM17	0x4001 4800	1Kbytes
	Reserved	0x4001 4C00	3Kbytes
	DBGMCU	0x4001 5800	1Kbytes
	Reserved	0x4001 5C00	9Kbytes
AHB1	Reserved	0x4000 0000	1Kbytes
	TIM3	0x4000 0400	1Kbytes
	Reserved	0x4000 0800	2Kbytes
	TIM6	0x4000 1000	1Kbytes
	TIM7	0x4000 1400	-
	Reserved	0x4000 1800	2Kbytes
	TIM14	0x4000 2000	1Kbytes
	Reserved	0x4000 2400	1Kbytes
AHB2	Reserved	0x4000 2800	1Kbytes
	WWDT	0x4000 2C00	1Kbytes
	FWDT	0x4000 3000	1Kbytes
	Reserved	0x4000 3400	1Kbytes
	SPI2	0x4000 3800	1Kbytes
	Reserved	0x4000 3C00	2Kbytes
Cortex-M0 internal peripherals		0xE000 0000	1Mbytes

7 Function description

7.1 Core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors .

The ARM® Cortex®-M0 supports low power and efficient operation , high performance interrupt response. It provides a higher code density than other 8-bit and 16-bit microcontrollers, and can be applied to a wider range of embedded systems.

It provides excellent performance. It is compatible with the rest of the Cortex-M processors.

7.2 Memories

CS32F035/F036 supports the following features:

- Flash has three blocks:
  - 32 Kbytes Program flash.
  - 192bytes Data flase.
  - option bytes and system memory.
- 4 Kbytes of embedded SRAM supports embedded parity checking for exception generation .

Program flash supports Write protection with sector size. According to option byte，Program flash supports different levels of protection:

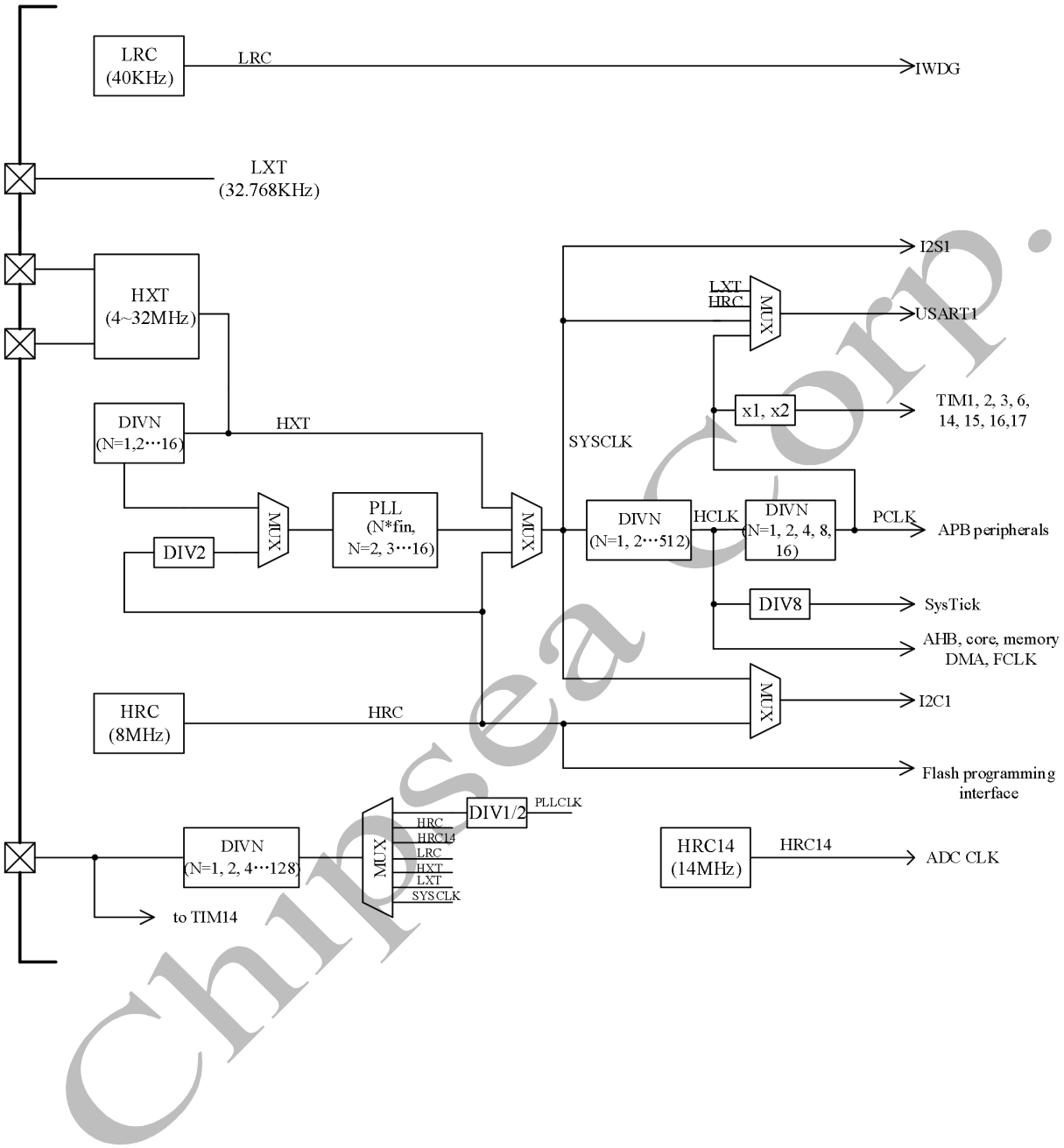
- Level 0 : no protection.
- Level 1: cannot write or read in debug mode or boot in SRAM/bootloader.
- Level 2: can read and cannot write in user mode. Debug mode or boot in SRAM/bootloader is disable.

7.3 Clocks

The clock system consists of:

- 8MHz internal high speed RC oscillator(HRC)
- 14MHz internal high speed RC oscillator(HRC14)
- 40KHz internal low speed RC oscillator(LRC)
- 4~32MHz external high speed crystal oscillator(HXT)
- Internal x2,x3,..,x16 Phase-locked loop(PLL)

Figure 7 Clock tree



7.4 Operation environment

7.4.1 Power supply

The device has three different power supply pins:
VDD: Power supply for I/O lines, internal regulator and HXT. The voltage range is from 2.0V to 5.5V.
VDDA: Power supply for ADC, HRC, HRC14, PLL, POR/PDR and LVD. The voltage range is from VDD to 5.5V. When ADC is used, the minimum voltage of VDDA is 2.4V.
VBAT: power supply for RTC, LXT and backup registers. The voltage range is from 1.65V to 5.5V.

7.5 BOOT mode

CS32F035/F036XXXX supports three different startup locations:

Different startup locations

BOOT0 pin	nBOOT1 bit	boot location
0	X	Program flash
1	1	system memory
1	0	SRAM

7.6 Power management

7.6.1 Low power modes

The device has four low power modes:

- Sleep mode

The CPU is stopped when the device enters into sleep mode. In the sleep mode, all peripherals can operate continuously and an interrupt/event can wake up the CPU.

- Deepsleep1 mode

In deepsleep1 mode, PLL, HRC and HXT are disabled. The regulator is on, the content of 1.5V domain can't be lost.

Any one of the EXTI lines can wake up the device in deepsleep1 mode.

- Deepsleep2 mode

In deepsleep2 mode, the PLL, HRC and HXT are disabled. The regulator is on, the content of 1.5V domain can't be lost. The internal regulator is in low power mode, so the wakeup time of deepsleep2 is bigger than the wakeup time of deepsleep1.

Any one of the EXTI lines can wake up the device in deepsleep2 mode.

- Powerdown mode

In powerdown mode, the 1.5V regulator is switched off so that the contents of SRAM and registers are lost except for backup registers in VBAT domain. The PLL, HRC, HRC14 and HXT are switched off.

An external reset, a FWDT reset, a rising edge on the WKUP pins can wake up the device in powerdown mode.

7.6.2 POR/PDR

The device has power-on reset and power-down reset circuits. The POR circuit monitors VDD supply voltage. The PDR circuit monitors both VDD and VDDA supply voltage.

These circuits are always active to monitor if operation voltage is bigger than 2V. Once the circuits monitor the power supply voltage is lower than 2V, the device will keep in reset state.

7.6.3 LVD

The device has a low voltage detector(LVD), which can monitor the VDD supply voltage and compare it to the threshold voltage of LVD. Once VDD is lower than the threshold voltage or higher than the threshold voltage, an interrupt will be generated. And the threshold voltage can be programmed.

7.7 I/Os

All GPIO pins can be configured as input (with pull-up or pull-down), output or allocated to peripherals. The output function can be configured to be push-pull or open-drain.

The I/O configuration can be locked to prevent from accidental operation.

7.8 ADC

The CS32F035/F036XXXX contains a 12-bit successive approximation analog-to-digital converter. The ADC can perform AD conversions on up to 13 channels, including 10 external channels and 3 internal channels. The three internal channels are used for monitoring the VBAT voltage, measuring the internal reference voltage and measuring the temperature of the chip. With the selected conversion group and work mode, conversions were performed in a single mode, continuous mode , or discontinuous mode. Vaious conversion configurations are supported, including sampling time,data resolution, data format alignment and scan sequence direction.

The conversion can be triggered by software or hareware events generated by different timers. A dedicated HRC14 clock is available for ADC, as well as divided PCLK, which contains no clock uncertainty in hardware trigger event.

An analog watchdog is built inside ADC, which can be activated to monitor the voltage of a single channel or a conversion group. Once the voltage is out of the given window, a WDGEVT alarm is generated.

The output data can be managed by DMA. DMA one-shot mode is provided to end AD conversion when a certain amount of data is transfered, while DMA circle allows output data to be continuous transferred until AD conversion is stopped manually.

7.8.1 Temperature sensor

Temperature sensor(TS) block generates a voltage TS_OUT which is linear with temperature. TS_OUT is snet to ADC channel ADIN_16. ADC will convert the voltage into a digital value. In order to provides good linearity, TS should be calibrated first. The calibration data are stored in the system memory area,which is read only.

TS calibration values

Calibration value name	Description	Address
TEMP30_CAL	TS ADC data at 30^0C(+/-5^0C), VDDA=3.3V(+/-10mV)	0x1FFF F7B8 - 0x1FFF F7B9
TEMP110_CAL	TS ADC data at 110^0C(+/-5^0C), VDDA=3.3V(+/-10mV)	0x1FFF F7C2 - 0x1FFF F7C3

7.8.2 Internal refenence voltage

The internal reference voltage Vrefint provides a bandgap voltage for ADC. It is sent to channel ADIN_17. Vrefint is measured during production test and stored in the system memory area,which is read only.

Vrefint calibration values

Calibration value name	Description	Address
VREFINT_CAL	V_{refint} ADC data at 30^0C(+/-5^0C), VDDA=3.3V(+/-10mV)	0x1FFF F7BA - 0x1FFF F7BB

7.8.3 VBAT monitor

VBAT voltage is measured by ADC to monitor if it is in the proper range. It is sent to channel ADIN_18. To avoid the case that VBAT is higher than VDDA, the VBAT voltage is divided by 2 before sent to ADC.

7.9 Timers

The devices include one advanced control timer, six general-purpose timers and one basic timer.

TIMx feature comparison

Type	Timer	Counter witdh	Direction	Pre-divider	DMA requrest	Channels	Complementary channels
Advanced Control	TIM1	16-bit	Up, down, up and down	From 1 to 65536	Yes	4	3
	TIM3	16-bit	Up, down, up and down	From 1 to 65536	Yes	4	0
	TIM14	16-bit	Up	From 1 to 65536	No	1	0
	TIM16	16-bit	Up	From 1 to 65536	Yes	1	1
	TIM17	16-bit	Up	From 1 to 65536	Yes	1	1

7.9.1 Advanced-control timer (TIM1)

The advanced timer (TIM1) is a 16-bit counter timer with a 16-bit pre-divider, which can count up, down or up and down. It has four-channels which supports input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. Its complementary output channels has common programmable inserted dead time.

TIM1 can be internal connected with other timers for synchronization or event trigger. The registers of TIM1 can be accessed by DMA when DMA request is enabled.

The counter can be stopped in debug mode.

7.9.2 General-purpose timer (TIM 3, 14, 16, 17)

There are four general-purpose timers, which can be used as simple time base or output PWM.

- **TIM3**

TIM3 is a 16-bit counter timer with a 16-bit pre-divider, which can count up, down or up and down. They have four channels for independent input capture, output compare and PWM.

TIM3 can work together or with other TIMs through internal connection for synchronization or event trigger. The registers of TIM3 can be accessed when DMA request is enabled.

The counter can be stopped in debug mode.

- **TIM14**

TIM14 is a 16-bit upcounter timer with a 16-bit pre-divider, which only has one channel for input capture, output compare and PWM.

The counter can be stopped in debug mode.

- **TIM16/TIM17**

TIM16(one channel) and TIM17 (one channel) are based on a 16-bit upcounter and a 16-bit pre-divider. Their channels can be used for input capture, output compare and PWM. A programmable dead time generator can be used for their complementary output channels.

Their registers can be accessed by DMA when DMA request is enabled. counters can be stopped in debug mode.

7.9.3 Free watchdog timer (FWDT)

The free watchdog timer is clocked by the internal 40KHz LRC, which is independent of the main clock. The main components of FWDT are an 8-bit pre-divider and a 12-bit downcounter with window option, which can work in deepsleep and powerdown mode. The FWDT can generate a reset when the downcounter reaches zero.

The counter can be stopped in debug mode.

7.9.4 Window watchdog timer (WWDT)

The main components of window watchdog timer are a pre-divider with four options and a 7-bit free running downcounter. It is clocked by PCLK. It can generate a reminder interrupt flag when the downcounter reaches 0x40 and a reset when the downcounter reaches 0x3F.

The counter can be stopped in debug mode.

7.9.5 SysTick

The SysTick can be used not only for real-time operating systems, but also as a standard down counter.

It is based on a 24-bit downcounter with autoreload function, which can be clocked by HCLK or HCLK/8. When the counter reaches zero, SysTick can generate a maskable system interrupt.

7.10 DMA

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and memory.

There are 5 channels in the DMA controller. Each channel is connected to dedicated peripheral(include SPIx,I2Sx,I2Cx,USARTx and TIMx) to manage memory access requests. An arbiter is implemented inside to handle DMA requests priority.

The DMA controller also supports circular buffer mode data transfer.It can remove user code intervention when the controller reaches the end of the buffer.

7.11 Inerrupt and events

Cortex-M0 integrates the Nested Vectored Interrupt Controller (NVIC) for efficient exception and interrupts processing. You can read the Technical Reference Manual of Cortex-M0 for more details.

The Extended interrupt/event controller (EXTI) contains up to 24 independent edge detectors and generates interrupt requests or events to the CPU/Interrupt Controller. The EXTI has three trigger types: rising edge, falling edge and both edges. Each edge detector can be configured and enabled independently.

7.12 SPI

The SPI module can communicate with external devices using the SPI protocol or the I2S audio protocol.

The SPI provide a SPI protocol of data transmission and reception function in master and slave mode. It supports full-duplex and simplex mode, which communication speed can up to 18Mbit/s. A hardware CRC function is also implemented.

DMA can be used for sequential transmission both in SPI mode and I2S mode.

SPIx function table

SPI features/modes	SPI1
Rx/Tx FIFO	√
NSS pulse mode	√
TI mode	√
Hardware CRC function	√

7.13 USART

The Universal Synchronous Asynchronous receiver transmitter (USART) provides a universal interface for serial communication between the MCU and external devices. The USART supports synchronous asynchronous full-duplex communication and single-wire half-duplex communication. It uses a programmable baud rate generator to provide different communication baud rate , up to 6 Mbit/s.

In addition, USART also supports DMA continuous data transmission, automatic baud rate detection, multiprocessor communication, Modbus communication, smartcard mode, LIN mode, IrDA mode, RS232 hardware flow control and RS485 drive enable.USART1 can wakeup MCU from deepsleep1or deepsleep2 mode.

USARTx function table

USART features/modes	USART1	USART2
Asynchronous full duplex communication	√	√
Synchronous mode	√	√
Single-wire half-duplex communication	√	√
DMA	√	√
Auto baud rate detection	√	X
Multiprocessor communication	√	√
Modbus communication	√	X
Smartcard mode	√	X
LIN mode	√	X
IrDA mode	√	X
RS232 hardware flow control	√	√
RS485 Driver Enable	√	√
Wakeup MCU from deepsleep1/2 mode	√	X

7.14 I2C

The I2C (inter-integrated circuit) module provides an industry standard I2C interface. It can work in master mode and slave mode. The I2C interface implements standard I2C protocol with standard-mode, fast-mode and fast-mode plus as well as CRC calculation and checking, SMBus (system management bus) and PMBus (power management bus). The I2C interface support DMA mode for high speed data transfer between memory and peripheral without CPU involved.

Its main features are the following:

- Support Master mode and slave mode
- Multi-master capability
- Programmed digital filter and optional analog filter
- Support 7-bit addressing mode 10-bit address mode
- Support standard-mode (up to 100 KHz) , fast-mode (up to 400 kHz)
- Wakeup from deepsleep1 and deepsleep2 mode
- Support DMA mode

I2Cx function table

I2C features/modes	I2C1
7-bit addressing mode	√
10-bit addressing mode	√
Standard mode(up to 100Kbit/s)	√
Fast mode(up to 400Kbit/s)	√
Independent clock	√
Wakeup from deepsleep1/2	√

7.15 CRC unit

In the field of data storage and data communication, in order to ensure the corretness of data, the cyclic redundancy check (CRC) is used commonly.

This CRC calculation unit can be used to calculate 32 bit CRC code with fixed polynomial.

7.16 Serial wire debug (SWD)

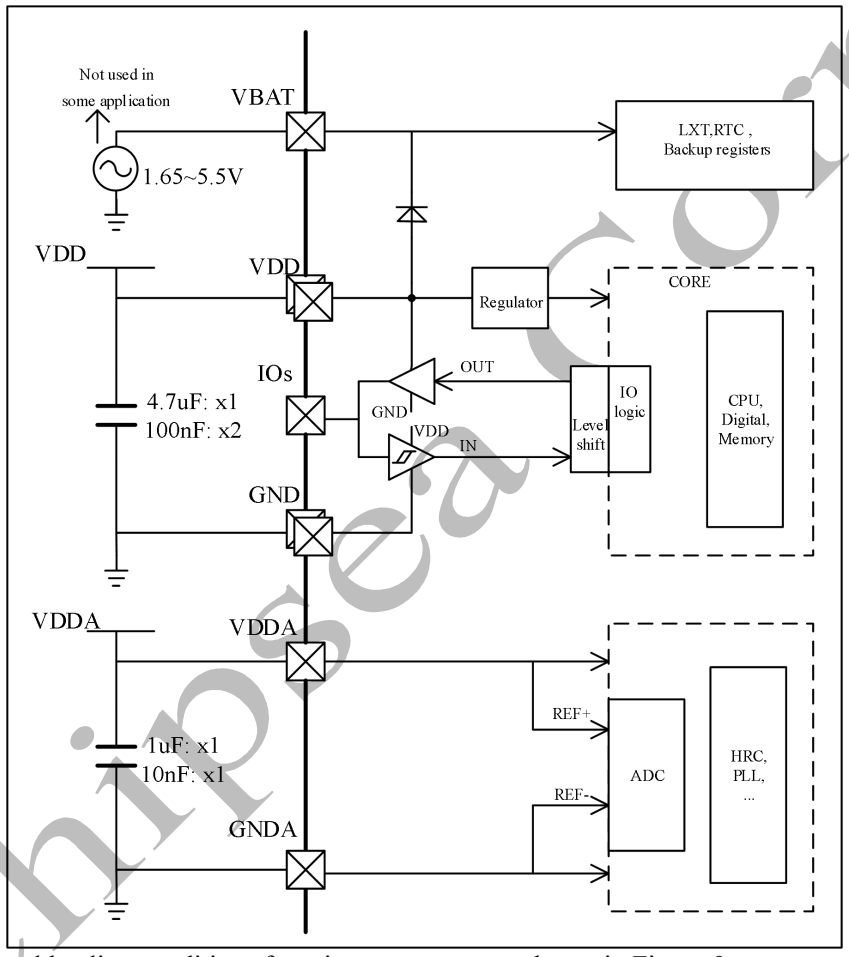
As the ARM Cortex-M0 Core is intergrated, the debug functionality is provided by ARM debug components within M0 core. The ARM serial wire debug port is implemented to access these debug component.

8 Electrical characteristics

8.1 Disclaimer

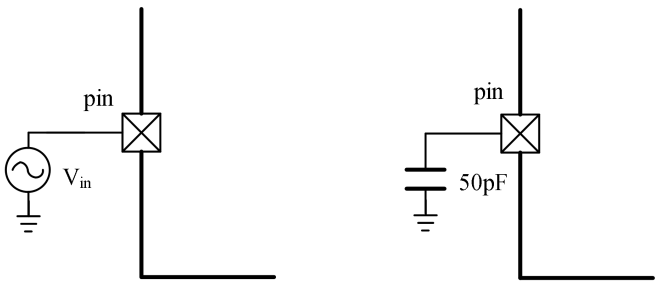
Figure 8 is the power supply scheme of CS32F035/F036.
Unless other specified, all typical values are based on T_{range}=25℃ and VDD=3.3V.
Unless other specified, all voltages are referenced to GND.
Unless other specified, the values are based on design guidelines.

Figure 8 Power supply scheme



The input voltage and loading conditions for pin parameters are shown in Figure 9.

Figure 9 Pin input voltage and loading conditions



(a) Input voltage (b) Loading

8.2 Absolute maximum ratings

Absolute maximum ratings

Symbol	Description	Min	Typ.	Max.	Units
VDD	The voltage between VDD and GND	-0.3	-	6	V
VDDA	The voltage between VDDA and GND	-0.3	-	6	V
VBAT	The voltage between VBAT and GND	-0.3	-	6	V
VDD-VDDA	The voltage between VDD and VDDA	-	-	0.4	V
$V_{i/o}$	The voltage on the I/O pins	GND-0.3	-	6	V
$T_{storage}$	Storage temperature	-65	-	150	℃
$T_{junction}$	Junction temperature	-	-	150	℃
$I_{total-pwr}$	Total current into all of the VDD power lines	-	-	120	mA
$I_{total-GND}$	Total current out of all of the GND power lines	-120	-	-	mA
$I_{pwr-pin}$	Current into each power pin	-	-	100	mA
$I_{GND-pin}$	Current out of each GND pin	-100	-		mA
$I_{total-sunk}$	Total current into all of I/O pin	-	-	80	mA
$I_{total-source}$	Total current out of all of I/O pin	-80	-		mA
$I_{sunk-pin}$	Current into any I/O pin	-	-	25	mA
$I_{source-pin}$	Current out of any I/O pin	-25	-	-	mA

8.3 Operation environment characteristics

Operation environment charateristics

Symbol	Description	Min	Typ.	Max.	Units
$V_{VDD-range}$	The operating voltage range of power supply VDD	2	-	5.5	V
$V_{VDDA-range}$	The operating voltage range of power supply VDDA	2	-	5.5	V
T_{range}	The operating ambient temperature range(case1)	-40	-	85	℃
	The operating ambient temperature range(case2)	-40	-	105	℃
$T_{junction-range}$	The junction temperature range(case1)	-40	-	105	℃
	The junction temperature range (case2)	-40	-	125	℃
$f_{AHB-clock}$	The internal AHB clock frequency range	0	-	48	MHz
$f_{APB-clock}$	The internal APB clock frequency range	0	-	48	MHz
$V_{IO-range}$	The I/Os input voltage range	-0.3	-	5.5	V
	QFN32 power dissipation at T_{range}=85℃ or T_{range}=105℃	-	-	484	mW
	QFN28 power dissipation at T_{range}=85℃ or T_{range}=105℃	-	-	-	mW
$T_{supply-rise}$	VDD/VDDA supply rise rate	0	-	-	uS/V
$T_{supply-fall}$	VDD/VDDA supply fall rate	20	-	-	uS/V
$T_{VDD-POR}$	Supply VDD power on reset threshold	1.84	1.92	2	V
$T_{VDD-fall}$	Supply VDD power down reset threshold	1.80	1.88	1.96	V
$T_{VDDA-fall}$	Supply VDDA power down reset threshold	1.80	1.88	1.96	V
$T_{reset-tempo}$	Reset temporization, $V_{VDD-range}$≤5.5V	-	4.2	10	mS
	Reset temporization, $V_{VDD-range}$≤3.6V	-	4.2	7.5	mS
V_{LVD}	The stage-0 rising threshold voltage of LVD	2.11	2.18	2.25	V
	The stage-0 falling threshold voltage of LVD	2.01	2.08	2.15	V
	The stage-1 rising threshold voltage of LVD	2.20	2.28	2.36	V
	The stage-1 falling threshold voltage of LVD	2.10	2.18	2.26	V
	The stage-2 rising threshold voltage of LVD	2.29	2.38	2.47	V
	The stage-2 falling threshold voltage of LVD	2.19	2.28	2.37	V
	The stage-3 rising threshold voltage of LVD	2.39	2.48	2.57	V
	The stage-3 falling threshold voltage of LVD	2.29	2.38	2.47	V
	The stage-4 rising threshold voltage of LVD	2.48	2.58	2.68	V
	The stage-4 falling threshold voltage of LVD	2.38	2.48	2.58	V

	The stage-5 rising threshold voltage of LVD	2.58	2.68	2.78	V
	The stage-5 falling threshold voltage of LVD	2.48	2.58	2.68	V
	The stage-6 rising threshold voltage of LVD	2.67	2.78	2.89	V
	The stage-6 falling threshold voltage of LVD	2.57	2.68	2.79	V
	The stage-7 rising threshold voltage of LVD	2.77	2.88	2.99	V
	The stage-7 falling threshold voltage of LVD	2.67	2.78	2.89	V

8.4 I/O Pin characteristics

I/O Pin charateristics

Symbol	Description	Min	Typ.	Max.	Units
V_{IH}	Input high level voltage	0.7*VDD	-	-	V
V_{IL}	Input low level voltage	-	-	0.3*VDD	V
$V_{IL-BOOT0}$	Input low level voltage of BOOT0	-	-	0.3*VDD -0.3	V
V_{OH}	Output high level voltage, $\|I_{source-pin}\|$=20mA, VDD≥2.7V	VDD-1.5	-	-	V
	Output high level voltage, $\|I_{source-pin}\|$=6mA	VDD-0.4, VDD-0.45(3)	-	-	V
V_{OL}	Output low level voltage, $\|I_{sunk-pin}\|$=20mA, VDD≥2.7V	-	-	1.1	V
	Output low level voltage, $\|I_{sunk-pin}\|$=6mA	-	-	0.36	V
V_{OL-FMP}	Fast mode plus for I2C, output low level voltage, $\|I_{sunk-pin}\|$=20mA, VDD≥2.7V	-	-	0.4	V
	Fast mode plus for I2C, output low level voltage, $\|I_{sunk-pin}\|$=10mA	-	-	0.3	V
$R_{pull-up}$	I/O pull-up resistance	17	40	140	Ω
$R_{pull-down}$	I/O pull-down resistance	15	40	154	Ω
$I_{leakage}$(1)	Input leakage in digital mode, GND< $V_{IO-range}$ <VDD	-	-	±0.5	uA
	Input leakage in digital model, VDD< $V_{IO-range}$ <VDDA	-	-	±0.5	uA
	Input leakage in analog mode, GND< $V_{IO-range}$ <VDDA	-	-	±0.5	uA
	Input leakage in analog mode, VDD< $V_{IO-range}$ <5V	-	-	5	uA
$I_{leakage}$(2)	Input leakage in digital mode, GND< $V_{IO-range}$ <VDD	-	-	±0.8	uA
	Input leakage in digital model, VDD< $V_{IO-range}$ <VDDA	-	-	±0.8	uA
	Input leakage in analog mode, GND< $V_{IO-range}$ <VDDA	-	-	±0.8	uA
f_{IO}	GPIOx_OSj[1:0]=x0, IO output frequency,CL=50pf	-	-	2	MHz
	GPIOx_OSj[1:0]=01, IO output frequency,CL=50pf	-	-	10	MHz
	GPIOx_OSj[1:0]=11, IO output frequency,CL=30pf, VDD≥2.7V	-	-	50	MHz
	GPIOx_OSj[1:0]=11, IO output frequency,CL=50pf, VDD≥2.7V	-	-	30	MHz
	GPIOx_OSj[1:0]=11, IO output frequency,CL=50pf, VDD＜2.7V	-	-	20	MHz
	Fast mode plus for I2C, output frequency, CL=50pf	-	-	2	MHz
$T_{io-fall}$	GPIOx_OSj[1:0]=x0, IO output fall time,CL=50pf	-	-	12	nS
	GPIOx_OSj[1:0]=01, IO output fall time,CL=50pf	-	-	11	nS
	GPIOx_OSj[1:0]=11, IO output fall time,CL=30pf, VDD≥2.7V	-	-	6	nS
	GPIOx_OSj[1:0]=11, IO output fall time,CL=50pf, VDD≥2.7V	-	-	8	nS
	GPIOx_OSj[1:0]=11, IO output fall time,CL=50pf, VDD＜2.7V	-	-	11	nS
	Fast mode plus for I2C, output fall time, CL=50pf	-	-	11	nS
$T_{io-rise}$	IO output rise time,CL=50pf	-	-	15	nS
	GPIOx_OSj[1:0]=11, IO output rise time,CL=30pf,	-	-	7	nS

	VDD≥2.7V				
	GPIOx_OSj[1:0]=11, IO output rise time,CL=50pf, VDD≥2.7V	-	-	10	nS
	GPIOx_OSj[1:0]=11, IO output rise time,CL=50pf, VDD＜2.7V	-	-	14	nS
T_{ext-pw}	The external-signal pulse width detected by EXTI	10	-	-	nS
$T_{nrst-fp}$	The external-signal pulse width filtered by NRST	-	-	60	nS
$T_{nrst-nfp}$	The external-signal pulse width no-filtered by NRST, $2.7V \le V_{VDD-range} \le 3.6V$	300	-	-	nS
	The external-signal pulse width no-filtered by NRST, $2V \le V_{VDD-range} \le 3.6V$	500	-	-	nS
	The external-signal pulse width no-filtered by NRST, $2V \le V_{VDD-range} \le 5.5V$	390	-	-	nS

(1) $2V \le V_{VDD-range} \le 3.6V$, $2V \le V_{VDDA-range} \le 3.6V$
(2) $2V \le V_{VDD-range} \le 5.5V$, $2V \le V_{VDDA-range} \le 5.5V$
(3) Applied to PF0

8.5 Low power mode wake-up time

Low power mode wake-up time

Symbol	Description	Min	Typ.	Max.	Units
$T_{wk-sleep}$	The sleep mode wake-up time	-	5 system clk	-	uS
$T_{wk-deepsleep1}$	The deepsleep1 mode wake-up time	-	3	5.3	uS
$T_{wk-deepsleep2}$	The deepsleep2 mode wake-up time	-	4	7.2	uS
$T_{wk-powerdown}$	The powerdown mode wake-up time	-	57	157	uS

8.6 RC oscillator characteristics

HRC characteristics

Symbol	Description	Min	Typ.	Max.	Units
f_{HRC}	The frequency of HRC	-	8	-	MHz
$TRIM_{HRC}$	HRC user trimming step	-	-	1	%
$Duty_{HRC}$	The duty cycle of HRC	48	-	52	%
$f_{voltage-HRC}$	Voltage characteristics of HRC frequency	-0.5	-	0.5	%
$f_{temp-HRC}$	temperature characteristics of HRC frequency	-2	-	2	%
$f_{accuracy-HRC}$	Accuracy of HRC frequency	-1	-	1	%
T_{setup_HRC}	The setup time of HRC	0.14	-	1.2	uS
I_{pd-HRC}	The power dissipation of HRC	44	66	102	uA

HRC14 characteristics

Symbol	Description	Min	Typ.	Max.	Units
f_{HRC14}	The frequency of HRC14	-	14	-	MHz
$TRIM_{HRC14}$	HRC14 user trimming step	-	-	1	%
$Duty_{HRC14}$	The duty cycle of HRC14	47	-	53	%
$f_{voltage-HRC14}$	Voltage characteristics of HRC14 frequency	-0.5	-	0.5	%
$f_{temp-HRC14}$	temperature characteristics of HRC14 frequency	-2	-	2	%
$f_{accuracy-HRC14}$	Accuracy of HRC14 frequency	-1	-	1	%
T_{setup_HRC14}	The setup time of HRC14	0.09	-	0.5	uS
$I_{pd-HRC14}$	The power dissipation of HRC14	64	96	152	uA

LRC characteristics

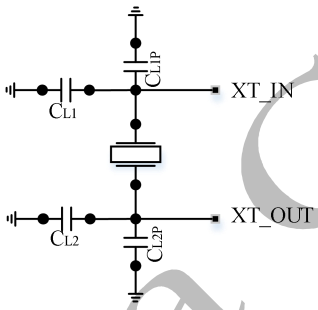
Symbol	Description	Min	Typ.	Max.	Units
f_{LRC}	The frequency of LRC	30	40	50	KHz
T_{setup_LRC}	The setup time of LRC	-	-	84	uS
I_{pd-LRC}	The power dissipation of LRC	-	0.71	1.27(1), 2.47(2)	uA

(1) VDDA=3.3V, -40℃ ≤ T_{range} ≤ 105℃
(2) VDDA=5.5V, -40℃ ≤ T_{range} ≤ 105℃

8.7 Crystal oscillator characteristics

Figure 10 shows the crystal and the loading and parasitic capacitances of crystal oscillator. Both C_{L1} and C_{L2} are the capacitance devices on the PCB board. Both C_{L1P} and C_{L2P} are parasitic capacitance on PCB board and package.

Figure 10 The loading and parasitic capacitances of crystal oscillator



CL(CL_{LXT} or CL_{HXT}) is the crystal load capacitance. The specified crystal has standard load capacitance.

$$C'_{L1} = C_{L1} + C_{L1P}$$
$$C'_{L2} = C_{L2} + C_{L2P}$$
$$CL = C'_{L1} * C'_{L2} / (C'_{L1} + C'_{L2})$$

HXT characteristics

Symbol	Description	Min	Typ.	Max.	Units
f_{HXT-IN}	Cystal oscillator frequency	4	8	32	MHz
I_{pd-HXT}	During startup time	-	1.8	6.5	mA
	VDD=3.3V, Rm=30Ω, CL=10pF@8MHz	0.12	0.22	0.45	mA
	VDD=3.3V, Rm=45Ω, CL=10pF@8MHz	0.13	0.24	0.46	mA
	VDD=3.3V, Rm=30Ω, CL=5pF@32MHz	0.21	0.34	0.6	mA
	VDD=3.3V, Rm=30Ω, CL=10pF@32MHz	0.33	0.46	0.7	mA
	VDD=3.3V, Rm=30Ω, CL=20pF@32MHz	0.58	0.72	0.87	mA
gm_{HXT}	The oscillator transconductance of HXT, HXTDRV[1:0]=00, low drive	0.7	-	16.4	mA/V
	The oscillator transconductance of HXT, HXTDRV[1:0]=01, medium low drive	5.0	-	27.3	mA/V
	The oscillator transconductance of HXT, HXTDRV[1:0]=10, medium high drive	6.2	-	32.6	mA/V
	The oscillator transconductance of HXT, HXTDRV[1:0]=11, high drive	13.1	-	43.4	mA/V
CL_{HXT}	The Crystal load capacitance of HXT	5	10	20	pF
T_{setup}	HXT setup time	-	1	-	mS

8.8 External clock characteristics

HXT external clock characteristics

Symbol	Description	Min	Typ.	Max.	Units
F_{HXT-IN}	External clock source frequency	-	8	32	MHz
V_{HXT-L}	Input pin low level voltage of HXT external source clock	GND	-	0.3*VDD	V
V_{HXT-H}	Input pin high level voltage of HXT external source clock	0.7*VDD	-	VDD	V
$T_{width-HXT}$	Input pin high or low time of HXT external source clock	15	-	-	nS
$T_{rise-HXT}$	Input pin rise time of HXT external source clock	-	-	20	nS
$T_{fall-HXT}$	Input pin fall time of HXT external source clock	-	-	20	nS

8.9 PLL characteristics

PLL characteristics

Symbol	Description	Min	Typ.	Max.	Units
f_{PLL-IN}	Frequency of PLL input clock	1	8	24	MHz
$Duty_{PLL-IN}$	Duty cycle of PLL input clock	40	-	60	%
$f_{PLL-OUT}$	Frequency of PLL output clock	16	-	48	MHz
T_{lock}	The lock time of PLL	-	-	200	uS
$jitter_{PLL}$	Cycle to cycle jitter	-	-	300	pS

8.10 Power consumption

Power consumption characteristics of run and sleep mode

Run mode	Code execute	conditions	f_{HCLK} (MHz)	IVDD (peripherals on) (mA)			IVDD (peripherals off) (mA)			IVDDA (uA)		
				Typ(1)	Max(2)	Max(3)	Typ(1)	Max(2)	Max(3)	Typ(1)	Max(2)	Max(3)
run	flash	HXT bypass，PLL on	48	15.6	20.5		9.13	11.2		316	430	
run	flash	HXT bypass，PLL on	32	10.41	12.6		6.82	8.4		240		
run	flash	HXT bypass，PLL on	24	8.47	10		5.69	6.9		207	301	
run	flash	HXT bypass，PLL off	8	4	7.6		3.1	4		2.86		
run	flash	HXT bypass，PLL off	1	2.1	3		2	2.9		2.86		
run	flash	HRC，PLL on	48	14.6			9.11			376		
run	flash	HRC，PLL on	32	10.44			6.86			302		
run	flash	HRC，PLL on	24	8.5			5.67			269		
run	flash	HRC，PLL off	8	4.06			3.08			61.5	104	
run	SRAM	HXT bypass，PLL on	48									
run	SRAM	HXT bypass，PLL on	32									
run	SRAM	HXT bypass，PLL on	24									
run	SRAM	HXT bypass，PLL off	8									
run	SRAM	HXT bypass，PLL off	1									

run	SRAM	HRC，PLL on	48									
run	SRAM	HRC，PLL on	32									
run	SRAM	HRC，PLL on	24									
run	SRAM	HRC，PLL off	8									
sleep	-	HXT bypass，PLL on	48	9.43			3.45			316		
sleep	-	HXT bypass，PLL on	32	7			2.92			240		
sleep	-	HXT bypass，PLL on	24	5.74			2.67			207		
sleep	-	HXT bypass，PLL off	8	3.07			2.11			2.86		
sleep	-	HXT bypass，PLL off	1	2.02			1.91			2.86		
sleep	-	HRC，PLL on	48	9.48			3.42			376		
sleep	-	HRC，PLL on	32	7.05			2.89			302		
sleep	-	HRC，PLL on	24	5.78			2.64			269		
sleep	-	HRC，PLL off	8	3.12			2.09			61.5		

Power consumption characteristics of deepsleep and power down mode

Run mode	Code execute	conditions	f_{HCLK} (MHz)	IVDD (peripherals on) (uA)			IVDD (peripherals off) (uA)			IVDDA (uA)		
				Typ(1)	Max(2)	Max(3)	Typ(1)	Max(2)	Max(3)	Typ(1)	Max(2)	Max(3)
deepsleep1	-	VDDA monitor on	-	21.3	42	-				2.73	15.8	
deepsleep1	-	VDDA monitor off	-	21.3	42	-				1.24		
deepsleep2	-	VDDA monitor on	-	5.6	21	-				2.71	15.8	
deepsleep2	-	VDDA monitor off	-	5.6	21	-				1.21		
powerdown	-	LRC on, FWDT on VDDA monitor on	-	1.2	-	-				3.6		
powerdown	-	LRC off, FWDT off VDDA monitor on	-	1.0	-	-				2.3		
powerdown	-	LRC on, FWDT on VDDA monitor off	-	1.2	-	-				2.5		
powerdown	-	LRC off, FWDT off VDDA monitor off	-	1.0	-	-				1.2		

(1) VDD=VDDA=VBAT=3.3V, T_{range}=25℃
(2) VDD=VDDA=VBAT=3.6V, T_{range}=105℃
(3) VDD=VDDA=VBAT=5.5V, T_{range}=105℃

8.11 Internal reference voltage

Internal reference voltage characteristics

Symbol	Description	Min	Typ.	Max.	Units
V_{refint}	Internal reference voltage	1.19	1.22	1.25	V
$deltV_{refint}$	Internal reference voltage variation over the temperature range	-	-	11	mV
Tc	Temperature coefficient	-60	-	60	ppm/^{0}C

8.12 ADC characteristics

ADC characteristics

Symbol	Description	Min	Typ.	Max.	Units
VDDA	VDDA power supply range for ADC	2.4	-	5.5	V
$I_{VDDA-ADC}$	VDDA power consumption of the ADC, Autoff=0, VDDA=3.3V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	0.6	-	14	MHz
T_{sample}	Sampling time of ADC	1.5	-	236.5	1/ f_{ADC}
$T_{convert-time}$	Convert time of ADC	14	-	252	1/ f_{ADC}
$T_{swtich-on}$	Switch-on time of ADC	-	-	1	uS
$T_{calibration}$	Calibration time of ADC	-	83	-	1/ f_{ADC}
$V_{range-input}$	The input voltage range of ADC	0	-	VDDA	V
$C_{input-ADC}$	The input capacitor of ADC	-	-	8	pF
$R_{ext-input}$	External input impedance	-	-	50	kΩ
B_{-3dB}	Input signal -3dB bandwidth		50		kHz
Iso_{input}	Input signal isolation	-	-	-100	dB
Resolution	The ADC programmable resolution	6	-	12	Bit
$ERR_{absolute}$	ADC absolute error	-	±3.3	±4	LSB
INL	ADC INL, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA≥2.7V	-	±1.2	±2.3	LSB
	ADC INL, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA=2.4V	-	±1.5	±3.5	LSB
DNL	ADC DNL, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA≥2.7V	-	±0.7	±1.3	LSB
	ADC DNL, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA=2.4V	-	±2.8	±3	LSB
Offset	ADC offset, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA≥2.7V	-	±1.9	±2.8	LSB
	ADC offset, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA=2.4V	-	±2	±3.5	LSB
ERR_{Gain}	ADC gain error, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA≥2.7V	-	±2.8	±3	LSB
	ADC gain error, f_{ADC}=14MHz, $R_{ext-input}$<10kΩ, VDDA=2.4V	-	±2.8	±3	LSB

$R_{ext-input}$ max for f_{ADC}=14MHz

T_{sample}(1/ f_{ADC})	T_{sample}(uS)	Max. $R_{ext-input}$(kΩ)
1.5	0.11	0.15
2.5	0.18	0.4
8.5	0.61	5.9
14.5	1.04	11.4
29.5	2.11	25.2
42.5	3.04	37.2
56.5	4.04	50
71.5	5.11	-
239.5	17.1	-

8.13 Temperature sensor characteristics

Temperature sensor characteristics

Symbol	Description	Min	Typ.	Max.	Units
L_{temp}	Linearity of temperature sensor	-	±1	±2	℃
S_{temp}	Average slope of temperature sensor voltage	4.35	4.47	4.60	mV/℃
V_{temp30}	Temperature sensor voltage of 30±5℃	1.37	1.43	1.50	V
$T_{start-temp}$	The startup time of Temperature sensor block	-	-	6	uS
$T_{sample-temp}$	The ADC sampling time of temperature sensor	4	-	-	uS

8.14 Flash characteristics

Flash characteristics

Symbol	Description	Min	Typ.	Max.	Units
T_{prog}	16-bit program time	33.6	35	36.4	uS
	32-bit program time	67.2	70	72.8	uS
T_{erase}	Page(1 kbytes) erase time	17.6	18.3	19.1	mS
$T_{mass-erase}$	Mass erase time	29.1	30.3	31.6	mS
$Cyc_{endurance}$	Sector endurance	20,000	-	-	Cycles
$T_{retention}$	Data retention, Trange =25℃	100	-	-	Year
	Data retention, Trange =85℃	20	-	-	Year
	Data retention, Trange = 105℃	10	-	-	Year

8.15 Timers characteristics

TIMx characteristics

Symbol	Description	Min	Typ.	Max.	Units
$T_{resolution}$	Timer resolution time	-	$T_{TIMx\ CLK}$	-	nS
$f_{ext-clk}$	Timer external clock frequency on CHx	-	$T_{TIMx\ CLK}/2$	-	MHz
$T_{max-count}$	Maximum period of 16-bit timer	-	$2^{16} * T_{TIMx\ CLK}$	-	nS
	Maximum period of 32-bit timer	-	$2^{32} * T_{TIMx\ CLK}$	-	nS

FWDT characteristics

Pre-divider	PDIV[2:0]	Min timeout UVAL[11:0]=0x000	Max timeout UVAL[11:0]=0x000	Units
/4	0	$4 * T_{40K}$	$16384 * T_{40K}$	mS
/8	1	$8 * T_{40K}$	$32768 * T_{40K}$	mS
/16	2	$16 * T_{40K}$	$65536 * T_{40K}$	mS
/32	3	$32 * T_{40K}$	$131072 * T_{40K}$	mS
/64	4	$64 * T_{40K}$	$262144 * T_{40K}$	mS
/128	5	$128 * T_{40K}$	$524288 * T_{40K}$	mS
/256	6 or 7	$256 * T_{40K}$	$1048576 * T_{40K}$	mS

WWDT characteristics

Pre-divider	PDIV[1:0]	Min timeout value	Max timeout value	Units
/1	0	$4096 * T_{PLCK}$	$262144 * T_{PLCK}$	mS
/2	1	$8192 * T_{PLCK}$	$524288 * T_{PLCK}$	mS
/4	2	$16384 * T_{PLCK}$	$1048576 * T_{PLCK}$	mS
/8	3	$32768 * T_{PLCK}$	$2097152 * T_{PLCK}$	mS

8.16 SPI characteristics

SPI characteristics

Symbol	Description	Min	Typ.	Max.	Units
f_{SCK}	SPI clock frequency in master mode (VDD ≥ 3V,Trange≤85 ℃)	-	-	18	MHz
	SPI clock frequency in slave mode (VDD ≥ 3V,Trange≤85 ℃)	-	-	18	MHz
	SPI clock frequency in master mode (VDD ≥ 3V, 85 ℃<Trange≤105 ℃)	-	-	15	MHz
	SPI clock frequency in slave mode	-	-	15	MHz

	(VDD ≥ 3V, 85 ℃<Trange≤105 ℃)				
	SPI clock frequency in master mode (VDD ≥ 2V, Trange≤105 ℃)	-	-	13	MHz
	SPI clock frequency in slave mode (VDD ≥ 2V, Trange≤105 ℃)	-	-	13	MHz
$T_{rise-SCK}$	The rise time of SPI clock with 15pf capacitive load	-	-	6	nS
$T_{fall-SCK}$	The fall time of SPI clock with 15pf capacitive load	-	-	6	nS
$T_{setup-NSS}$	NSS setup time in slave mode	50	-	-	nS
$T_{hold-NSS}$	NSS hold time in slave mode	$2*T_{pclk}+10$	-	-	nS
$T_{width-SCK}$	High or low time of SPI clock, f_{PCLK}=36MHz, PCLKPDIV=4	$2*T_{pclk}-3$	-	$2*T_{pclk}+1$	nS
$T_{setup-din}$	Data input setup time in master mode	4	-	-	nS
	Data input setup time in slave mode	5	-	-	nS
$T_{hold-din}$	Data input hold time in master mode	4	-	-	nS
	Data input hold time in slave mode	5	-	-	nS
$T_{access-dout}$	Data output access time in slave mode, f_{PCLK}=20MHz	0	-	32	nS
$T_{disable-dout}$	Data output disable time in slave mode	0	-	32	nS
$T_{valid-dout}$	Data output valid time in slave mode after enable edge	-	-	35	nS
	Data output valid time in master mode after enable edge	-	-	6	nS
$T_{hold-dout}$	Data output hold time in slave mode after enable edge	11.5	-	-	nS
	Data output hold time in master mode after enable edge	2	-	-	nS
$Duty_{SCK}$	Slave input clock duty cycle of SPI	25	-	75	nS

Figure 11 SPI timing – slave mode (1)

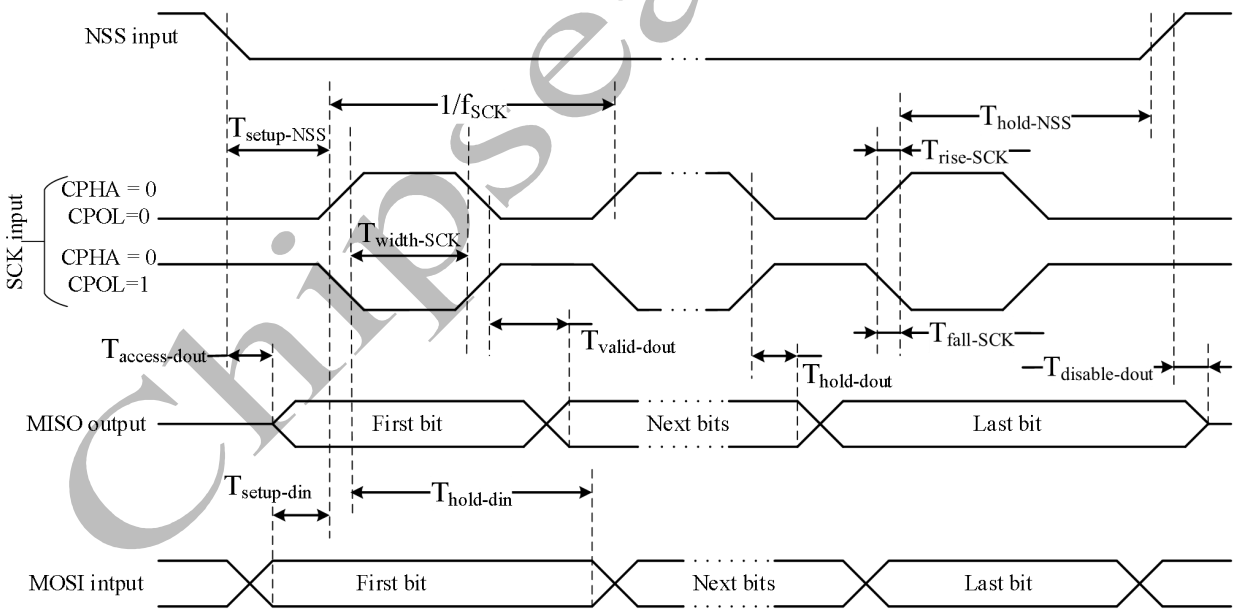


Figure 12 SPI timing – slave mode (2)

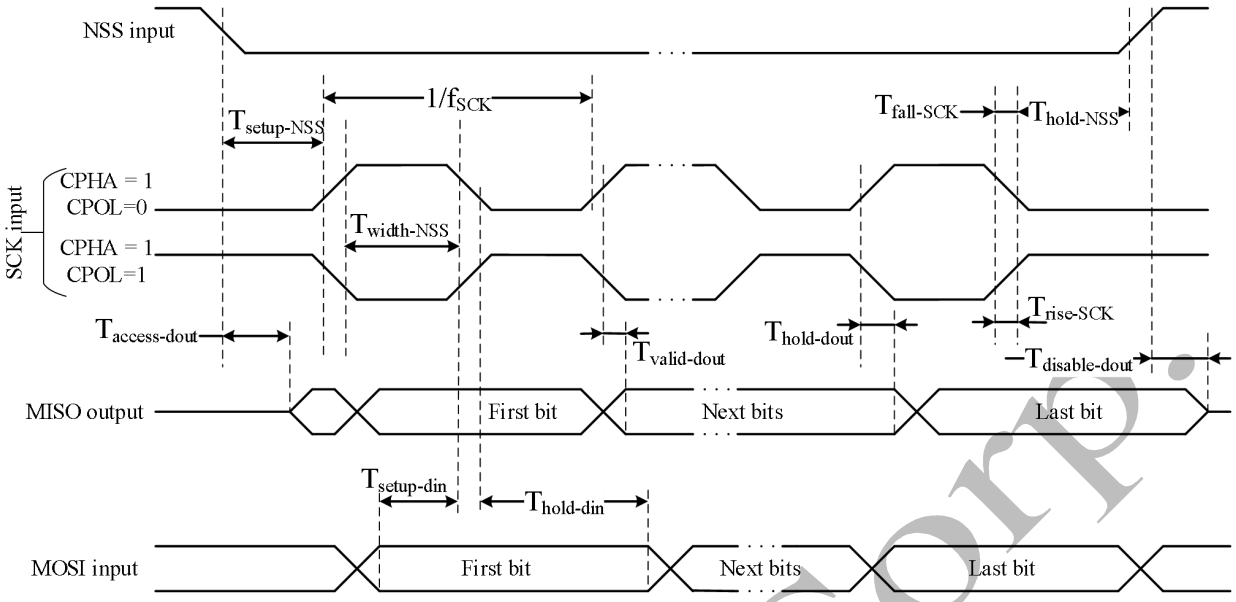
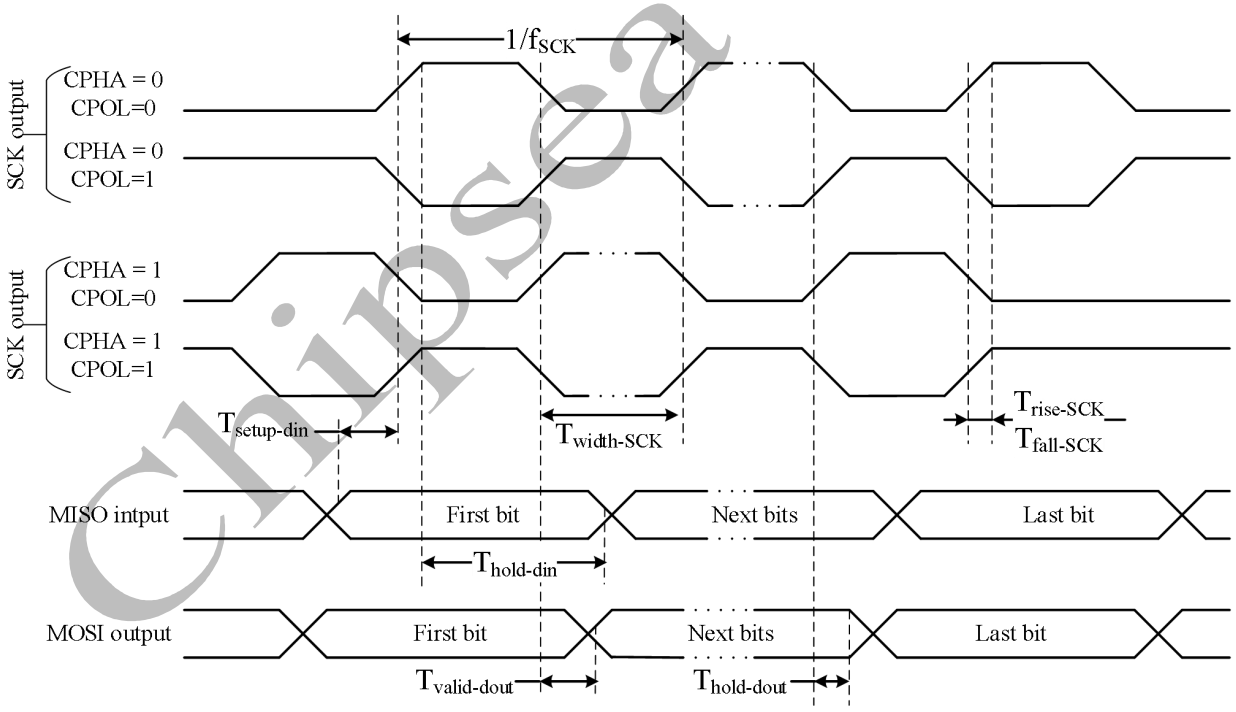


Figure 13 SPI timing – master mode



8.17 I2C characteristics

I2C characteristics

I2C mode	Max rate	Units
Standard mode	100	Kbit/S
Fast mode	400	Kbit/S

I2C analog filter characteristics

Symbol	Description	Min	Typ.	Max.	Units
T_{I2C-fp}	The external-signal pulse width filtered by I2C analog filter		-	50	nS
$T_{I2C-nfp}$	The external-signal pulse width no-filtered by I2C analog filter	160	-	-	nS

8.18 ESD characteristics

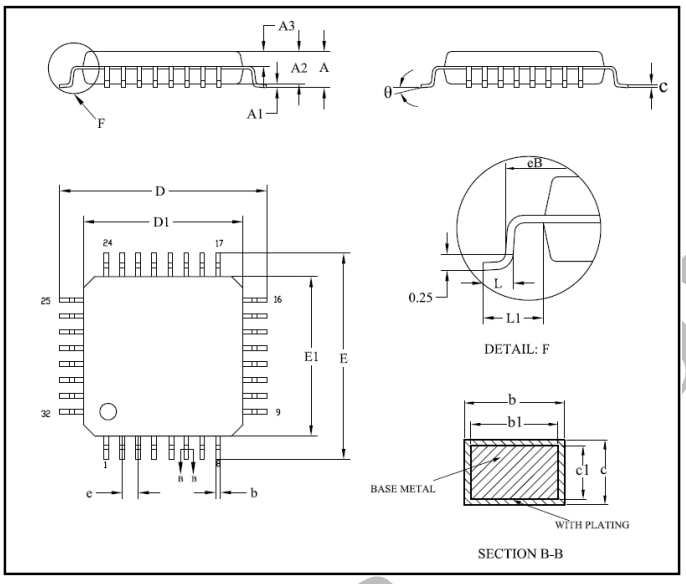
ESD characteristics

Symbol	Description	Class	Value	Units
$V_{ESD-HBM}$	Electrostatic discharge voltage of human body model, Based on MIL-STD-883E, Trange =23±5℃ Relative humidity: 55%±10%(RH)	3A	≥4000	V
V_{ESD-MM}	Electrostatic discharge voltage of machine model, Based on JEDEC EIA/JESD22-A115, Trange =23±5℃ Relative humidity: 55%±10%(RH)	C	≥400	V
$V_{ESD-CDM}$	Electrostatic discharge voltage of charge device model, Based on JEDEC EIA/JESD22-C101F, Trange =23±5℃ Relative humidity: 55%±10%(RH)	C2	≥500	V
$I_{latchup}$	Electrostatic discharge voltage of machine model, Based on JEDEC STANDARD NO.78C SEPTMBER 2010, Trange =105±5℃ Relative humidity: 55%±10%(RH)	II	≥200	mA

9 Packaging information

9.1 LQFP32

Figure 14 LQFP32 package outline



LQFP32 package dimensions

Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

LQFP32 Package thermal characteristics

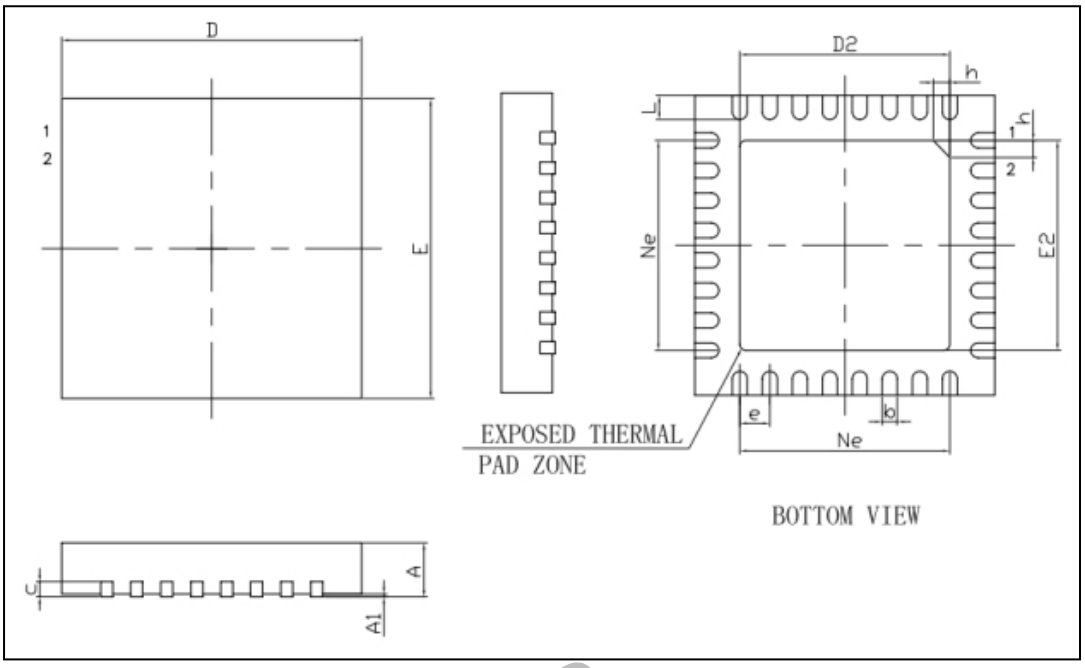
Name	Value	Unit
Θ_{JA}, by 2S2P	54	℃/W
Θ_{JC}	18.2	℃/W

LQFP32 Moisture Sensitivity

Name	Level
Moisture sensitivity Level	MSL3

9.2 QFN32(5×5×0.75-e=0.50)

Figure 15 QFN32 package outline



QFN32L package dimensions

Symbol	Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.19	0.24	0.29
b1	0.18REF		
c	0.152REF		
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
Ne	3.50BSC		
L	0.35	0.40	0.45
K	0.30	0.35	0.40
h	0.30	0.35	0.40

QFN32 Package thermal characteristics

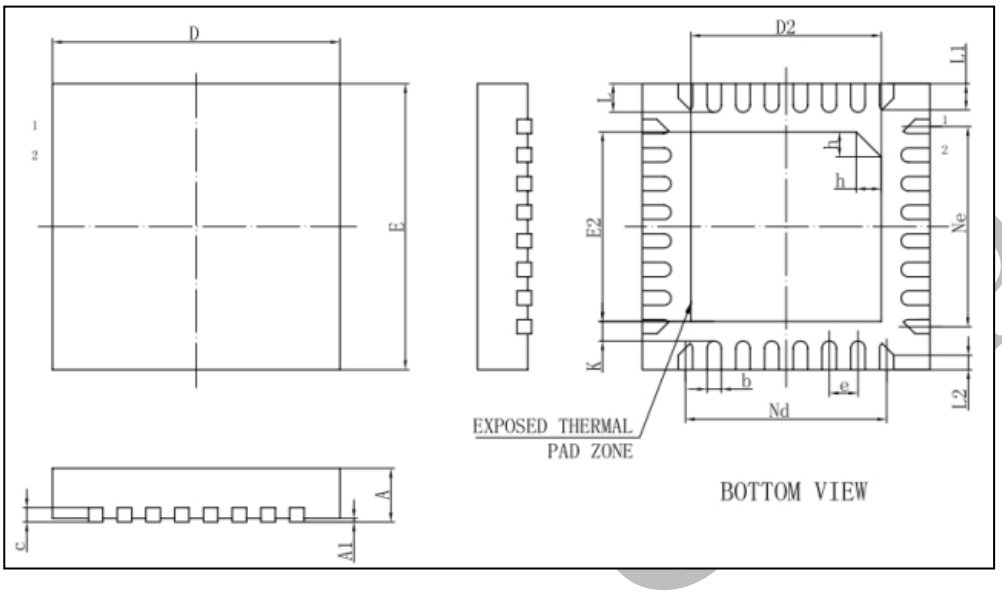
Name	Value	Unit
Θ_{JA}, by 2S2P	TBD	℃/W
Θ_{JC}	TBD	℃/W

QFN32 Moisture Sensitivity

Name	Level
Moisture sensitivity Level	MSL3

9.3 QFN32(4×4×0.75-e=0.4)

Figure 16 QFN32 package outline



QFN32 package dimensions

Symbol	Millimeter		
	Min		Min
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40

QFN32 Moisture Sensitivity

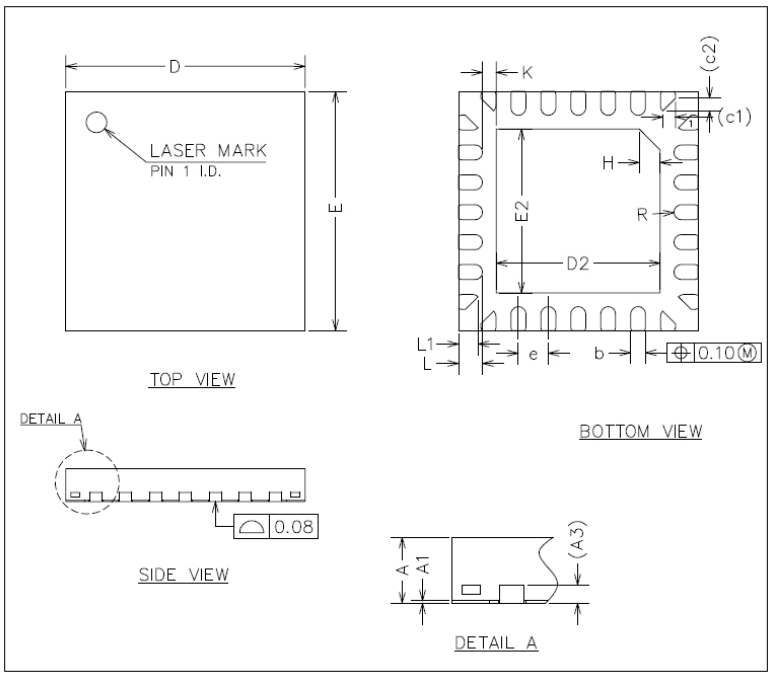
Name	Value	Unit
Θ_{JA}, by 2S2P	TBD	℃/W
Θ_{JC}	TBD	℃/W

QFN32 Moisture Sensitivity

Name	Level
Moisture sensitivity Level	MSL3

9.4 QFN28

Figure 17 QFN28 package outline



QFN28 package dimensions

Symbol	Millimeter		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.15REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.64	2.74	2.84
E2	2.64	2.74	2.84
e	0.40	0.50	0.60
H		0.35REF	
K	0.13	0.23	0.33
L	0.30	0.40	0.50
L1	0.20	0.30	0.40
R	0.10	-	-
c1	-	0.21	-
c2	-	0.21	-

QFN28 Package thermal characteristics

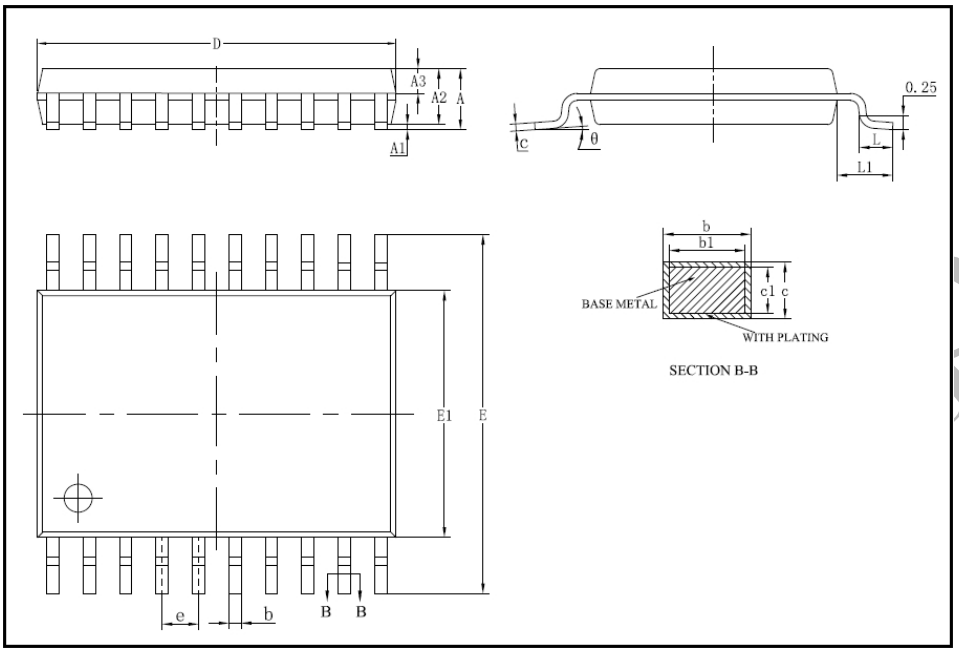
Name	Value	Unit
Θ_{JA}, by 2S2P	50.80	℃/W
Θ_{JC}	19.7	℃/W

QFN28 Moisture Sensitivity

Name	Level
Moisture sensitivity Level	MSL3

9.5 TSSOP20

Figure 18 TSSOP20 package outline



TSSOP20 package dimensions

Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

TSSOP20 Package thermal characteristics

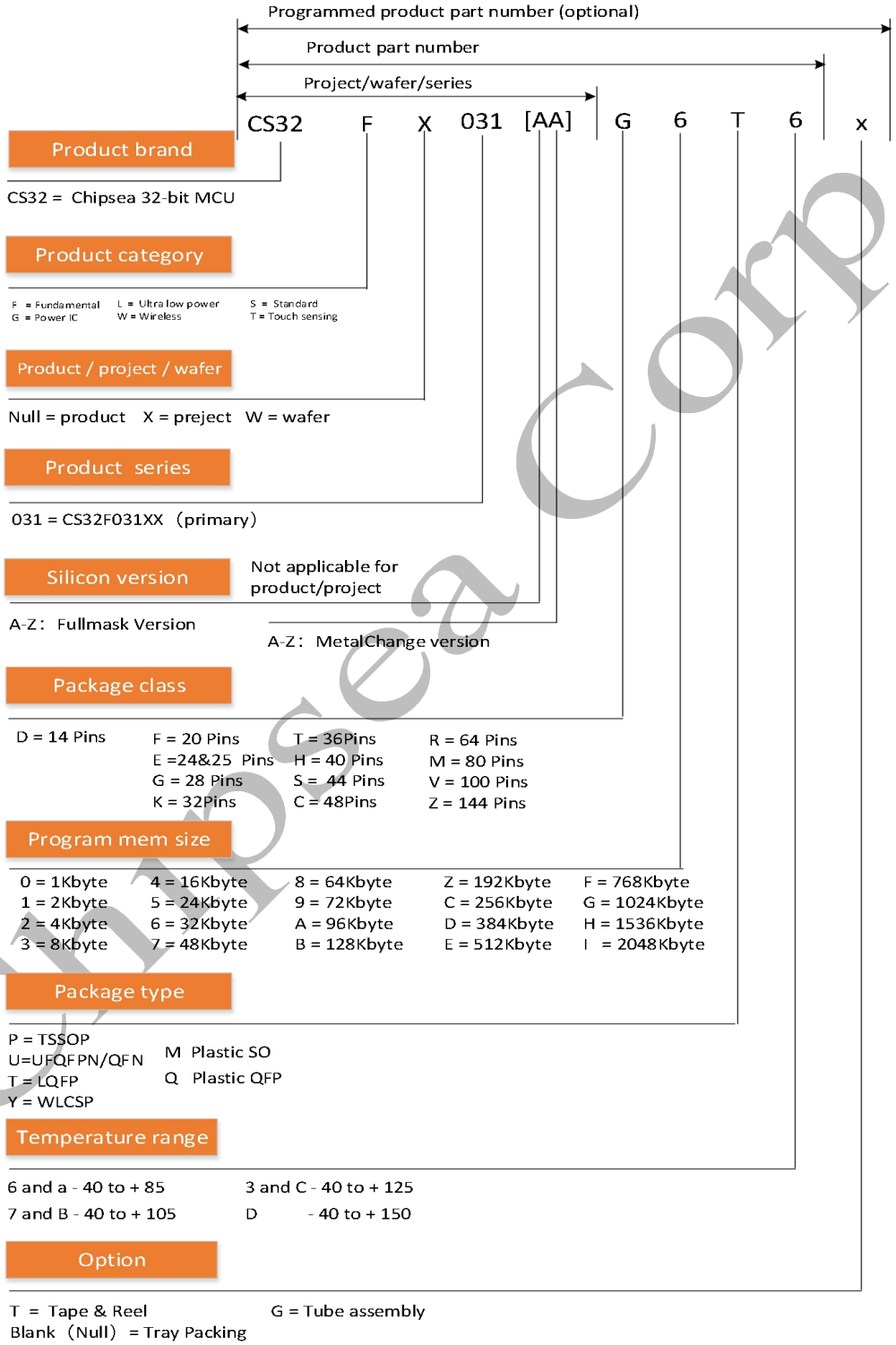
Name	Value	Unit
Θ_{JA}, by 2S2P	103	℃/W
Θ_{JC}	35.7	℃/W

TSSOP20 Moisture Sensitivity

Name	Level
Moisture sensitivity Level	MSL3

10 Product naming rules

10.1 Product model description



10.2 Product printing mark

Marking instructions:	
1	Front pin Pin1 mark;
2	The first row on the front (Chipsea);
3	The second line on the front (product model);
4	The third line on the front (yywwxxx) is the main batch number. The two digits YY on the left are taken from the last two digits of the Gregorian calendar year, and the two digits WW in the middle are taken from the calendar weeks of the current year. If there are less than two digits, 0 is added on the left, and the three digits XXX on the right are variables, which shall be subject to the order specification;
5	Font is "Arial";
6	The printing method is laser positive printing

For example, the marking of F035K6U6 is as follows:

11 Ordering information

Ordering information

Part number	Lead Count	Flash	Package	Pack Type	Package Qty.	Operating temperature
CS32F035K6U6	32	32KB	QFN32(4×4×0.75-e=0.40)	Tray	4900	-40°C ~85°C
CS32F035K6U6T	32	32KB	QFN32(4×4×0.75-e=0.40)	Tape & Reel	3000	-40°C ~85°C
CS32F036F6P7	20	32KB	TSSOP20	Tube	6000	-40°C ~105°C
CS32F036G6U7	28	32KB	QFN28(4×4×0.55-e=0.50)	Tray	4900	-40°C ~105°C
CS32F036K6U7	32	32KB	QFN32(5×5×0.75-e=0.50)	Tray	4900	-40°C ~105°C
CS32F036K6U7T	32	32KB	QFN32(5×5×0.75-e=0.50)	Tape & Reel	3000	-40°C ~105°C
CS32F036K6T7	32	32KB	LQFP32	Tray	2500	-40°C ~105°C

12 Errata

Please refer to the document “Errata of CS32F03X”.

13 Abbreviations

Abbreviations	Description
ADC	Analog to Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machines
Cortex	Embedded Microcontroller Processors
CPU	Central Processing Unit
CRC	Cyclic redundancy check
DMA	Direct Memory Access
ESD	Electrostatic Discharge
ETR	External trigger input
EXTI	Extended interrupt/event controller
FLASH	Floating gate transistor memory
FWDT	Free watchdog timer
GPIO	General Purpose Input/Output
HXT	External high speed crystal oscillator
HRC	Internal high speed RC oscillator
I2C	Inter-integrated circuit
I2S	Inter-IC sound
IR	Infrared radiation
IrDA	Infrared data association
ISO7816	International Organization for Standardization （ISO）7816
LIN	Local interconnect network
LRC	Internal low speed RC oscillator
LSB	Last Significant Bit
LVD	Low voltage detector
LXT	External low speed crystal oscillator
MCU	Microcontroller Unit
MISO	Master In / Slave Out
MOSI	Master Out / Slave In
NRST	Negative reset
NSS	Slave Select
NVIC	Nested vectored interrupt controller
PCB	Printed Circuit Board
PDR	Power-down reset
PLL	Phase locked loop
PMBus	Power Management Bus
POR	Power-on reset
RAM	Random Access Memory
RTC	Real-time clock
SCK	Serial Clock
SD	Serial Data
SMBus	System Management Bus
SPI	Serial peripheral interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
TIM	TIMER

TS	Temperature Sensor
USART	Universal synchronous/asynchronous receiver/transmitter
WS	Word Select
WWDT	Window watchdog timer

14 Sales and service

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