CMOS single-chip 8-bit MCU with 12-bit A/D converter

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 8Kbytes Flash Code Memory
  - 512bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator (±1.5%, T_A= 0 ~ +50°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (10 inputs)
  - UART 8-bit x 1-ch
  - SPI 8-bit x 1-ch
  - I2C 8-bit x 1-ch
- **I/O and Packages**
  - Up to 18 Programmable I/O lines with 20 SOP
  - 20 SOP, 20 PDIP, 20 QFN, 16 SOPN
  - Pb-free package
- **Operating Conditions**
  - 1.8V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Small Home Appliance

MC96F8208S

Data Sheet

V 1.15

Revised 11 June, 2018

Revision history

Version	Date	Revision list
0.0	2013.01.02	Published this book.
0.1	2013.01.24	Remove a Package Type “MC96F8208SV (16-DIP)”
0.2	2013.03.26	Add a Package Type “MC96F8208SU (20-QFN)”
1.0	2013.06.26	Add content related to “MC96F8208 EVA(MC96F8208OCD/OB/OU/OM)” Add a Programmer Type “PGMplusLC Writer”
1.1	2013.07.15	Add a content of IOH/IOL in different table. Remove a Package Type “MC96F8208SM (16-SOP)” Remove content related to “MC96F8208OM(EVA)”
1.2	2014.02.27	Fix the byte count of instruction “DJNZ Rn,rel” Add a current unit at DC Characteristics(IDD1,IDD2,IDD3,IDD4,IDD5) Add a Package Type “MC96F8208SMN (16-SOP)”
1.3	2014.03.24	AVREF range changed from 1.8V~VDD to 2.7V~VDD.
1.4	2014.04.14	AVREF range changed from 2.7V~VDD to 1.8V~VDD. Add “Instructions on how to use the input port.” on appendix.
1.5	2014.07.09	Remove a Programmer Type “PGMplusLC Writer” Change ‘Read Protection’ to ‘Code Read Protection’ in Configure Option. Change ‘Hard-Lock’ to ‘Code Write Protection’ in Configure Option. Change ‘RESETB port with a pull-up resistor’ to ‘Enable RESETB pin’ in Configure Option. Change ‘Protection Area Enable/Disable’ to ‘Specific Area Write Protection’ in Configure Option. Change ‘Protection Area Size Select’ to ‘Select Specific Area for Write Protection’ in Configure Option.
1.6	2014.11.05	Add contents of Flash, “Protection for Invalid Erase/Write”.
1.7	2015.02.03	Add a Package Type “MC96F8208SR (20-TSSOP)” Modify contents of Interrupt sequence flow
1.8	2015.03.10	Modify the Figure 4.1 20-Pin SOP Package Modify the Figure 11.32 A/D Analog Input Pin with Capacitor
1.9	2015.04.09	Add a note at P0, P1, P2, P3, EIFLAG0, EIFLAG1 register description and SFR map.
1.10	2015.05.11	Add a chapter “17.3 ESD Test Method”.
1.11	2016.04.07	Add Flash Data Retention Time in Chapter 7.14 Internal Flash Rom Characteristics Add a chapter 7.20 Recommended Circuit and Layout with SMPS Power. Modify the program tips in Chapter 15. Flash Memory. Add an appendix about “Flash Protection for invalid Erase/Write” Fixed typos.
1.12	2016.10.27	Correct the 20QFN Package Diagram.
1.13	2017.01.20	Added the note on the flash memory erase and write in Chapter 15. Flash Memory. Updated OCD dongle image and writing tool images in Chapter 1.3 Development tools. Fixed typos of I2C Status Register in Chapter 11.12 I2C.
1.14	2017.03.24	Updated Package diagrams in Chapter 4. Package Diagram.
1.15	2018.06.11	Revised this book. Add Device Nomenclature. Updated Package diagrams in Chapter 4. Package Diagram. Fixed typos.

Version 1.15

Published by FAE team

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1 Overview

1.1. Description

The MC96F8208S is advanced CMOS 8-bit microcontroller with 8 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 8k bytes of FLASH, 256 bytes of IRAM, 256 bytes of XRAM , general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F8208S also supports power saving modes to reduce power consumption.

Device Name	EVA	FLASH	XRAM	IRAM	Package
MC96F8208SD	MC96F8208OCD	8 Kbytes FLASH	256 bytes	256 bytes	20 SOP
MC96F8208SR	MC96F8208OR				20 TSSOP
MC96F8208SB	MC96F8208OB				20 PDIP
MC96F8208SU	MC96F8208OU				20 QFN
MC96F8208SM	MC96F8208OM				16 SOPN

Table 1.1 Ordering Information of MC96F8208S

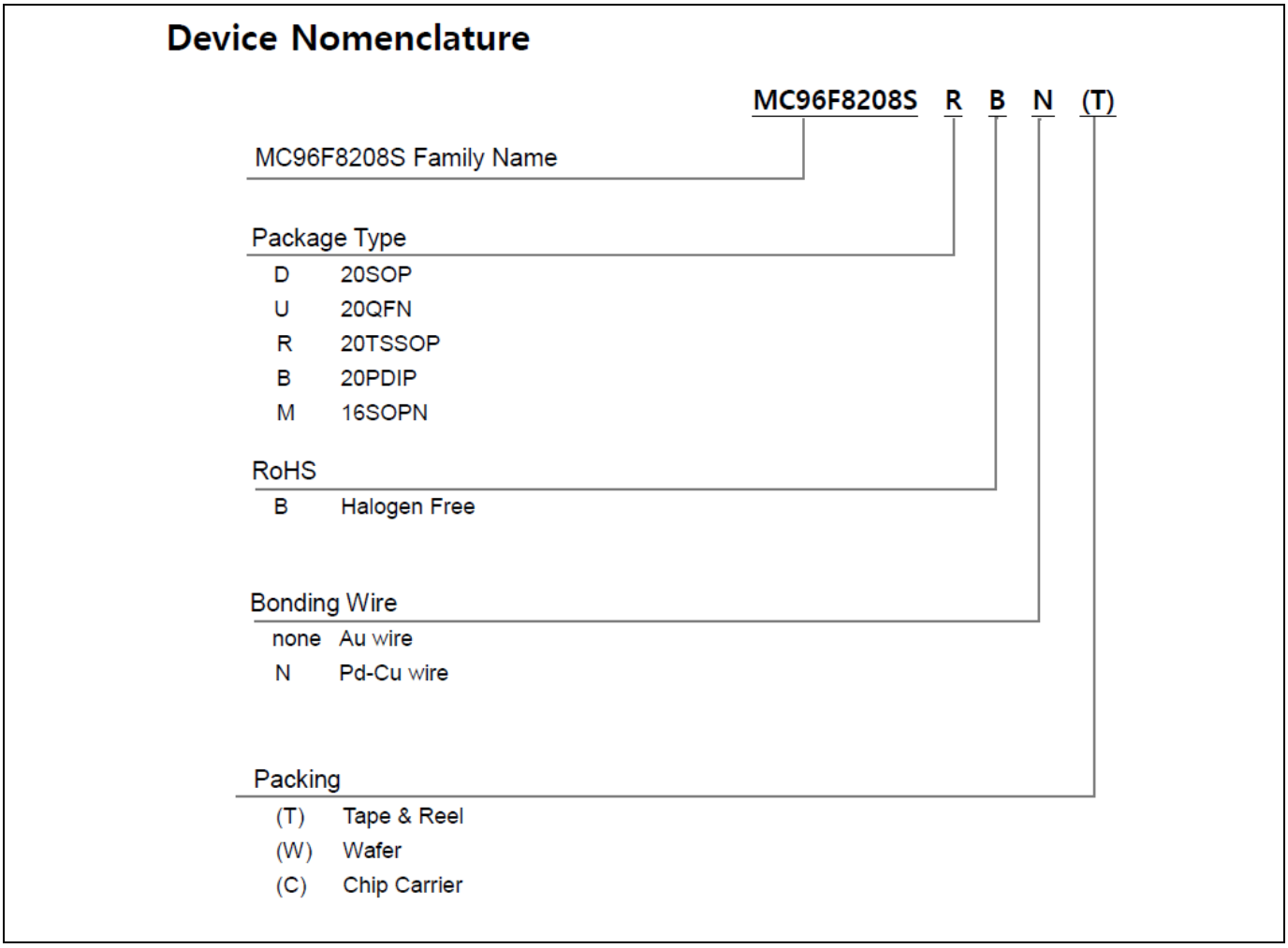


Figure 1.1 Device Nomenclature of MC96F8208S

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 8 Kbytes Flash with self read/write capability
  - In-System Programming(ISP)
  - Endurance : 10,000 times(Sector 0~247)
    100,000 times(Sector 248~255)
  - Retention : 10 years
- **256bytes IRAM**
- **256bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 18 Ports
    (P0[3:0], P1[6:1], P2[5:4], P3[7:5/2:0])
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit× 1-ch
  - Watch Dog Timer (WDT) 8-bit× 1-ch
  - 5kHz internal RC oscillator
  - 8-bit× 1-ch(T0), 16-bit× 2-ch (T1/T2)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
  - 8-Bit PWM (by T0)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1min interval at 4.194304MHz
- **Buzzer**
  - 8-bit× 1-ch
- **SPI 2**
  - 8-bit× 1-ch
- **UART**
  - 8-bit× 1-ch
- **I2C**
  - 8-bit× 1-ch
- **12-bit A/D Converter**
  - 10 Input channels
  - Power down wake-up function
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60/ 2.00/ 2.10/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Low Voltage Indicator**
  - 13 level detect (2.00 / 2.10/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/ 4.00/ 4.40V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0~2, EINT5, EINT6, EINT10, EINT11, EINT12) (6)
  - Timer(0/1/2) (4)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SPI (1)
  - UART (2)
  - I2C (1)
  - ADC (1)
  - ADC Wake-up (1)
- **Internal RC Oscillator**
  - Internal RC frequency:
    16MHz ±1.5% (T_A= 0 ~ +50°C, V_{DD}=2.0V ~ 5.5V)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal)
  - 2.7V ~ 5.5V (@ 0.4 ~ 10.0MHz with X-tal)
  - 3.0V ~ 5.5V (@ 0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.5 ~ 8.0MHz with Internal RC)
  - 2.0V ~ 5.5V (@ 0.5 ~ 16.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz main clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock

• **Package Type**
  - 20 SOP
  - 20 TSSOP
  - 20 PDIP
  - 20 QFN
  - 16 SOPN
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F8208S is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on all Microsoft-Windows operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- DSCL (MC96F8208 EVA P01 port)
- DSDA (MC96F8208 EVA P00 port)

NOTE)

1. MC96F8208S does not support the OCD function. MC96F8208 EVA should be used for debugging.
2. MC96F8208 EVA is MC96F8208OCD, MC96F8208SR, MC96F8208OB, MC96F8208OMN and MC96F8208OU.

OCD connector diagram: Connect OCD with user system

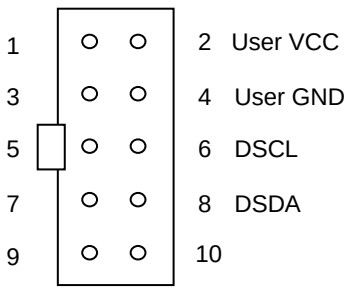


Figure 1.2 Debugger(OCD1/OCD2) and Pin description

Subject	MC96F8208S	MC96F8208 EVA(Evaluation chip)
Program/Data Memory	1. FLASH : 8k bytes 2. XRAM : 256 bytes	1. FLASH : 16k bytes 2. XRAM : 512 bytes
IOH/IOL of ports (Chapter 7.8 – DC Characteristics)	1. All Output Port : IOH = -2mA @VDD=4.5V 2. All Output Port : IOL = 15mA @VDD=4.5V	1. P1 : IOH = -20mA @VDD = 4.5V / P0, P26, P3 : IOH =-10mA @VDD = 4.5V / P20-25 : IOH =-10mA @VDD=4.5 2. All Output Port except P20-P25 : IOL = 15mA @VDD=4.5/ P20-P25 : IOL = 160mA @VDD4.5V
P04 – P06 Related Registers (Chapter 9.3 – P0 Port)	1. Bits 4-6 of P0/P0IO/P0PU/P0OD Registers : “Not used” 2. Bits 2-4 of P03DB Register : “Not used” 3. Bits 5-7 of P0FSR Register : “Not used”	1. Bits 4-6 of P0/P0IO/P0PU/P0OD Registers : “Used (000b)” 2. Bits 2-4 of P03DB Register : “Used (000b)” 3. Bits 5-7 of P0FSR Register : “Used (000b)”
P10 and P17 Related Registers (Chapter 9.4 – P1 Port)	1. Bits 0 and 7 of P1/P1IO/P1PU/P1OD Registers : “Not used” 2. Bit 0 of P12DB Register : “Not used” 3. Bit 6 of P1FSRH Register : “Not used” 4. Bit 0 of P1FSRL Register : “Not used”	1. Bits 0 and 7 of P1/P1IO/P1PU/P1OD Registers : “Used (0b and 0b)” 2. Bit 0 of P12DB Register : “Used (0b)” 3. Bit 6 of P1FSRH Register : “Used (0b)” 4. Bit 0 of P1FSRL Register : “Used (0b)”
P20 – P23 and P26 Related Registers (Chapter 9.5 – P2 Port)	1. Bits 0-3 and 6 of P2/P2IO/P2PU/P2OD Registers : “Not used” 2. Bits 4-7 of P12DB Register : “Not used”	1. Bits 0-3 and 6 of P2/P2IO/P2PU/P2OD Registers: “Used (0000b and 0b)” 2. Bits 4-7 of P12DB Register : “Used (0000b)”
P33 – P34 Related Registers (Chapter 9.6 – P3 Port)	1. Bits 3-4 of P3/P3IO/P3PU/P3OD/P3FSR Registers: “Not used”	1. Bits 3-4 of P3/P3IO/P3PU/P3OD/P3FSR Registers: “Used (00b)”
EINT2 – 4 Related Registers (Chapter 10.2 – Ext. Interrupt)	1. INT5E of IE controls only EINT0/1. 2. Bits 2-4 of EIFLAG0 Register : “Not used” 3. Bits 4-7 of EIPOL0L Register : “Not used” 4. Bits 0-1 of EIPOL0H Register : “Not used”	1. INT5E of IE controls EINT0-4. 2. Bits 2-4 of EIFLAG0 Register : “Used (000b)” 3. Bits 4-7 of EIPOL0L Register : “Used (0000b)” 4. Bits 0-1 of EIPOL0H Register : “Used (00b)”
EINT5 Related Registers (Chapter 10.2 – Ext. Interrupt)	1. Bit 0 of IE1 Register : “Not used” 2. Bit 5 of EIFLAG0 Register : “Not used” 3. Bits 2-3 of EIPOL0H Register : “Not used”	1. Bit 0 of IE1 Register : “Used (0b)” 2. Bit 5 of EIFLAG0 Register : “Used (0b)” 3. Bits 2-3 of EIPOL0H Register : “Used (00b)”
EINT7 – A Related Registers (Chapter 10.2 – Ext. Interrupt)	1. Bit 5 of IE2 Register : “Not used” 2. Bits 0-3 of EIFLAG1 Register : “Not used” 3. EIPOL2 is not exist.	1. Bit 5 of IE2 Register : “Used (0b)” 2. Bits 0-3 of EIFLAG1 Register : “Used (0000b)” 3. Bits 0-7 of EIPOL2 Register : “Used (0000 0000b)”

Table 1.2 Difference between MC96F8208S and evaluation chip (MC96F8208 EVA)

Subject	MC96F8208S	MC96F8208 EVA(Evaluation chip)
Clock Generator Related Registers (Chapter 11.1)	1. Bits 0-1 of SCCR Register ”11b” : “Not available” 2. Bit 0 of OSCCR Register : “Not used”	1. Bit0-1 of SCCR Register ”11b” : “Available” 2. Bit 0 of OSCCR Register : “Used (0b)”
Watch Timer Related Register (Chapter 11.4)	1. Bits 0-1 of WTCR Register “00b” : “Not available”	1. Bits 0-1 of WTCR Register “00b” : “Available”
Timer 0 Related Register (Chapter 11.5)	1. Bits 1-3 of T0CR Register “111b” : “Not available”	1. Bits 1-3 of T0CR Register “111b” : “Available”
Timer 2 Related Register (Chapter 11.7)	1. Bit 3 of T2CRL Register : “Always 1b”	1. Bit 3 of T2CRL Register : “Used (0b)”
Buzzer Related Register (Chapter 11.7)	1. Bits 1-3 of BUZCR Register ”1xxb” : “Not available”	1. Bits 1-3 of BUZCR Register ”1xxb” : “Available”
AN4 – AN7,AN14 Related Registers (Chapter 11.9)	1. Bits 0-3 of ADCCRL Register “0100b”/ “0101”/ “0110b”/ “0111”/ “1110b”: “Not available” 2. ADWRCR2 is not exist. 3. Bits 4-5 of ADWRCR3 Register : “Not used” 4. Bit 6 of ADWCRH Register : “Not used” 5. Bits 4-7 of ADWCRL Register : “Not used” 6. Bit 6 of ADWIFRH Register : “Not used” 7. Bits 4-7 of ADWIFRL Register : “Not used”	1. Bits 0-3 of ADCCRL Register : “0100b”/ “0101”/ “0110b”/ “0111”/ “1110b”: “Available” 2. Bits 0-7 ADWRCR2 Register : “Used (0000 0000b) 3. Bits 4-5 of ADWRCR3 Register : “Used (00b)” 4. Bit 6 of ADWCRH Register : “Used (0b)” 5. Bits 4-7 of ADWCRL Register : “Used (0000b)” 6. Bit 6 of ADWIFRH Register : “Used (0b)” 7. Bits 4-7 of ADWIFRL Register : “Used (0000b)”
SPI Related Register (Chapter 11.10)	1. Bit 2/5 of SPISR Register : “Not used”	1. Bit 2/5 of SPISR Register : “Used (00b)”
I2C Related Register (Chapter 11.12)	1. If P31 and P30 are used as SCL/SDA for I2C, P3OD[1] and P3OD[0] should be set “1”. 2. If P25 and P24 are used as SCL/SDA for I2C, P2OD[5] and P2OD[4] should be set “1”.	1. Don’t care
Full-flash Erase Mode Method (Chapter 15 – Flash Memory)	1.Sector Erase Mode	1.Sector and Byte Erase Mode

Table 1.2 Difference between MC96F8208S and evaluation chip (MC96F8208 EVA)

1.3.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

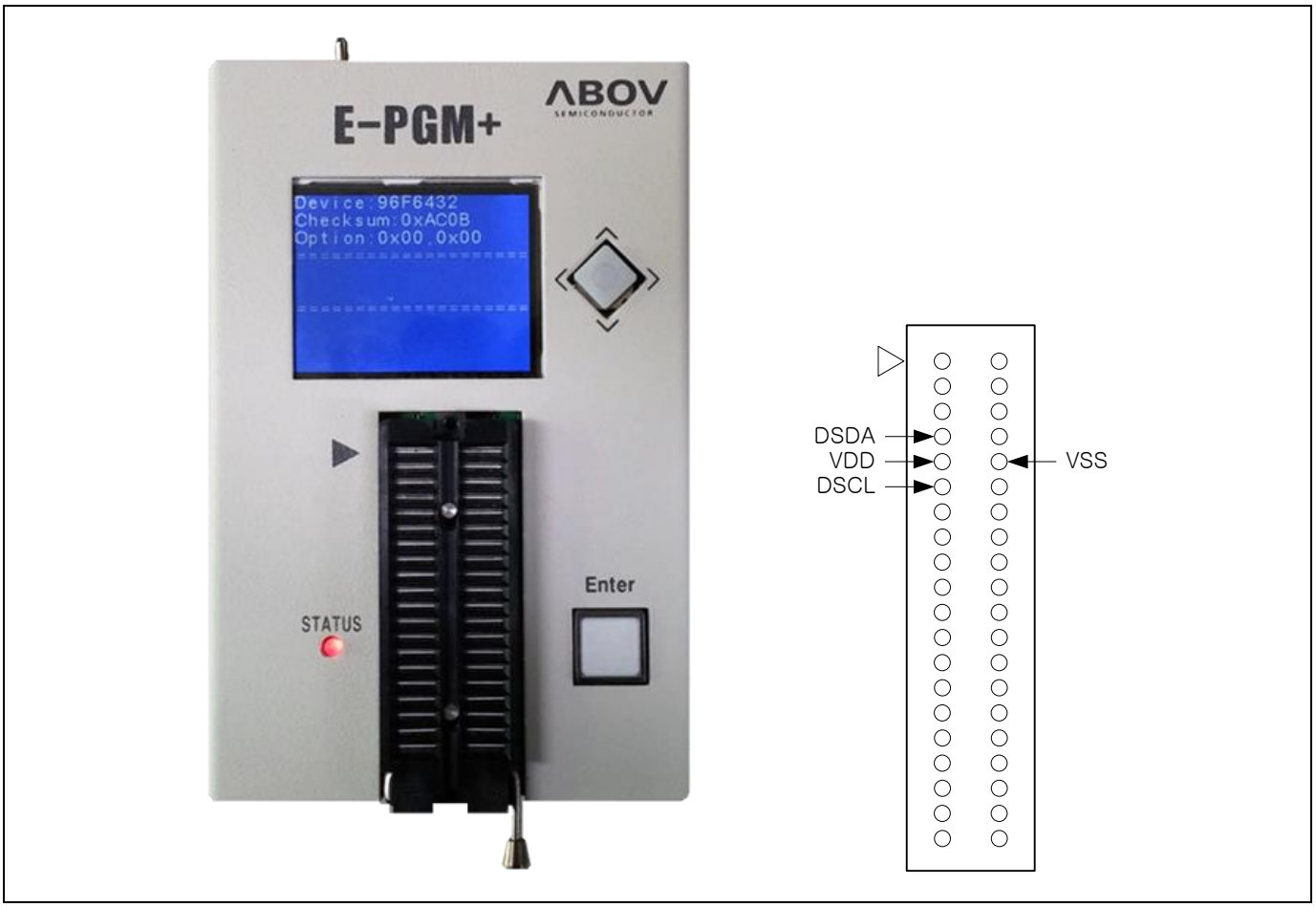


Figure 1.3 E-PGM+(Single writer)

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC96F8208S is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

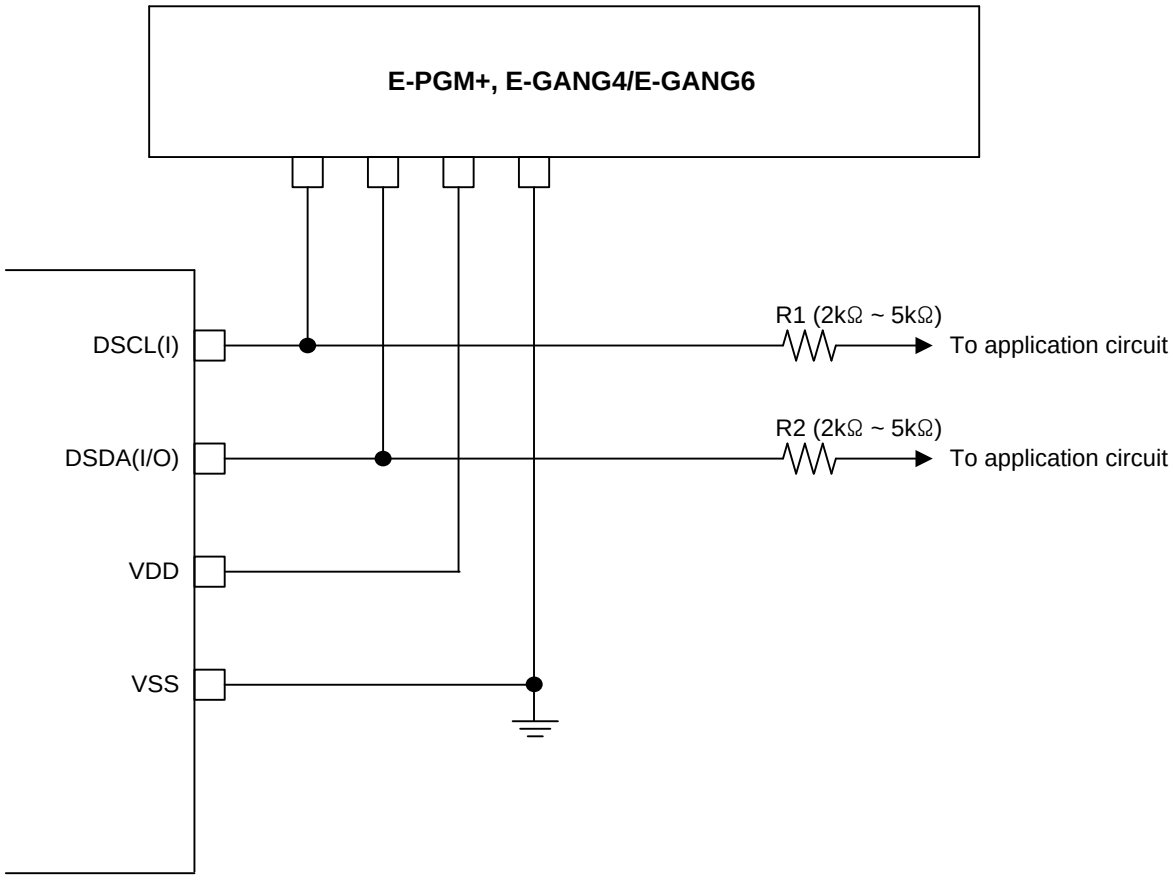
Table 1.3 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The MC96F8208S needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming. Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.5 PCB design guide for on board programming

2 Block diagram

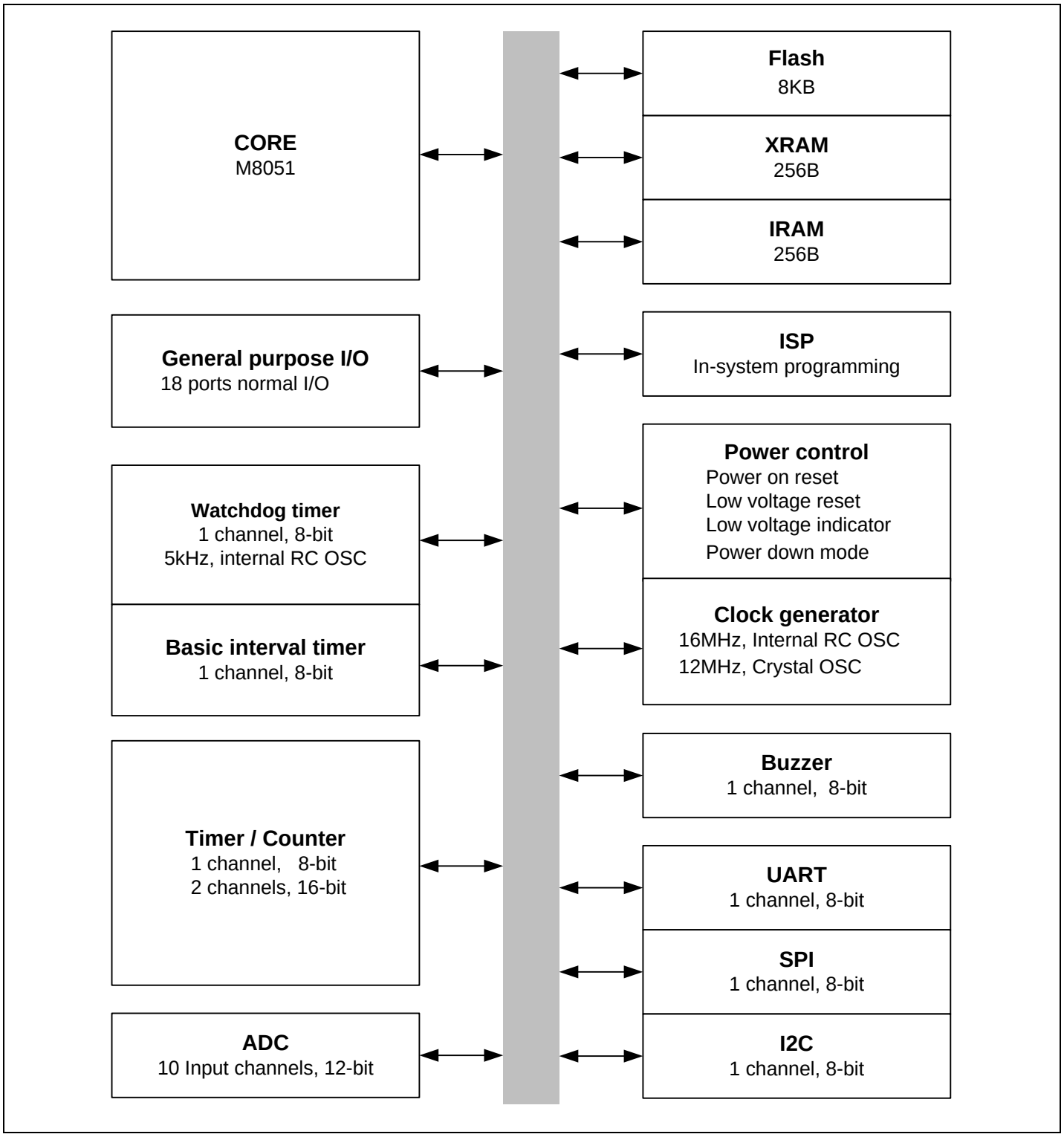
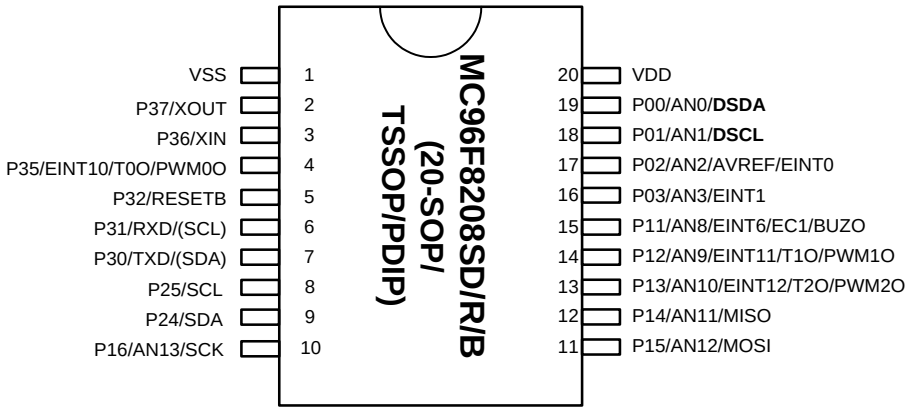


Figure 2.1 Block diagram of MC96F8208S

NOTE)

1. The P03, P11, P24 and P25 are not in the 16-Pin package.

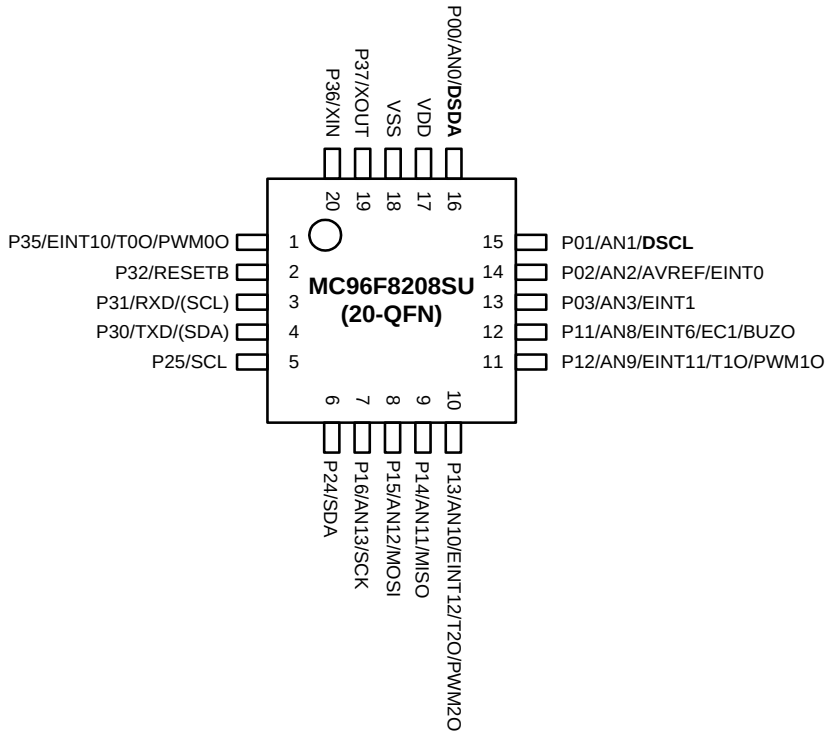
3 Pin assignment



NOTE)

1. The programmer (E-PGMplus, E-GANG4/E-GANG6) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

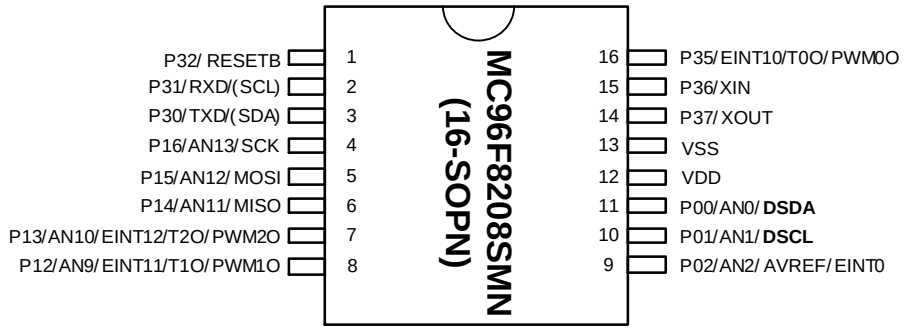
Figure 3.1 MC96F8208SD/R/B 20SOP/TSSOP/PDIP Pin Assignment



NOTE)

1. The programmer (E-PGMplus, E-GANG4/E-GANG6) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

Figure 3.2 MC96F8208SU 20QFN Pin Assignment



NOTE)

1. The programmer (E-PGMplus, E-GANG4/E-GANG6) uses P0[1:0] pin as DSCL, DSDA.
2. The P03, P11, P24 and P25 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used.
3. The SDA/SCL lines for I2C can be configured on the P30/P31 pins by software control.

Figure 3.3 MC96F8208SMN 16SOPN Pin Assignment

4 Package Diagram

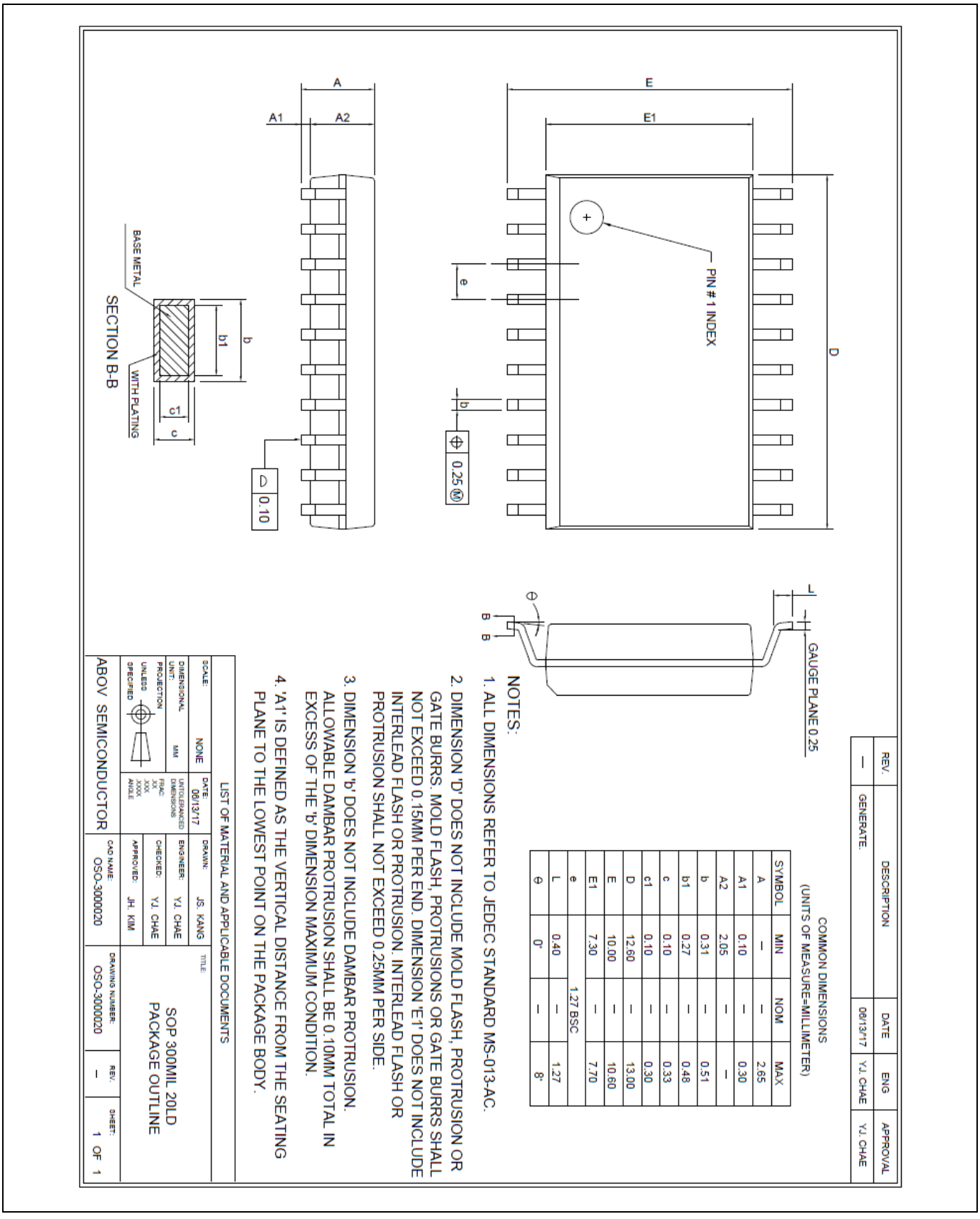


Figure 4.1 20-Pin SOP Package

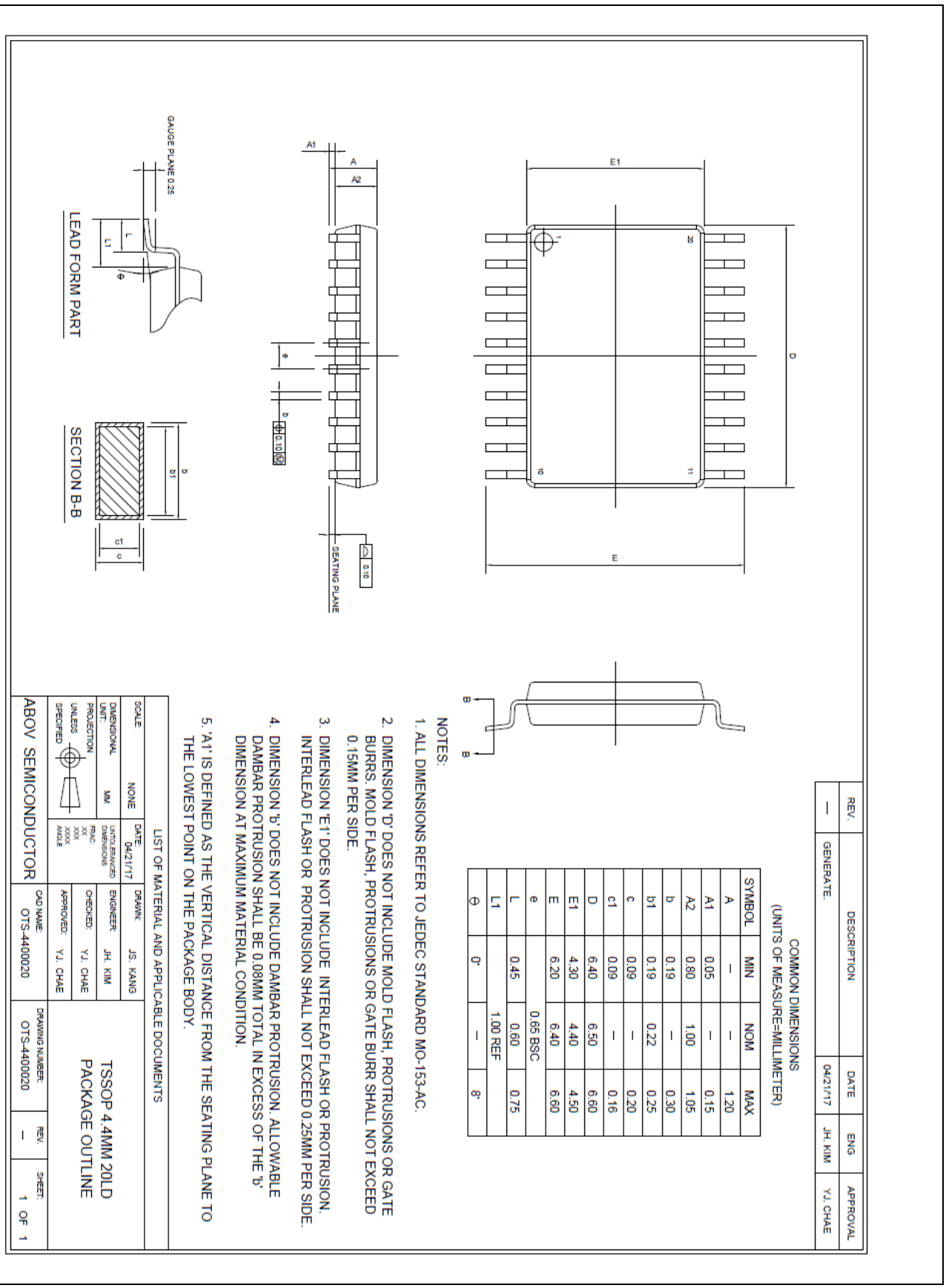


Figure 4.2 20-Pin TSSOP Package

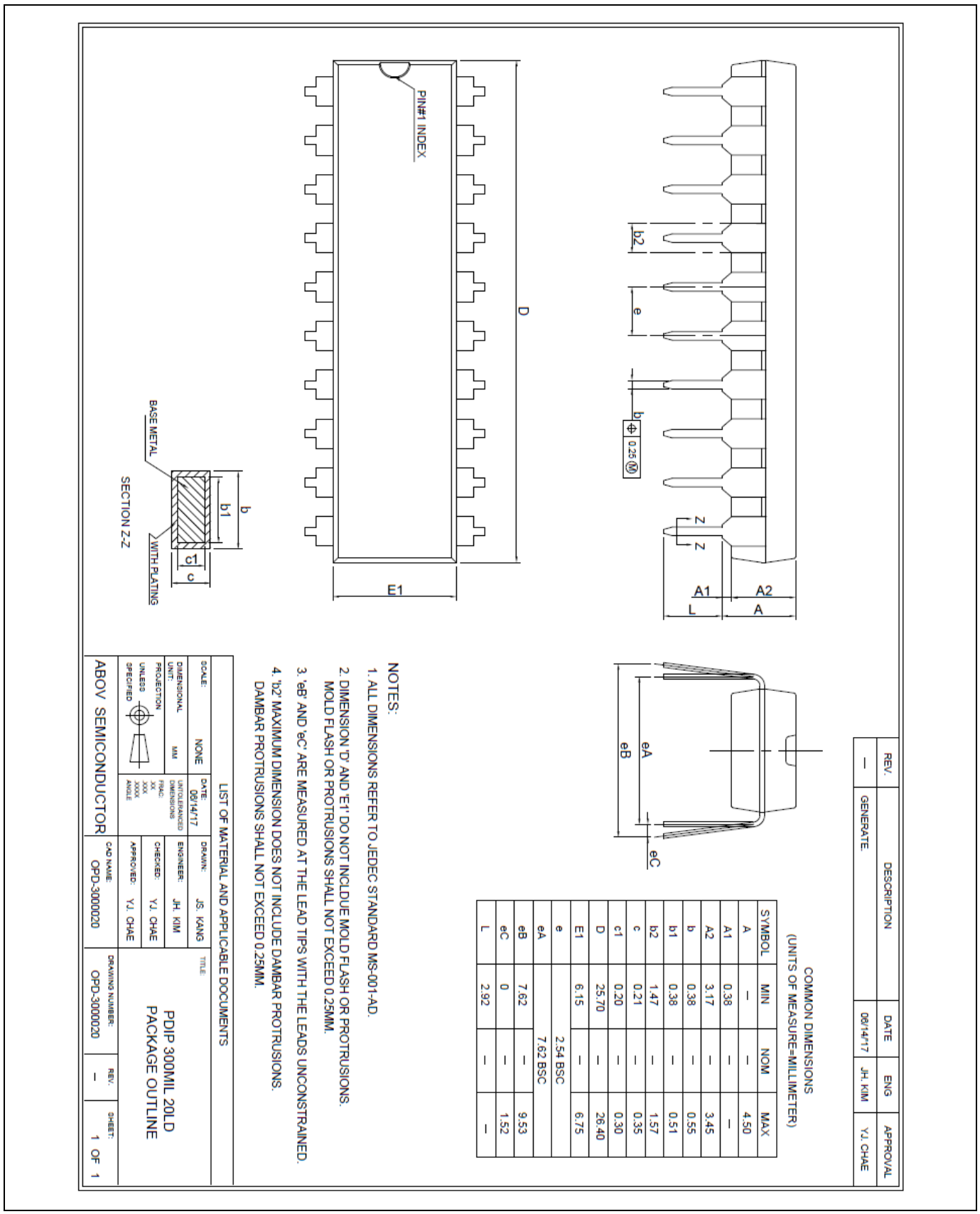


Figure 4.3 20-Pin PDIP Package

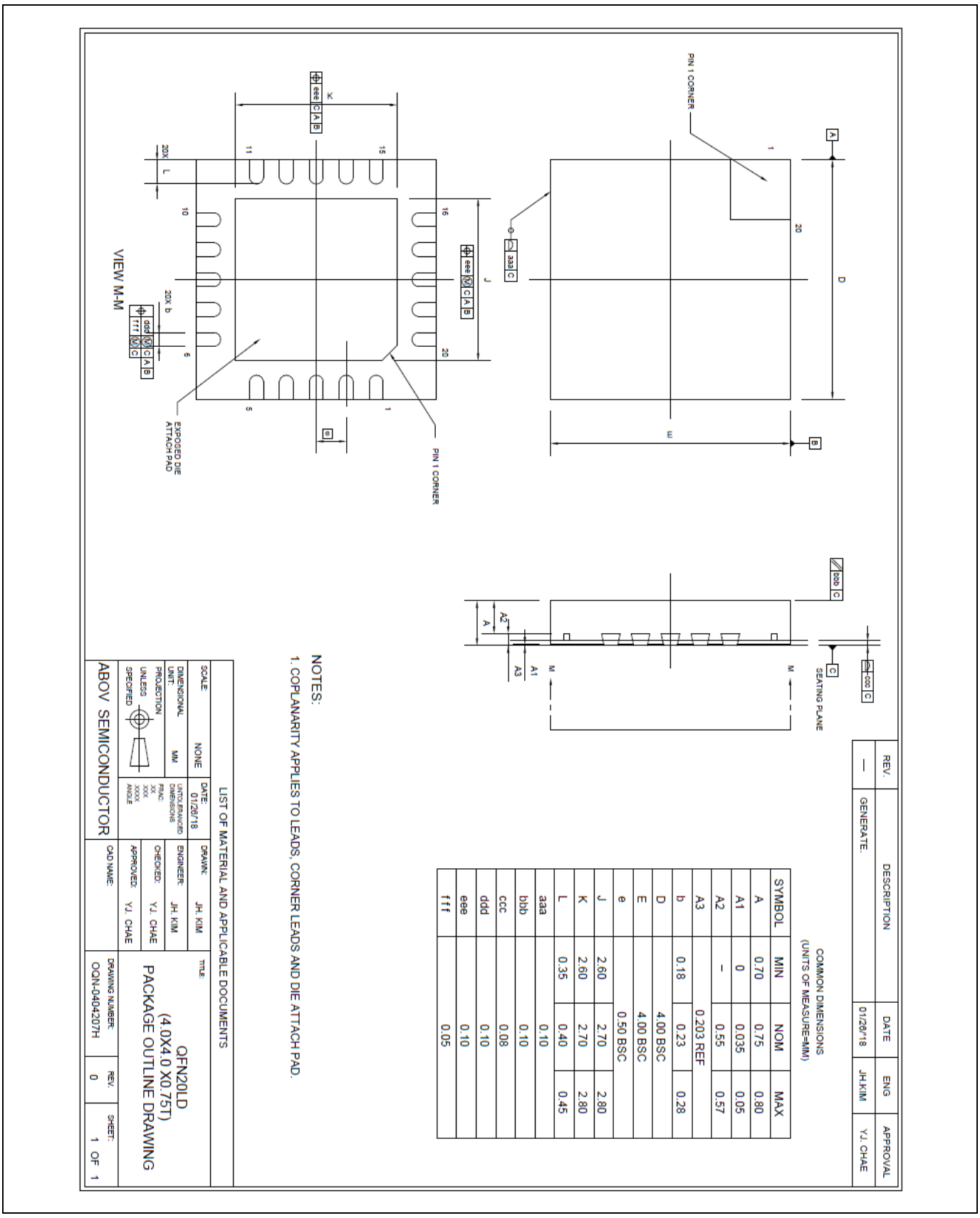


Figure 4.4 20-Pin QFN Package

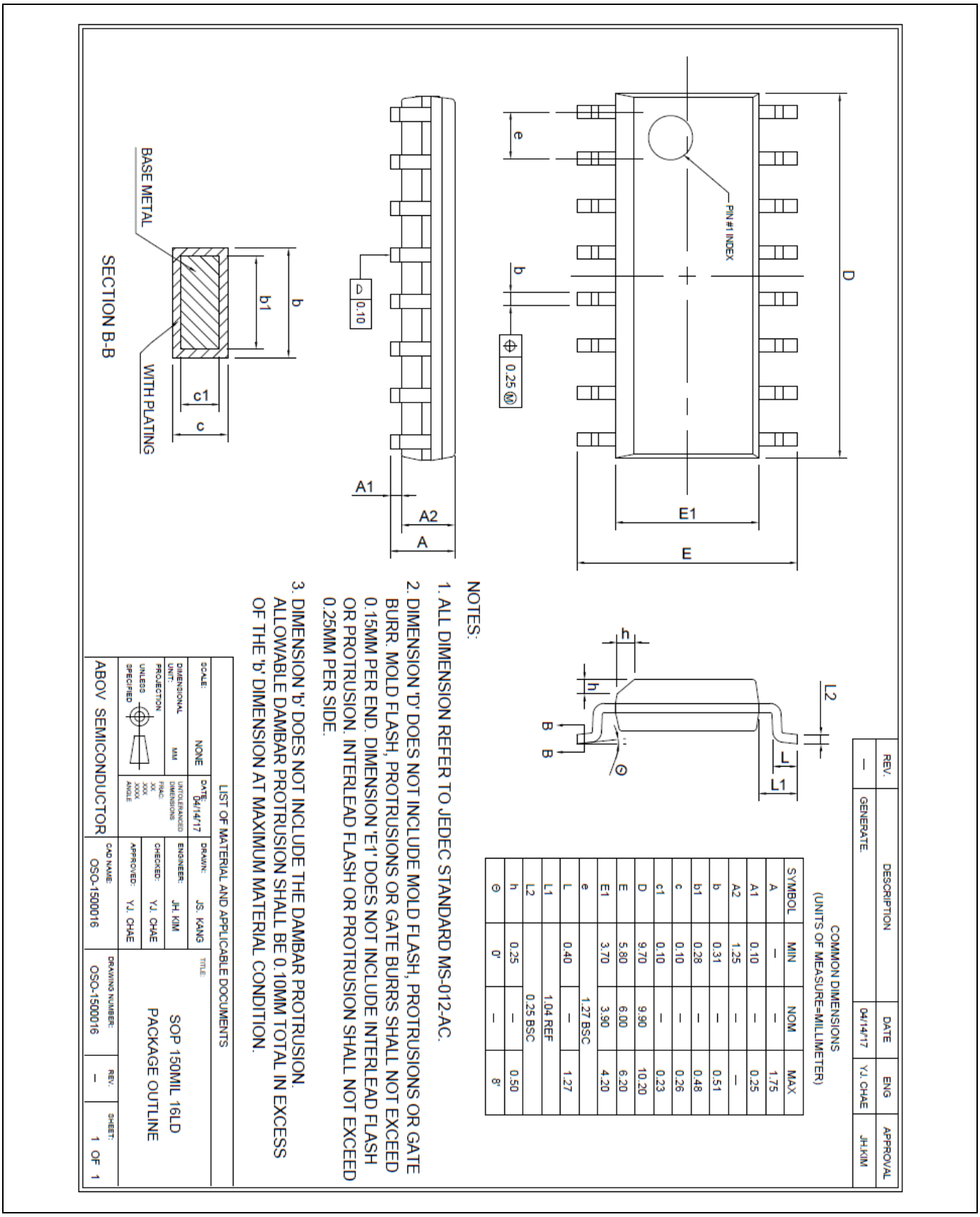


Figure 4.5 16-Pin SOPN Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P03 is only in the 20-Pin package.	Input	AN0/DSDA
P01				AN1/DSCL
P02				AN2/AVREF/EINT0
P03				AN3/EINT1
P11	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P11 is only in the 20-Pin package.	Input	AN8/EINT6/EC1/BUZO
P12				AN9/EINT11/T1O/PWM1O
P13				AN10/EINT12/T2O/PWM2O
P14				AN11/MISO
P15				AN12/MOSI
P16				AN13/SCK
P24	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P24 - P25 are only in the 20-Pin package.	Input	SDA
P25				SCL
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	TXD
P31				RXD
P32				RESETB
P35				EINT10/T0O/PWM0O
P36				XIN
P37				XOUT
EINT0	I/O	External interrupt inputs	Input	P02/AN2/AVREF
EINT1				P03/AN3
EINT6				P11/AN8/EC1/BUZO
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P35/T0O/PWM0O
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P12/AN9/T1O/PWM1O
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P13/AN10/T2O/PWM2O
T0O	I/O	Timer 0 interval output	Input	P35/EINT10/PWM0O
T1O	I/O	Timer 1 interval output	Input	P12/AN9/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P13/AN10/EINT12/PWM2O
PWM0O	I/O	Timer 0 PWM output	Input	P35/EINT10/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P12/AN9/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P13/AN10/EINT12/T2O
EC1	I/O	Timer 1 event count input	Input	P11/AN8/EINT6/BUZO
BUZO	I/O	Buzzer signal output	Input	P11/AN8/EINT6/EC1
SCK	I/O	Serial clock input/output	Input	P16/AN13
MISO	I/O	Serial data input/output	Input	P14/AN11
MOSI	I/O	Serial data input/output	Input	P15/AN12
TXD	I/O	UART data output	Input	P30
RXD	I/O	UART data input	Input	P31
SCL	I/O	I2C clock input/output	Input	P25
SDA	I/O	I2C data input/output	Input	P24

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
AVREF	I/O	A/D converter reference voltage	Input	P02/AN2/EINT0
AN0	I/O	A/D converter analog input channels	Input	P00/DSDA
AN1				P01/DSCL
AN2				P02/AVREF/EINT0
AN3				P03/EINT1
AN8				P11/EINT6/EC1/BUZO
AN9				P12/EINT11/T1O/PWM1O
AN10				P13/EINT12/T2O/PWM2O
AN11				P14/MISO
AN12				P15/MOSI
AN13				P16/SCK
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P32
DSDA	I/O	Programmer data input/output (NOTE4,5)	Input	P00
DSCL	I/O	Programmer clock input (NOTE4,5)	Input	P01
XIN	I/O	Main oscillator pins	Input	P36
XOUT				P37
VDD, VSS	–	Power input pins	–	–

Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P03, P11, P24 and P25 are not in the 16-Pin package.
2. The P32/RESETB pin is configured as one of the P32 and the RESETB pin by the “CONFIGURE OPTION”.
3. The P37/XOUT and P36/XIN pins are configured as a function pin by software control.
4. If the P00 and P01 pins are connected to the programmer during power-on reset, the pins are automatically configured as In-System programming pins.
5. The P00 and P01 pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.

6 Port Structures

6.1 General Purpose I/O Port

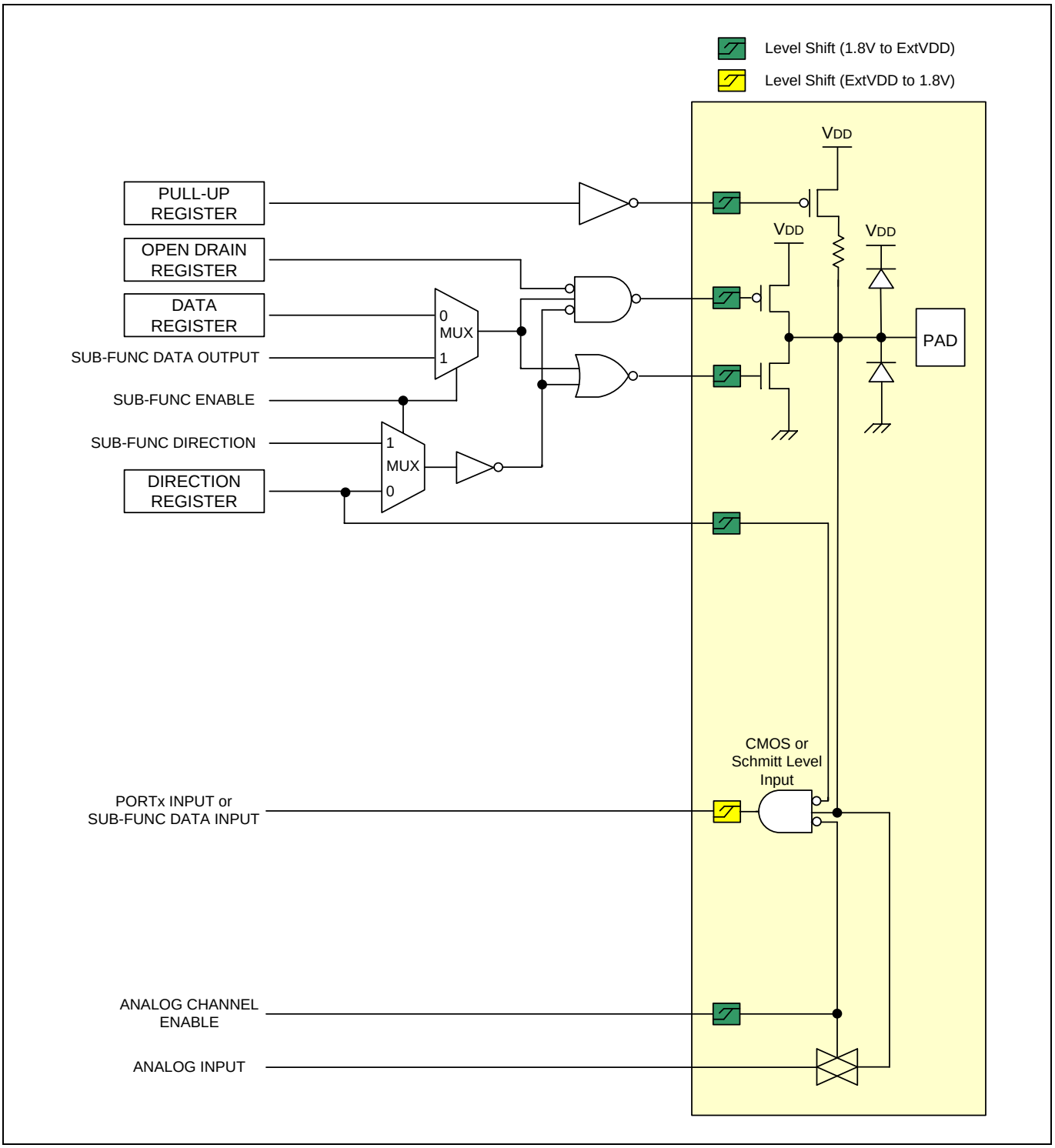


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

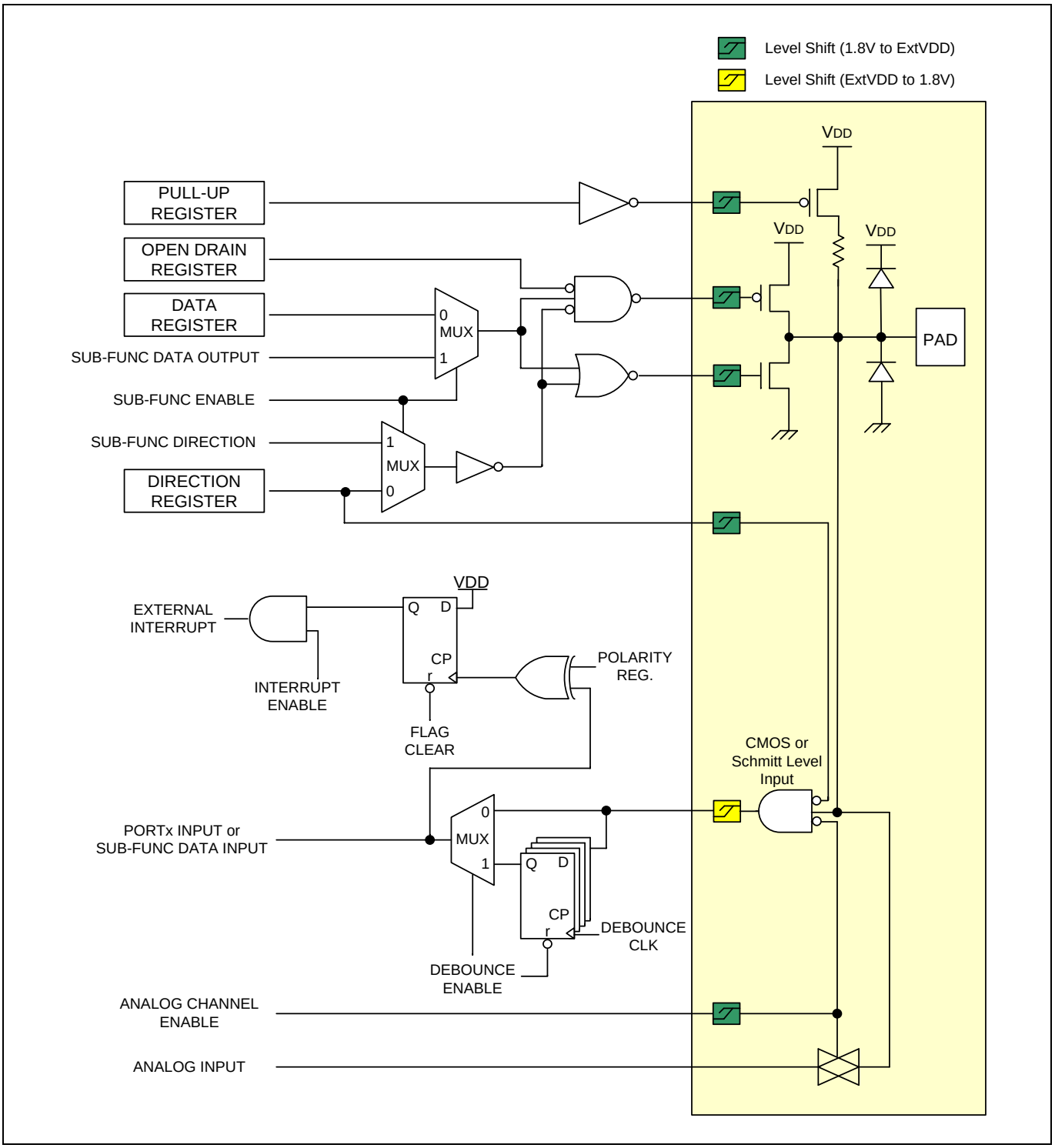


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 0.4 ~ 4.2MHz	Main Crystal	1.8	–	5.5	V
		f_X= 0.4 ~ 10.0MHz		2.7	–	5.5	
		f_X= 0.4 ~ 12.0MHz		3.0	–	5.5	
		f_X= 0.5 ~ 8.0MHz	Internal RC	1.8	–	5.5	
		f_X= 0.5 ~ 16.0MHz		2.0	–	5.5	
Operating Temperature	T_{OPR}	VDD= 1.8 ~ 5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–	12	–	bit
Integral Linear Error	ILE	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±6	LSB
Differential Linearity Error	DLE			–	–	±1	
Zero Offset Error	ZOE			–	–	±5	
Full Scale Error	FSE			–	–	±5	
Conversion Time	t_{CON}	12-bit resolution, 8MHz		20	–	–	us
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		1.8	–	VDD	
VDD18	–	–		–	1.8	–	V
Analog Input Leakage Current	I_{AN}	AVREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.7V, the ADC resolution is worse.

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.4 Power-on Reset Characteristics

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V		–	1.60	1.79	V
				1.85	2.00	2.15	
				1.95	2.10	2.25	
				2.05	2.20	2.35	
				2.17	2.32	2.47	
				2.29	2.44	2.59	
				2.39	2.59	2.79	
				2.55	2.75	2.95	
				2.73	2.93	3.13	
				2.94	3.14	3.34	
				3.18	3.38	3.58	
				3.37	3.67	3.97	
				3.70	4.00	4.30	
				4.10	4.40	4.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	0.1	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 High Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.0 – 5.5V		–	16	–	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass Capacitor	–	–	±1.5	%
		T_A = -20°C to +85°C				±2.5	
		T_A = -40°C to +85°C				±3.5	
Clock Duty Ratio	TOD	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.6 High Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

7.8 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	All input pins, RESETB		0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, RESETB		–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD= 4.5V, I_{OH}= -2mA, All output ports		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL}= 15mA; All output ports		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A= 25°C RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
ADC wake-up pull-up resistor	R_{AWPU1}	T_A= 25°C		100	150	200	kΩ
	R_{AWPU2}			200	300	400	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz, VDD= 5V±10%		–	3.0	6.0	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	2.2	4.4	
		f_{IRC}= 16MHz, VDD= 5V±10%		–	3.0	6.0	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz, VDD= 5V±10%		–	1.3	2.6	mA
		f_{XIN}= 10MHz, VDD= 3V±10%		–	0.7	1.4	
		f_{IRC}= 16MHz, VDD= 5V±10%		–	0.8	1.6	
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	uA

Table 7.8 DC Characteristics

NOTE)

1. Where the fXIN is an external main oscillator, the fIRC is an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.9 AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	EC1, VDD = 5V	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	EC1, VDD = 5V	20	–	–	

Table 7.9 AC Characteristics

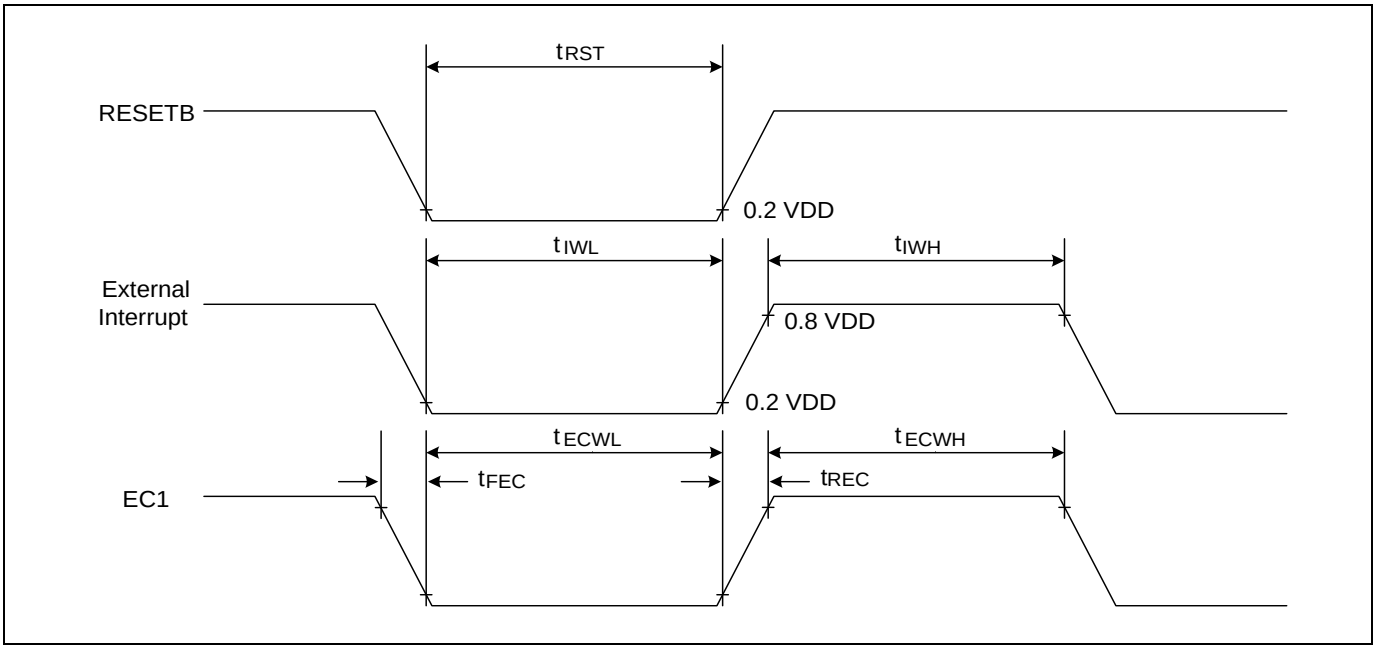


Figure 7.1 AC Timing

7.10 SPI Characteristics

(T_A=-40°C– +85°C, VDD=1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.10 SPI Characteristics

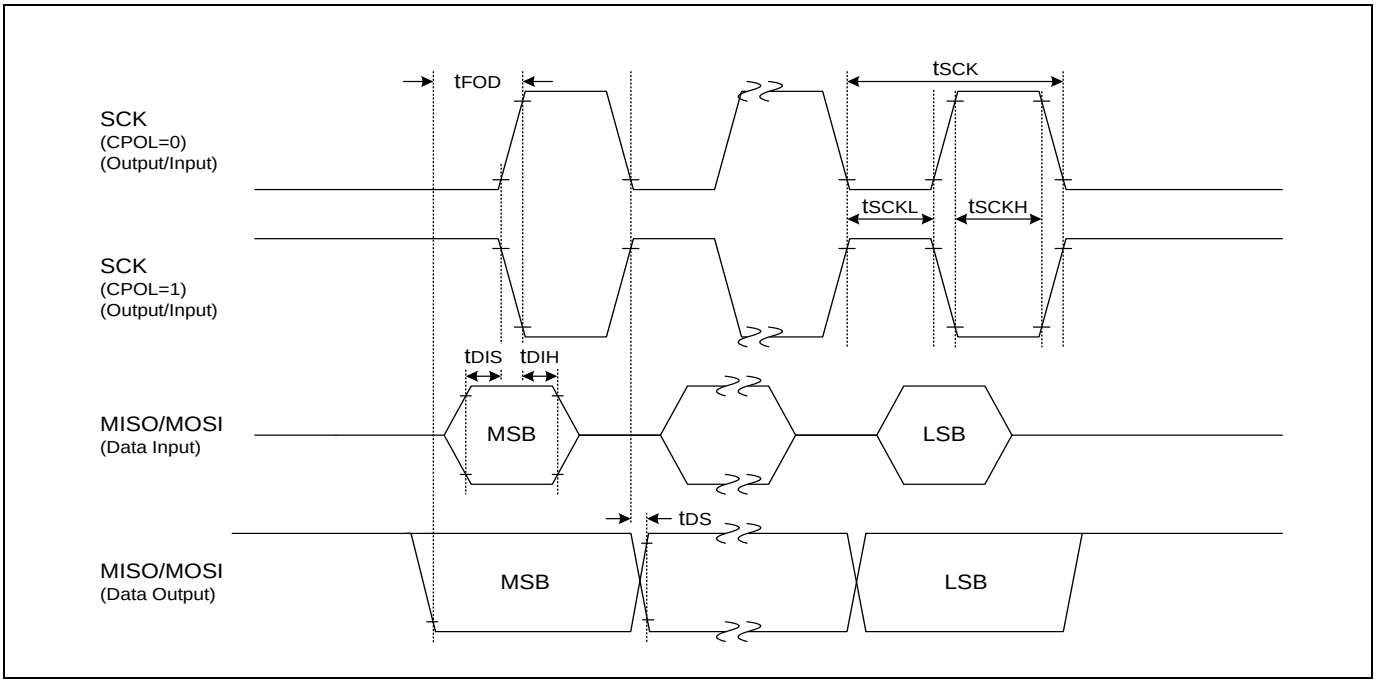


Figure 7.2 SPI Timing

7.11 UART Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	ns

Table 7.11 UART Characteristics

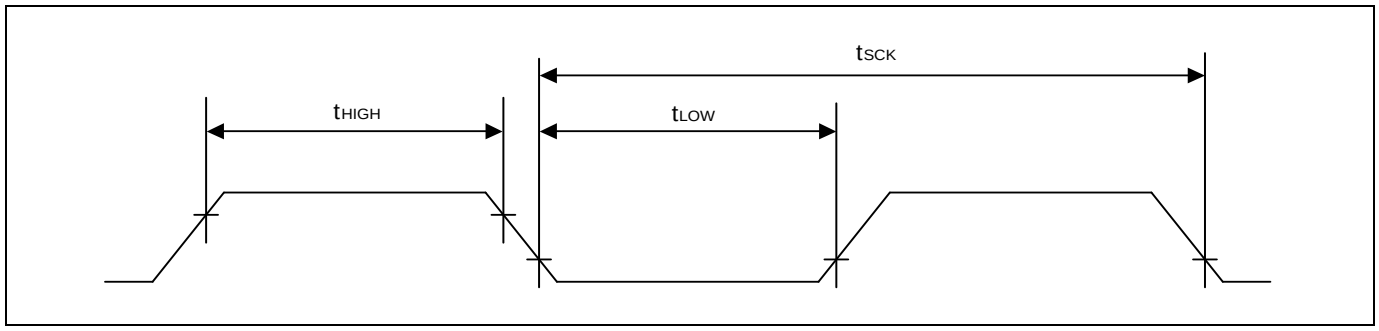


Figure 7.3 Waveform for UART Timing Characteristics

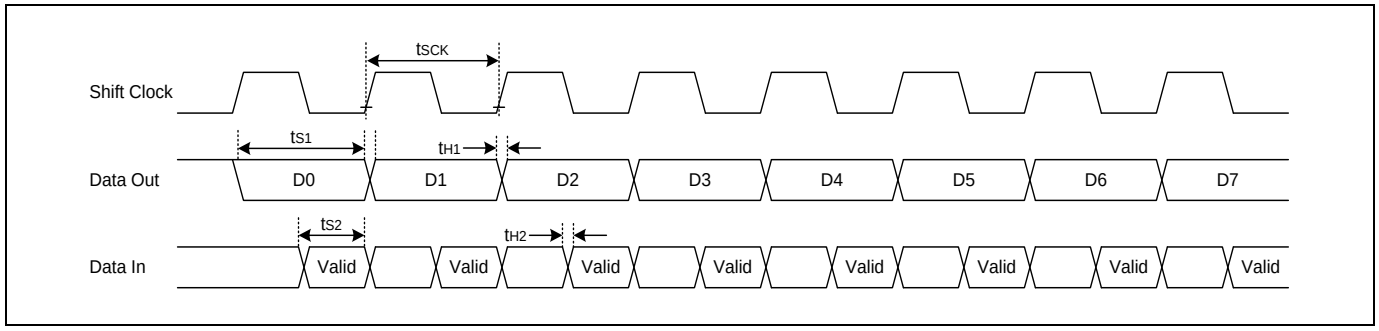


Figure 7.4 Timing Waveform for the UART Module

7.12 I2C Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.12 I2C Characteristics

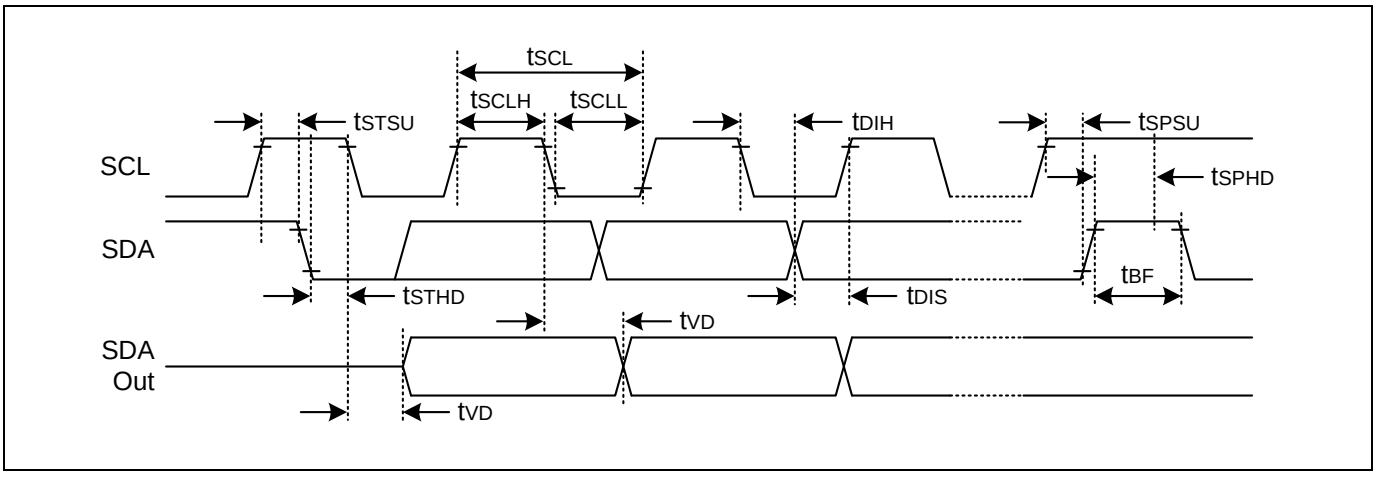


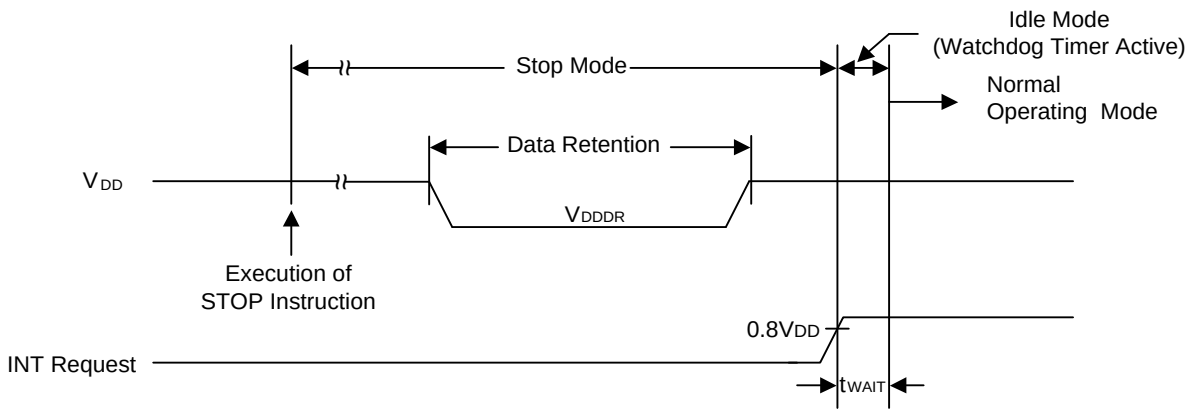
Figure 7.5 I2C Timing

7.13 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

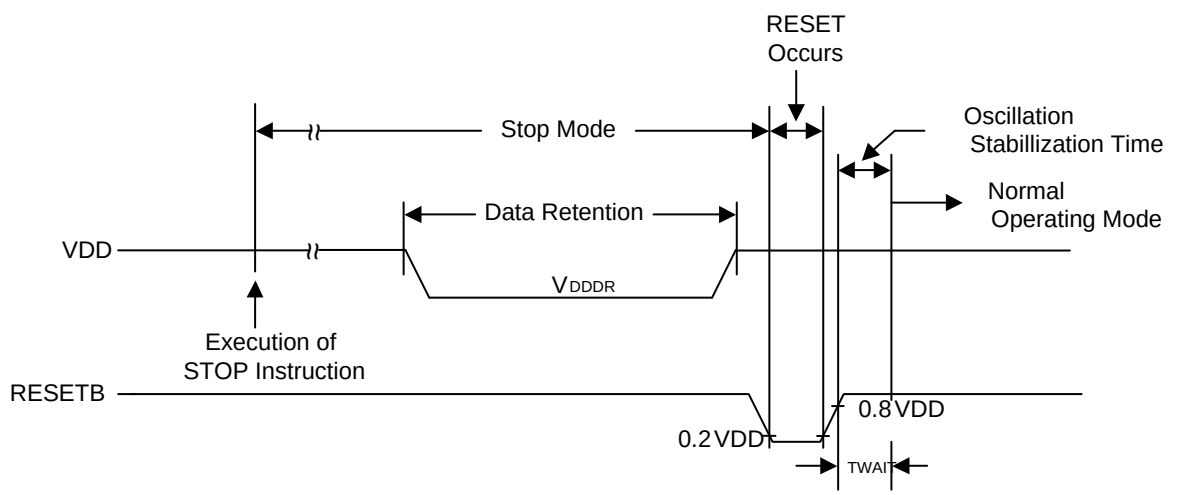
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7.13 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.14 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase(Sector 0~247)	NF_{WE}	–	–	–	10,000	times
Endurance of Write/Erase(Sector 248~255)					100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Table 7.14 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.15 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.15 Input/Output Capacitance

7.16 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	10.0	
		3.0V – 5.5V	0.4	–	12.0	

Table 7.16 Main Clock Oscillator Characteristics

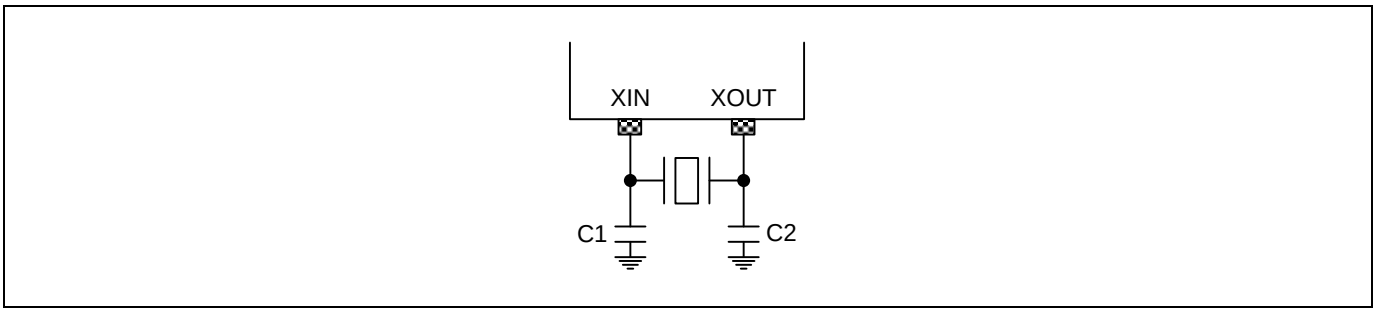


Figure 7.8 Crystal/Ceramic Oscillator

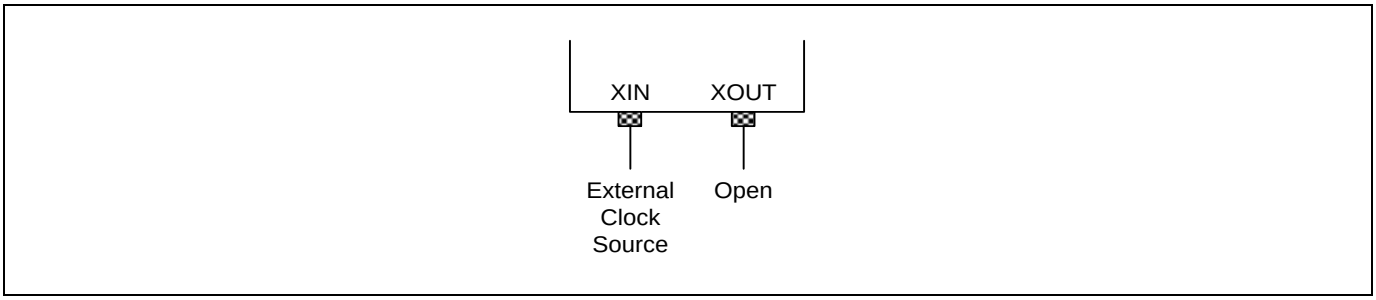


Figure 7.9 External Clock

7.17 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

Table 7.17 Main Oscillation Stabilization Characteristics

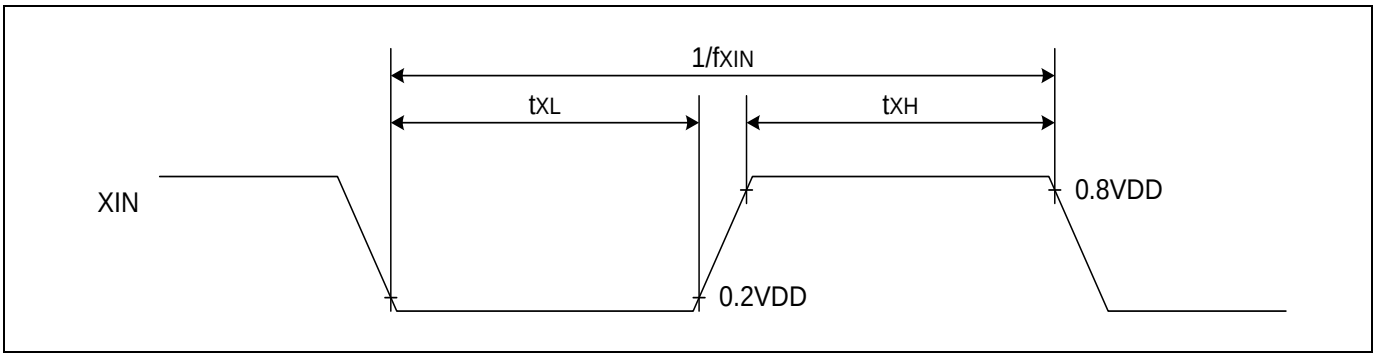


Figure 7.10 Clock Timing Measurement at XIN

7.18 Operating Voltage Range

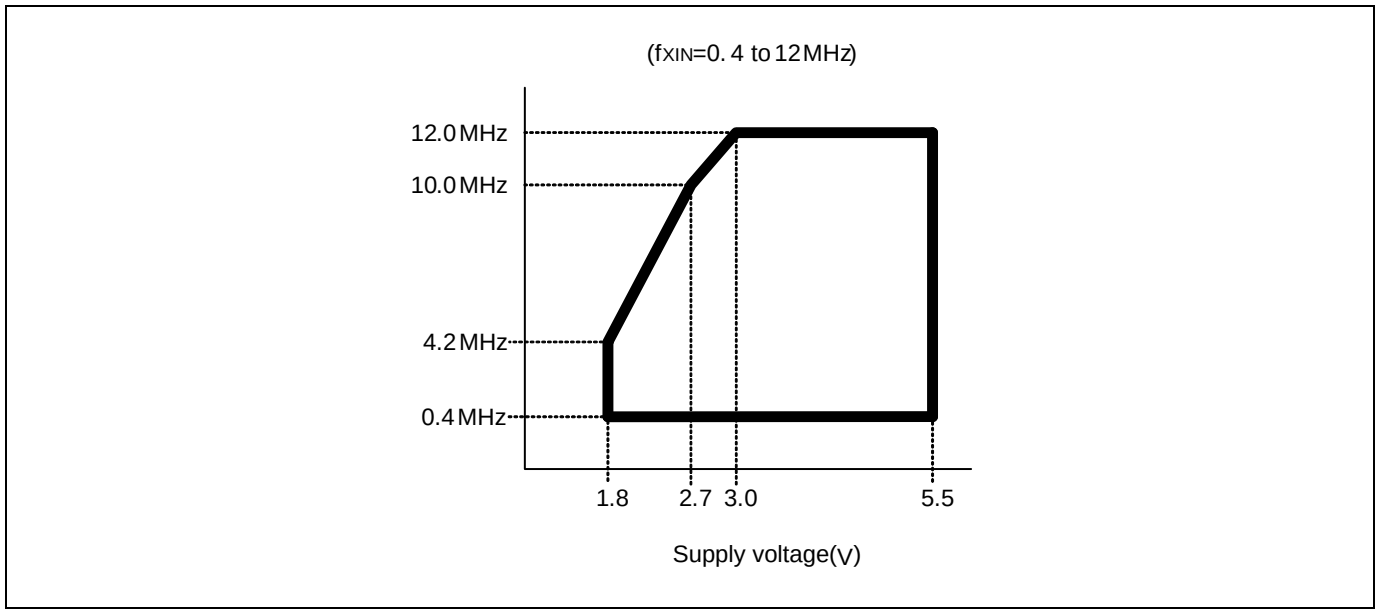


Figure 7.11 Operating Voltage Range

7.19 Recommended Circuit and Layout

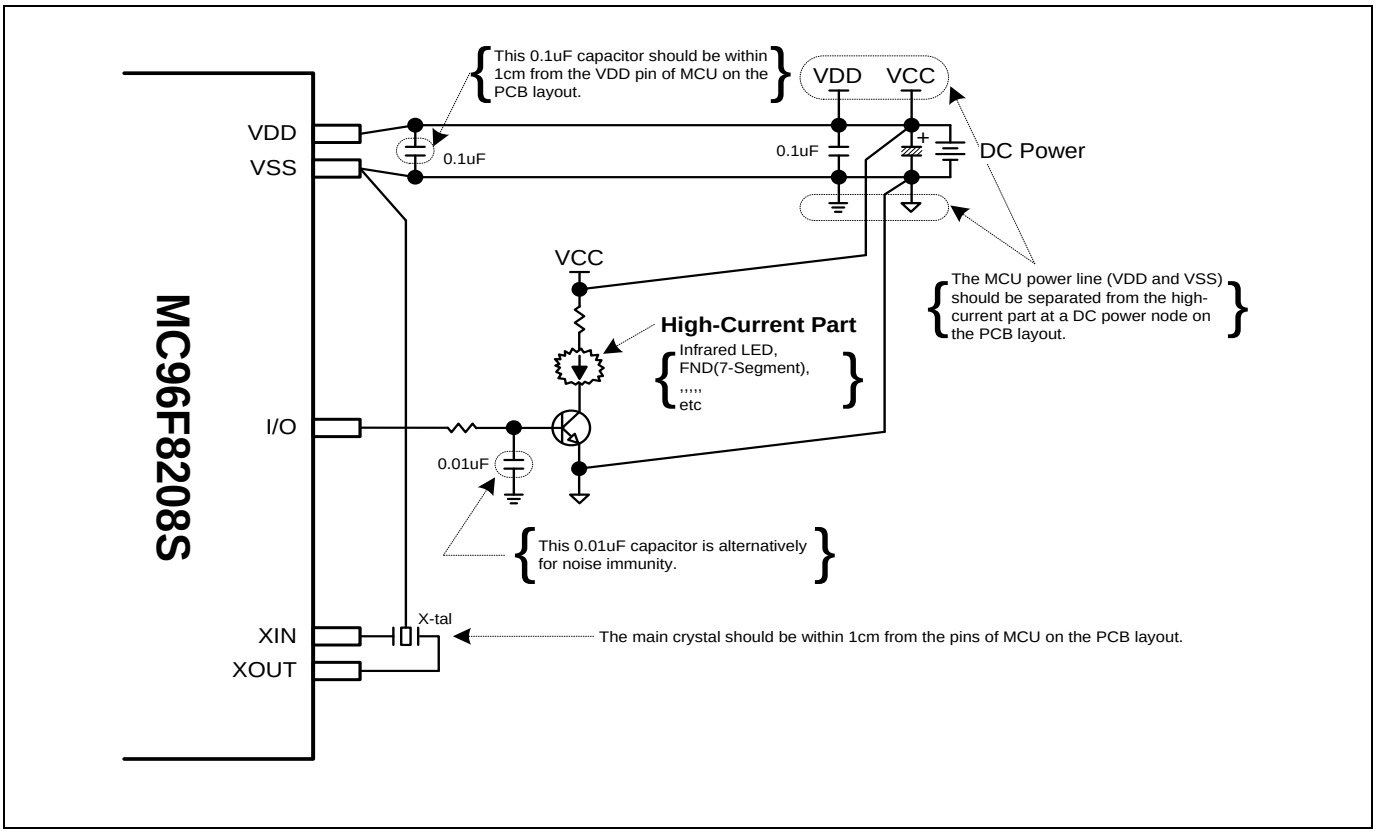
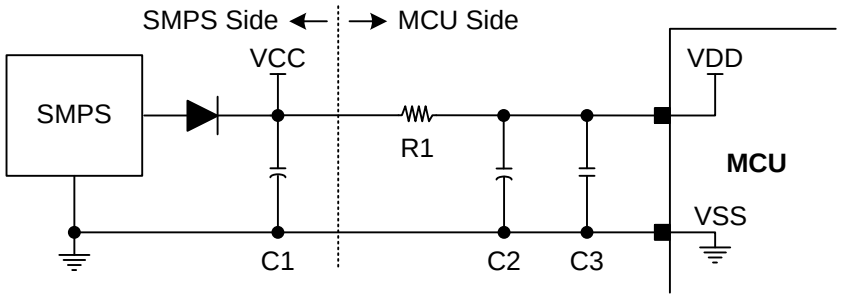


Figure 7.12 Recommended Circuit and Layout

7.20 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.13 Recommended Circuit and Layout with SMPS Power

7.21 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

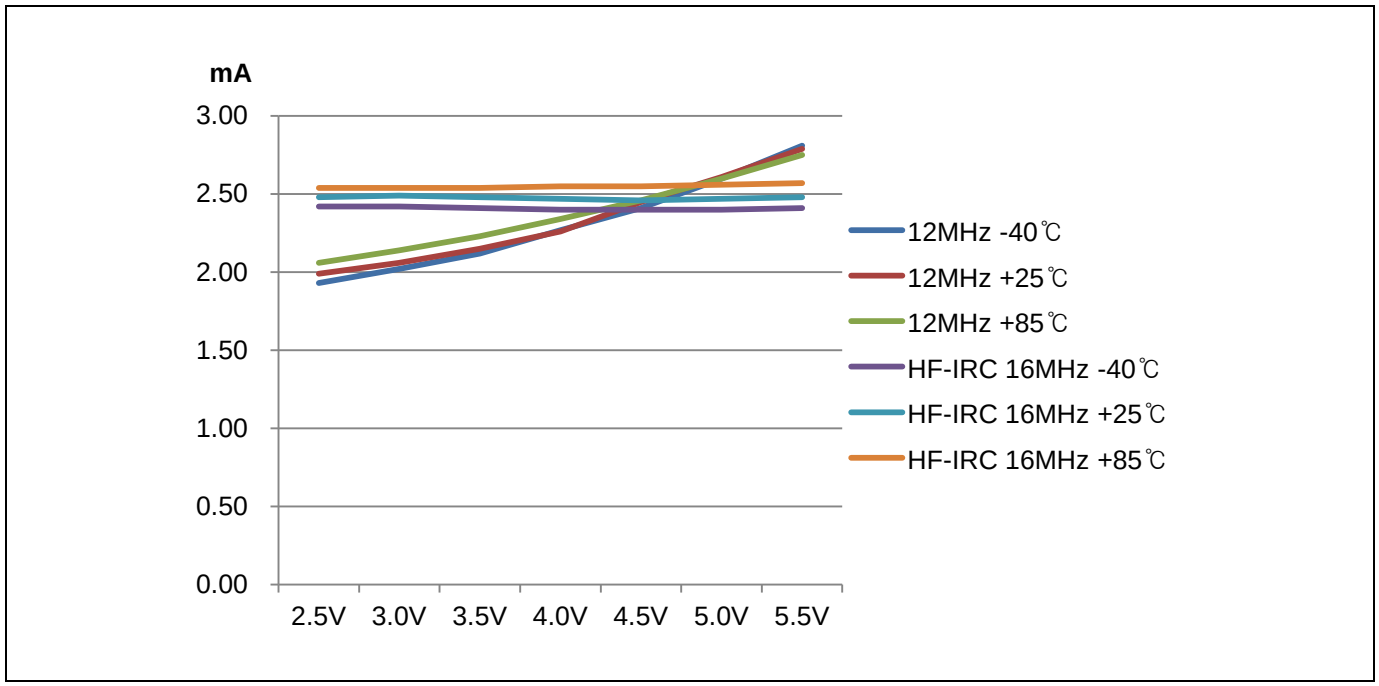


Figure 7.14 RUN (IDD1) Current

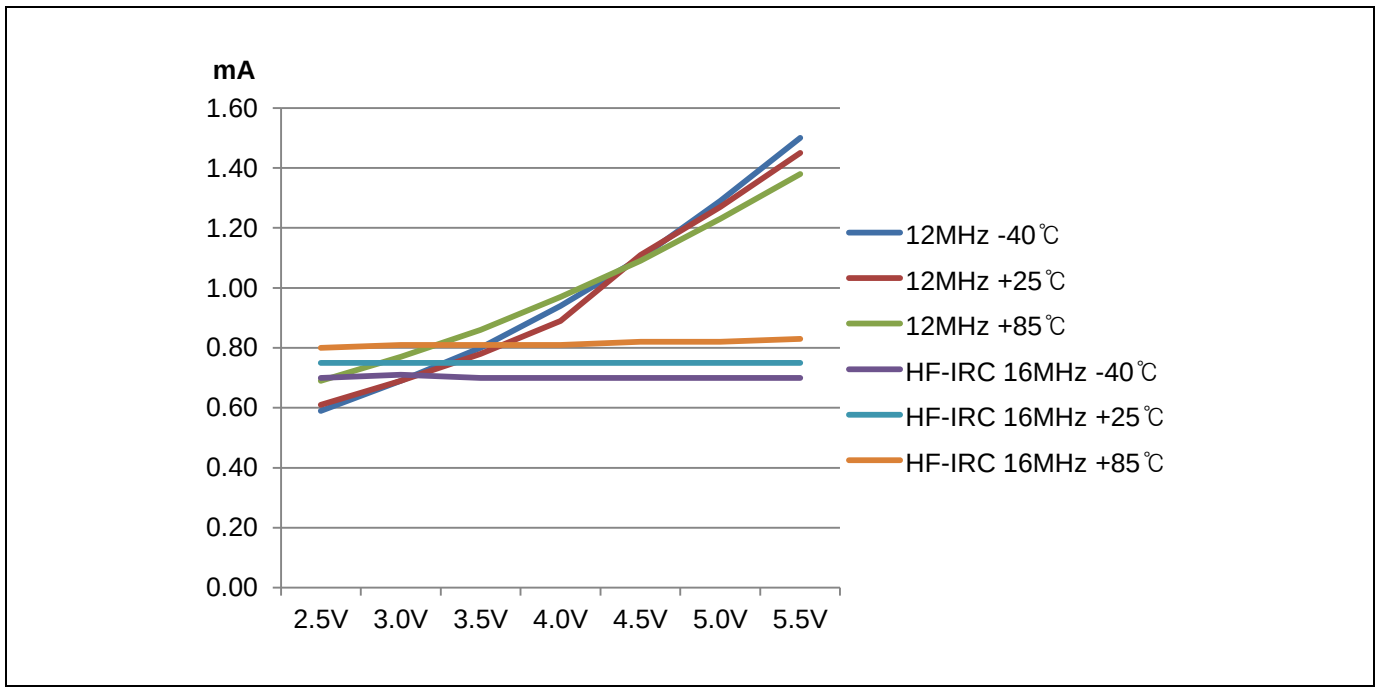


Figure 7.15 IDLE (IDD2) Current

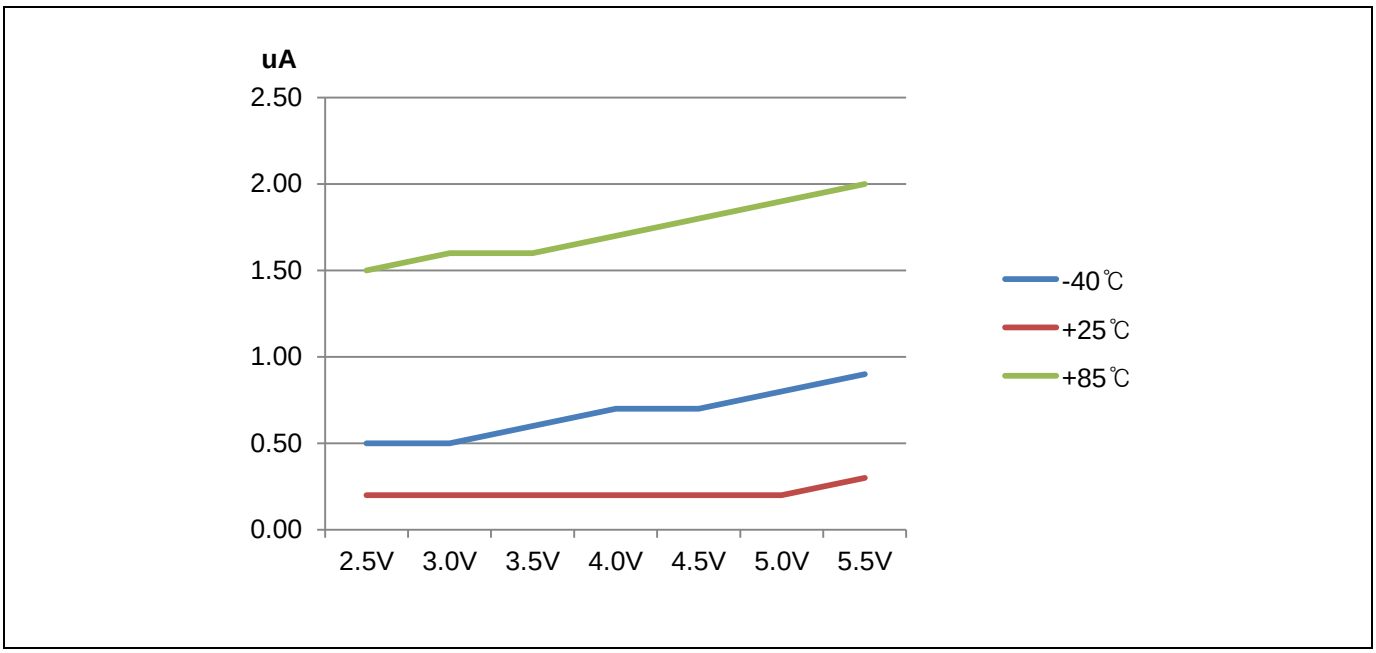


Figure 7.16 STOP (IDD5) Current

Table of contents