Product Brief

MM32F0020

ARM® Cortex®-M0 based 32-bit Microcontrollers

Revision: 1.0

Contents

Figures

Tables

1 Introduction

1.1 Overview

The MM32F0020 microcontrollers are based on ARM Cortex-M0 core. These devices have a maximum clocked frequency of 48MHz, built-in 32KB Flash storage, and contain and extensive range of peripherals and I/O ports. These devices contain one 12-bit ADC, one 16-bit advanced timer, one 16-bit general purpose timer and one 16-bit basic timer, as well as communication interfaces including one I2C, one SPI and two UART.

The operating voltage of these devices is 2.0V to 5.5V, and the operating temperature range (ambient temperature) includes the industrial tier -40°C to 85°C and extended industrial tier -40°C to 105°C. Multiple sets of power-saving modes make possible the design of low-power applications.

The target applications of these devices include:

- Chargers
- Communication module
- Toys
- Fans
- Battery management
- Smoke detectors
- 8/16-bit MCU upgrade

These devices are available in QFN20 and TSSOP20 packages.

1.2 Key features

- Core and system
  - 32-bit ARM Cortex-M0.
  - Frequency up to 48MHz.
- Memory
  - Up to 32KB embedded Flash storage.
  - Up to 2KB SRAM.
  - Embedded Bootloader to support In-System-Programming (ISP).
- Clock, reset and power management
  - Power supply ranges from 2.0 to 5.5V.
  - Power-on and Power-down reset (POR/PDR), Brown-out reset (BOR), Programmable voltage detector (PVD).
  - 4 to 24MHz high speed crystal oscillator.
  - 8MHz factory-trimmed high speed RC oscillator.
  - Integrated PLL to generate up to 48MHz system clock and support multiple

prescaler rate to provide clock sources to bus matrix and peripherals.
  - 40KHz low speed oscillator.
- Low power
  - Multiple low power modes including sleep mode, stop mode, deep stop mode and standby mode.
  - Ten 16-bit backup registers that keep the value in standby mode.
- Total 6 timers:
  - One 16-bit 4-channel advanced timer (TIM1), each channel providing two PWM output including one complementary output, supports hardware dead-time insertion and emergency brake when fault detected.
  - One 16-bit general purpose timer (TIM3), with up to four input capture or output compare channels and can be used for infrared decode.
  - One 16-bit basic timer (TIM14), with one input capture or output compare channel and one complementary output, support hardware dead-time insertion, emergency brake when fault detected, and integrated modulator circuit for infrared control.
  - Two watchdog timers, include one independent watchdog (IWDG) and one window watchdog (WWDG).
  - One 24-bit Systick timer.
- Up to 18 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts.
  - All I/O ports can accept input or generate output signal voltage level lower than V_{DD}.
- Up to 4 communication interfaces:
  - Two UART.
  - One I2C.
  - One SPI (support I2S mode).
- One 12-bit Analog-digital-converter (ADC), support 1μs conversion duration, with up to 8 external inputs and 1 internal inputs
  - Conversion range: 0 to V_{DDA}.
  - Configurable sampling cycles and resolution.
  - On-chip voltage sensor.
- Embedded CRC engine
- 96bit chip unique ID (UID)
- Debug mode
  - Serial-debug-interface (SWD).
- Available in QFN20 and TSSOP20 packages

2 Ordering information

2.1 Ordering table

Table 2-1 Ordering table

Part numbers / Features		MM32F0020B1T(V)	MM32F0020B1N(V)
CPU frequency		48 MHz	
Flash - KB		32	32
SRAM - KB		2	2
Timers	16-bit GP	1	1
	Basic	1	1
	Advanced	1	1
Interfaces	UART	2	2
	I2C	1	1
	SPI / I2S	1	1
GPIO		18	18
12-bit ADC	Modules	1	1
	Channels	8	8
Supply voltage		2.0V to 5.5V	
Temperature range		-40◦C to +85◦C / -40◦C to +105◦C (V part)	
Package		TSSOP20	QFN20

2.2 Marking information

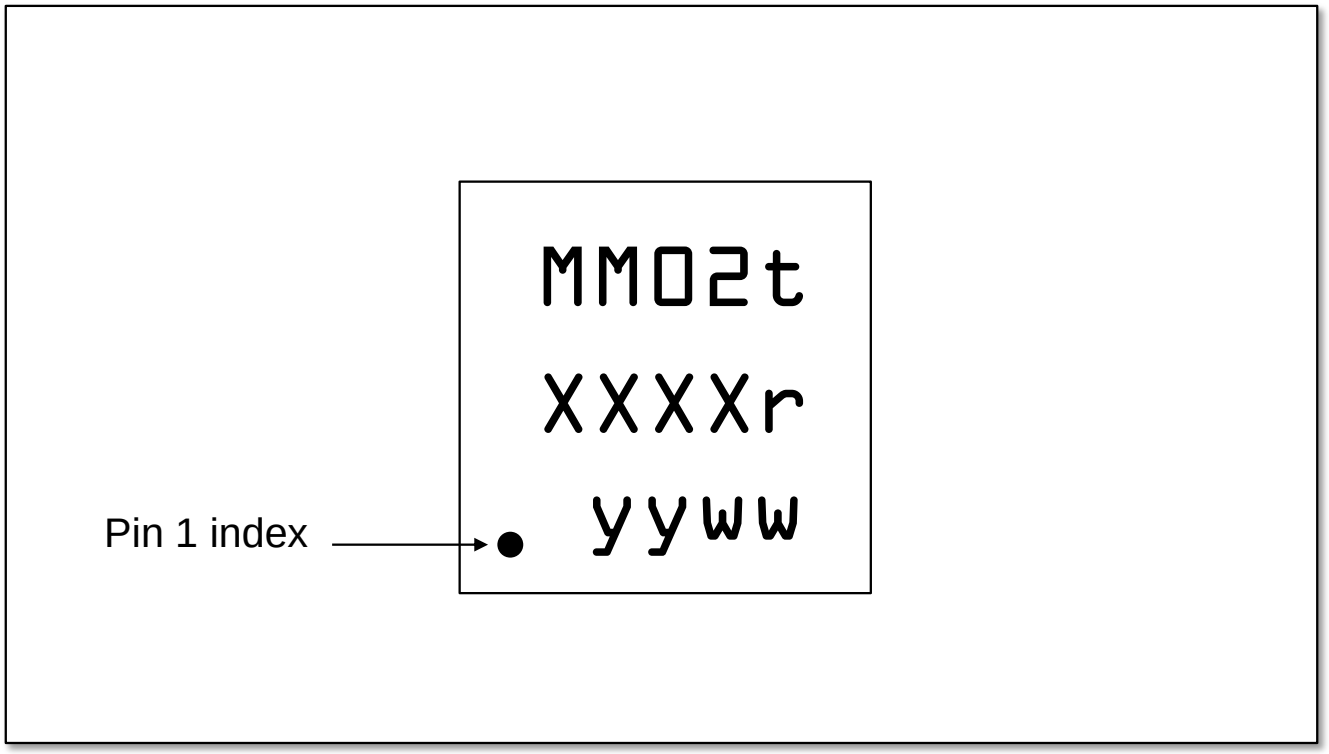

Figure 2-1 QFN20 package marking

The QFN20 package has the following topside marking:

- 1st line: MM02t
  - Abbreviation of the product name. “MM02” means MM32F0020 series. “t” means ambient temperature range, “t” = (blank) means -40 to 85°C, “t” = “V” means -40 to 105°C.
- 2nd line: xxxxr
  - Trace code + revision code, the “r” means chip revision.
- 3rd line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

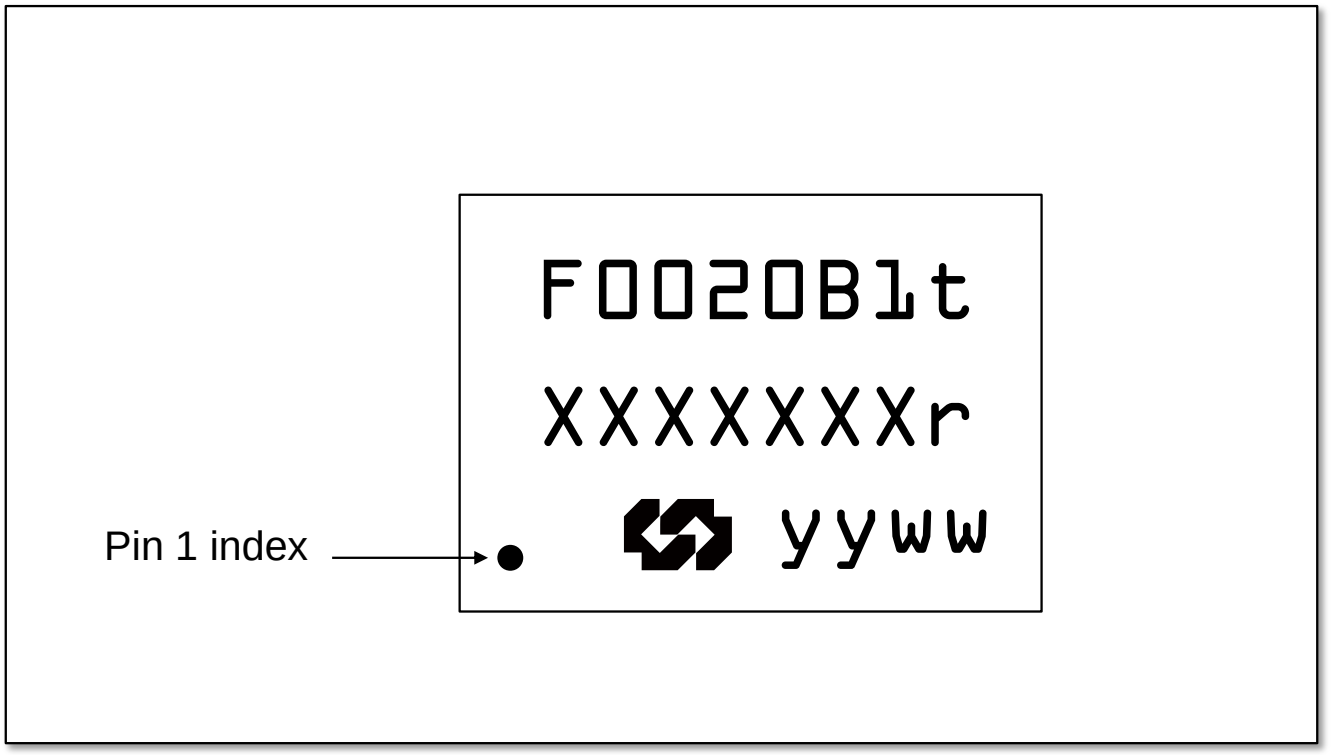

Figure 2-2 TSSOP20 package marking

The TSSOP20 package has the following topside marking:

- 1st line: F0020xxt
  - Product name. “t” means ambient temperature range, “t” = (blank) means -40 to 85°C, “t” = “V” means -40 to 105°C.
- 2nd line: xxxxxxxr
  - Trace code + revision code, the “r” means chip revision.
- 3rd line: yyww
  - Date code, “yy” means year and “ww” means week in date code.

3 Functional description

3.1 Block diagram

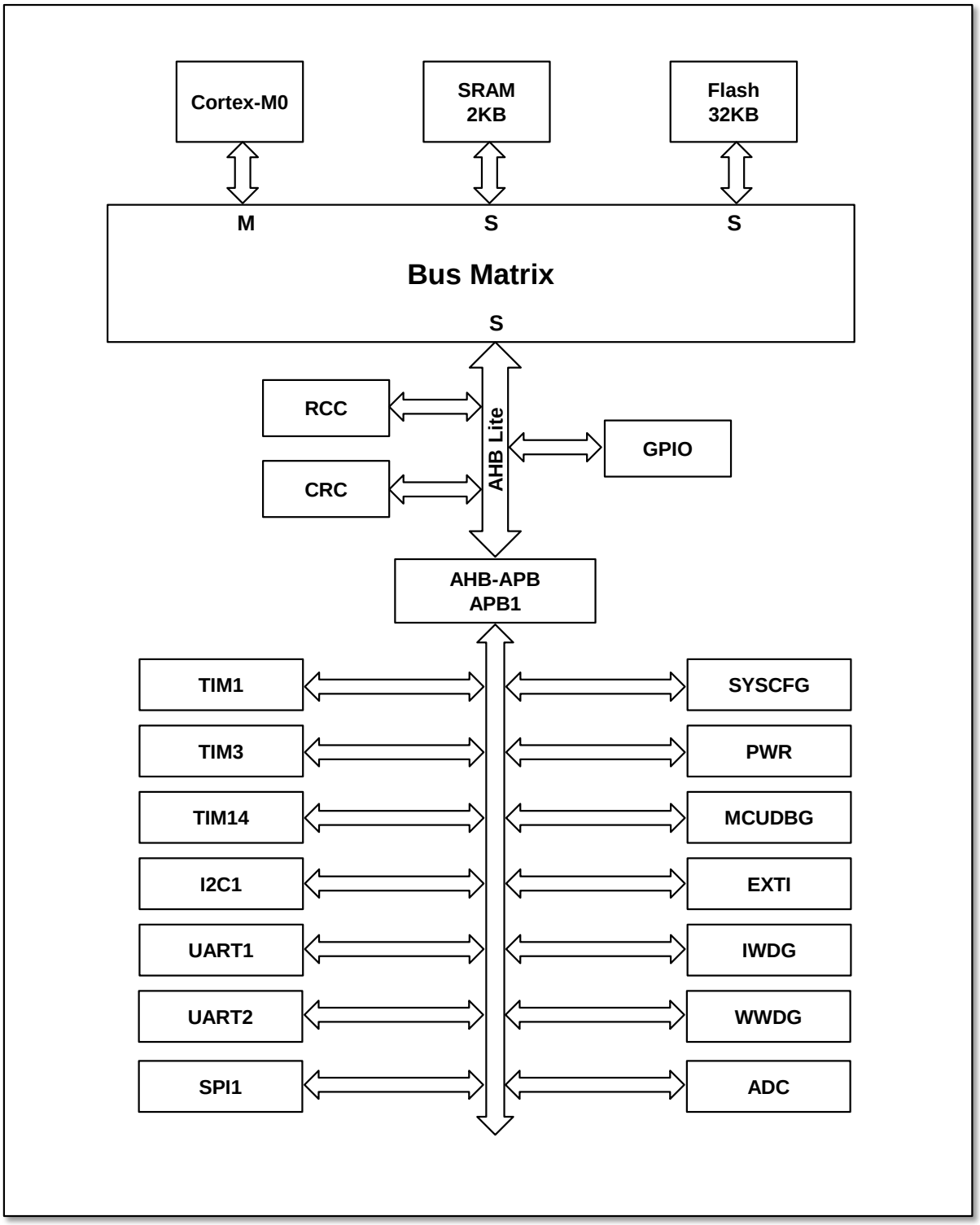

Figure 3-1 System block diagram

3.2 Core introduction

The ARM® Cortex®-M0 processor provides real-time processing and advanced interrupt handling system, which is perfect for cost-effective and low-pin-count microcontrollers targeting real-time control and low power applications.

The ARM® Cortex®-M0 is a 32-bit RISC processor, provides state-of-the-art code efficiency, which is extremely suitable for small memory size microcontrollers and small code size applications.

With its embedded ARM core, this product is compatible with all the tools and software for ARM-based products.

3.3 Bus introduction

The bus matrix includes one AHB inter-connection bus matrix, one AHB bus and two AHB-to-APB bridges. The bus matrix has arbitration capability for scenarios when both CPU and DMA send access simultaneously. The peripherals on the AHB bus (e.g., RCC, GPIO, CRC) are connected to the system bus through the inter-connection matrix. The data are transferred between AHB and APB bus using an AHB-to-APB bridge. When there's 8-bit or 16-bit access to APB registers, the APB bus will extend the access to 32-bit automatically.

3.4 Memory map

Table 3-1 Memory map

Bus	Address range	Size	Peripheral
Flash	0x0000 0000-0x0000 7FFF	32 KB	Main flash memory, system memory or SRAM, depending on BOOT configuration
	0x000 4000-0x07FF FFFF	~127 MB	Reserved
	0x0800 0000-0x0800 7FFF	32 KB	Main Flash memory
	0x0801 0000-0x1FF0 FFFF	~383 MB	Reserved
	0x1FFE 0000-0x1FFE 01FF	0.5 KB	Reserved
	0x1FFE 0200-0x1FFE 0FFF	3 KB	Reserved
	0x1FFE 1000-0x1FFE 11FF	0.5 KB	Reserved
	0x1FFE 1200-0x1FFE 1BFF	2.5 KB	Reserved
	0x1FFE 1C00-0x1FFF F3FF	~256 MB	Reserved
	0x1FFF F400-0x1FFF F7FF	1 KB	System memory
	0x1FFF F800-0x1FFF F80F	16 B	Option bytes
	0x1FFF F810-0x1FFF FFFF	2 KB	Reserved
SRAM	0x2000 0000-0x2000 07FF	2KB	SRAM
	0x2000 4000-0x2FFF FFFF	~255 MB	Reserved
APB1	0x4000 0000-0x4000 03FF	1 KB	Reserved
	0x4000 0400-0x4000 07FF	1 KB	TIM3
	0x4000 0800-0x4000 0BFF	8 KB	Reserved
	0x4000 2800-0x4000 2BFF	1 KB	Reserved

Bus	Address range	Size	Peripheral
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG
	0x4000 3000-0x4000 33FF	1 KB	IWDG
	0x4000 3400-0x4000 37FF	1 KB	Reserved
	0x4000 3800-0x4000 3BFF	1 KB	Reserved
	0x4000 4000-0x4000 43FF	1 KB	Reserved
	0x4000 4400-0x4000 47FF	1 KB	UART2
	0x4000 4800-0x4000 4BFF	3 KB	Reserved
	0x4000 5400-0x4000 57FF	1 KB	I2C1
	0x4000 5800-0x4000 5BFF	1 KB	Reserved
	0x4000 5C00-0x4000 5FFF	1 KB	Reserved
	0x4000 6000-0x4000 63FF	1 KB	Reserved
	0x4000 6400-0x4000 67FF	1 KB	Reserved
	0x4000 6800-0x4000 6BFF	1 KB	Reserved
	0x4000 6C00-0x4000 6FFF	1 KB	Reserved
	0x4000 7000-0x4000 73FF	1 KB	PWR
	0x4000 7400-0x4000 FFFF	35 KB	Reserved
	0x4001 0000-0x4001 03FF	1 KB	SYSCFG
	0x4001 0400-0x4001 07FF	1 KB	EXTI
	0x4001 0800-0x4001 23FF	7 KB	Reserved
	0x4001 2400-0x4001 27FF	1 KB	ADC1
	0x4001 2800-0x4001 2BFF	1 KB	Reserved
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1
	0x4001 3000-0x4001 33FF	1 KB	SPI1
	0x4001 3400-0x4001 37FF	1 KB	DBGMCU
	0x4001 3800-0x4001 3BFF	1 KB	UART1
	0x4001 3C00-0x4001 3FFF	1 KB	Reserved
	0x4001 4000-0x4001 43FF	1 KB	TIM14
	0x4001 4400-0x4001 47FF	1 KB	Reserved
	0x4001 4800-0x4001 4BFF	1 KB	Reserved
	0x4001 4C00-0x4001 7FFF	13 KB	Reserved
AHB	0x4002 0000-0x4002 03FF	1 KB	Reserved
	0x4002 0400-0x4002 0FFF	3 KB	Reserved
	0x4002 1000-0x4002 13FF	1 KB	RCC
	0x4002 1400-0x4002 1FFF	3 KB	Reserved
	0x4002 2000-0x4002 23FF	1 KB	Flash Interface
	0x4002 2400-0x4002 2FFF	3 KB	Reserved
	0x4002 3000-0x4002 33FF	1 KB	CRC
	0x4002 3400-0x4002 FFFF	47 KB	Reserved
	0x4003 0000-0x4003 03FF	1 KB	Reserved
	0x4003 0400-0x47FF FFFF	~127 MB	Reserved
	0x4800 0000-0x4800 03FF	1 KB	GPIOA
	0x4800 0400-0x4800 07FF	1 KB	GPIOB
	0x4800 0800-0x4800 0BFF	1 KB	Reserved

Bus	Address range	Size	Peripheral
	0x4800 0C00-0x4800 0FFF	1 KB	Reserved
	0x4800 1000-0x5FFF FFFF	~384 MB	Reserved

3.5 Flash

This product provides up to 32KB embedded Flash memory available for storing code and data.

3.6 SRAM

This product provides up to 2KB embedded SRAM.

3.7 NVIC

This product embeds a Nested vector interrupt controller (NVIC), able to handle multiple maskable interrupt channels (excluding the 16 interrupt lines of the Cortex-M0) and manage 16 programmable priority levels.

- Tightly coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector table address passed directly to the core.
- Tightly coupled NVIC interfaces.
- Allow early processing of interrupts.
- Support high priority interrupt preemption.
- Support interrupt tail-chaining.
- Automatically save processor status.
- Automatic restoration when the interrupt returns with no instruction overhead.

This module provides flexible interrupt management with minimal interrupt latency.

3.8 EXTI

The external interrupt/event controller (EXTI) contains multiple edge detectors to capture the level changes on the I/O ports and generate interrupt/event to CPU. All I/O ports are connected to 16 external interrupt lines. Each interrupt line can be independently enabled or disabled and configured to select the trigger mode (rising edge, falling edge or both edges). A pending register can save all the interrupt request status.

The EXTI can detect the level fluctuation of an external line with a pulse width shorter than the internal APB clock period.

3.9 Clock and boot

The system clock can be configured after chip power-on. After the power-on reset, the default clock is the internal 8MHz high speed oscillator (HSI). User can configure to use the external 4 to 24MHz crystal oscillator (HSE) as the system clock. The system will

automatically block the external clock source, turn off the PLL and use the internal oscillator when the external clock is detected to be invalid. Meanwhile, if the clock monitor interrupt is enabled, an interrupt request will be generated.

The clock system uses multiple pre-dividers to generate the clock for the AHB and APB bus. The maximum frequency of the AHB and APB bus clock can reach up to 48MHz.

3.10 Boot modes

During boot, BOOT0 pins and BOOT1 bit are used to select one of three boot options:

- Boot from embedded Flash
- Boot from system memory
- Boot from embedded SRAM

The Bootloader code locates in the system memory. Once the chip boots from the system memory, it will run the bootloader code and user can program the embedded Flash through UART1 port by using the bootloader.

3.11 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: I/O ports and internal voltage regulator are powered by the V_{DD} Pins.
- V_{DDA} = 2.0V ~ 5.5V: ADC, reset logic, oscillators, PLL are powered by the V_{DDA} pin. V_{DDA} and V_{SSA} can either be connected to V_{DD} and V_{SS} respectively or be powered individually. When powered individually, the power supply should be at the same voltage level as the V_{DD} and V_{SS}.

3.12 Power supply supervisors

This product integrates the power-on reset (POR) and power-down reset (PDR) circuit. This circuit is workable in all power modes, to make sure the chip can work above the lowest power supply voltage. When the V_{DD} is lower than the preset threshold (V_{POR}/V_{PDR}), this circuit will put system to reset status, without need of an external reset circuit.

This product also integrates a programmable voltage monitor (PVD), it can monitor the V_{DD} and V_{DDA} voltage, and compare it with the preset threshold V_{PVD}. When V_{DD} is lower or higher than V_{PVD}, an interrupt request can be generated, then the interrupt handler can send out warning information or put the chip into safe mode. The PVD function can be configured to be enable through user program.

3.13 Voltage regulator

The on-chip voltage regulator can regulate the external supply voltage to a lower and stable supply voltage that can be served by the internal circuits. The voltage regulator is workable after the chip power-on reset (POR).

3.14 Low power mode

This product supports multiple low power modes, user can select the low power modes according to their end application to achieve a balance between power consumption, wakeup time and wakeup source.

Sleep mode

In sleep mode, only the CPU clock is gated off. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

In stop mode, low power consumption can be achieved with all RAM and registers content in retention. In stop mode, HSI and HSE are powered off. The microcontroller can be woken up by the EXTI signals. EXTI signals can come from the 16 external I/O ports or PVD output.

Deep stop mode

Similar as stop mode, but with lower power consumption.

Standby mode

In standby mode, the lowest power consumption can be achieved. In this mode, the voltage regulator is powered off, and all the 1.5V domain are shut down. PLL, HSI and HSE are also powered off. Wakeup sources include rising edge on WKUP pin, active reset on NRST pin or IWDG reset. SRAM and registers content are lost in this mode. Only backup register and standby circuit are powered.

3.15 Timers and watchdogs

This product has one advanced timer, two general purpose timers, three basic timers, two watchdog timers and one Systick timer. The table below compares the features of advanced, general purpose and basic timers.

Table 3-2 Feature summary of advanced, general purpose and basic timers

Type	Instance	Resolution	Counter direction	pre-divider	DMA request	Capture/compare channels	Complementary output
Advanced	TIM1	16-bit	up, down, up/down	1 to 65536	Yes	4	Yes
General purpose	TIM3	16-bit	up, down, up/down	1 to 65536	Yes	4	No
Basic	TIM14	16-bit	up	1 to 65536	Yes	No	No

Advanced timer (TIM1)

The advanced timer includes a 16-bit counter, four capture/compare channels and three phases complementary PWM generator. This timer supports hardware dead-time insertion when using as complementary PWM generator. This timer can also be used as a full-function general purpose timer. This timer has four independent channels, each channel

can be used for:

- Input capture
- Output compare
- PWM generator (center- or edge-aligned)
- Single pulse output

When this timer is used as a general-purpose timer, it has the same function as the TIM3. When this timer is used as a 16-bit PWM generator, it can be configured to a broad duty cycle range from 0% to 100%.

The advanced timer has lots of identical features and internal structures as the general-purpose timer, in this way the advanced timer can work together with the general-purpose timer through the link function, to provide synchronization and event trigger function.

In debug mode, the counter stops counting, and PWM output will be disabled.

General-purpose timer (TIMx)

This product has one general-purpose timer (TIM3). The timer has a 16-bit counter, support both up and down counting, with automatically reload. The timer also has a 16-bit frequency pre-divider and four independent channels. Each channel can be used as input capture, output compare, PWM or single pulse output.

These general-purpose timers can also work together through the timer link function, to provide synchronization between timers and event trigger function.

Any general-purpose timer can be used to generate PWM output or work as basic timer.

These timers can also be used to decode incremental encoder signals and can also be used to decode one to four Hall sensors' digital output.

In debug mode, the counter stops counting, and PWM output will be disabled.

Basic timer (TIM14)

The basic timer is based on a 16-bit up counter and a 16-bit prescaler. In debug mode, the counter stops counting.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an internal independent 40KHz oscillator. Because this oscillator is independent of the main clock, it can run in shutdown and standby modes. It can be used to reset the entire system when a system error occurs or as a free timer to provide timeout management for applications. It can be configured to start the watchdog by software or hardware through the option byte. In debug mode, the counter stops counting.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down counter, and it can be set to free-running. It can be used as a watchdog to reset the entire system when an system error occurs. It is clocked by the main clock and has an early warning interrupt function; in debug mode, the counter stops counting.

System tick timer (Systick)

This timer is dedicated to the real-time operating system and can also be used as a general down counter. It has the following features:

- 24-bit down counter
- Support auto reload
- A maskable interrupt can be generated when counter value is 0
- Programmable clock source

3.16 Backup registers

This product has twenty 16-bit backup registers that can be used to store user application data. They are in the backup domain. They will not be reset when the system is woken up from standby mode, or when there is a system reset or power reset.

3.17 GPIO

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripherals function port. Most GPIO pins are shared with digital or analog functions. If necessary, the peripheral functions of the I/O pins can be locked by specific operation to avoid accidental writing to the I/O register.

3.18 UART

This product series has up to two UART interfaces. The UART interface supports configurable data length of 5-, 6-, 7-, 8-, and 9-bits. The UART interface also supports LIN master and slave function and ISO7816 smart card mode.

3.19 I2C

This product series has up to one I2C interface. The I2C bus interface can work in multi-master mode or slave mode and supports standard and fast mode. The I2C interface supports 7-bit or 10-bit addressing.

3.20 SPI

This product series has up to one SPI interfaces. The SPI interface can be configured as 1 to 32 bits per frame in master or slave mode. The highest speed of master mode is 24 Mbps, and the highest speed of slave mode is 12 Mbps.

3.21 I2S

This product has up to two I2S interfaces shared with the SPI module. The I2S module shares three pins with SPI, supports half-duplex communication (transmitter or receiver

only), master or slave operation, underflow flag in transmit mode (only slave), and overflow flag in receive mode (master and slave mode) and frame error flag in receive and transmit mode (only slave). 8-bit programmable linear prescaler is used to achieve precise audio sampling frequency from 8KHz to 192KHz. The data format can be 16-bit, 24-bit or 32-bit, and the data packet frame is fixed at 16-bit (16-bit data frame) or 32-bit (16-bit, 24-bit or 32-bit data frame).

3.22 ADC

This product has a 12-bit analog/digital converter (ADC), with up to 8 external channels available, which can realize single-shot single-cycle and continuous scan conversion. In the scan mode, the conversion of the sampling value on the selected group of analog inputs is automatically performed.

The analog watchdog function allows very precise monitoring of one or all selected channels. When the monitored signal exceeds a preset threshold, an interrupt will be generated. The triggers generated by the general-purpose timers (TIMx) and the advanced timers can be selected to trigger the ADC sampling, in this way the ADC sampling can be synchronized with the timer.

3.23 CRC

The cyclic redundancy check (CRC) module uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a method to detect flash memory errors. The CRC module can be used to calculate the signature of the software package in real time and compare it with the signature generated when the software is linked and generated.

3.24 SWD

This product equips ARM standard two-wire serial debug interface (SWD).

4 Pinout and assignment

4.1 Pinout diagram

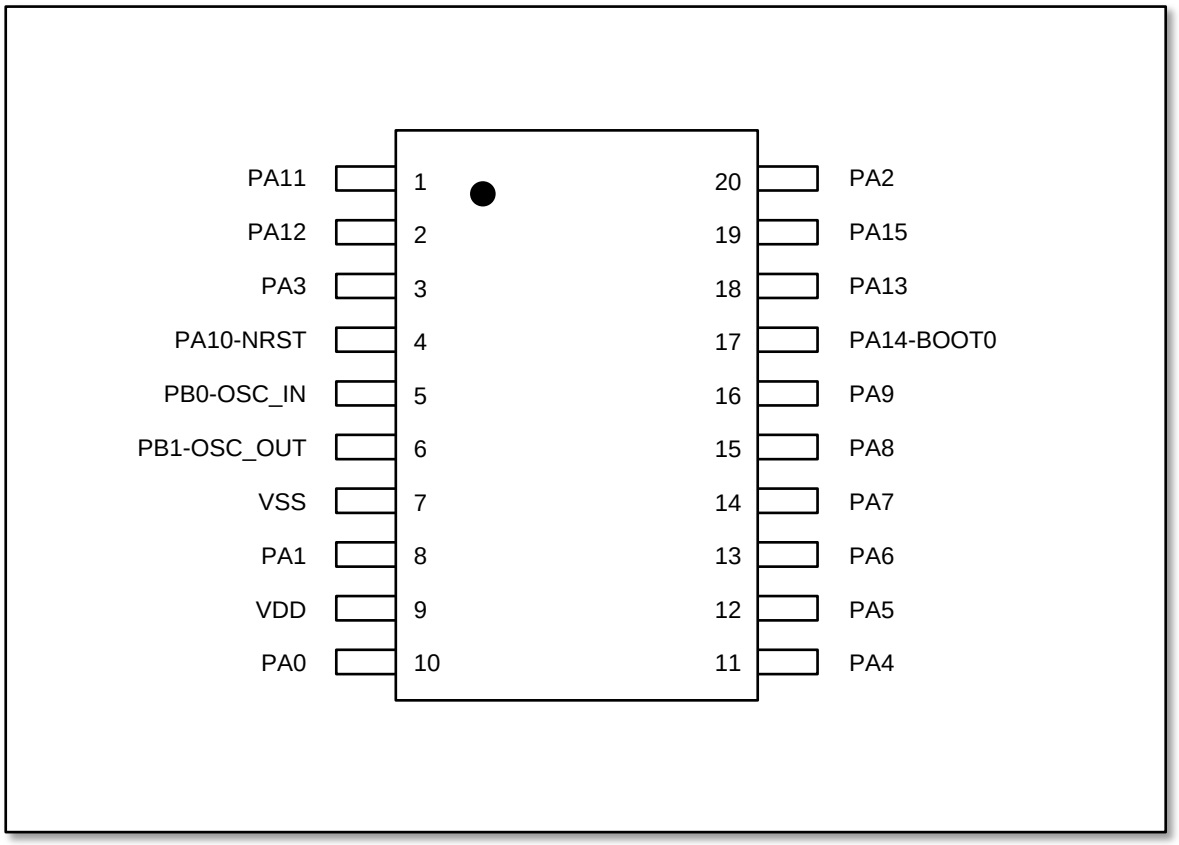

Figure 4-1 TSSOP20 pinout diagram

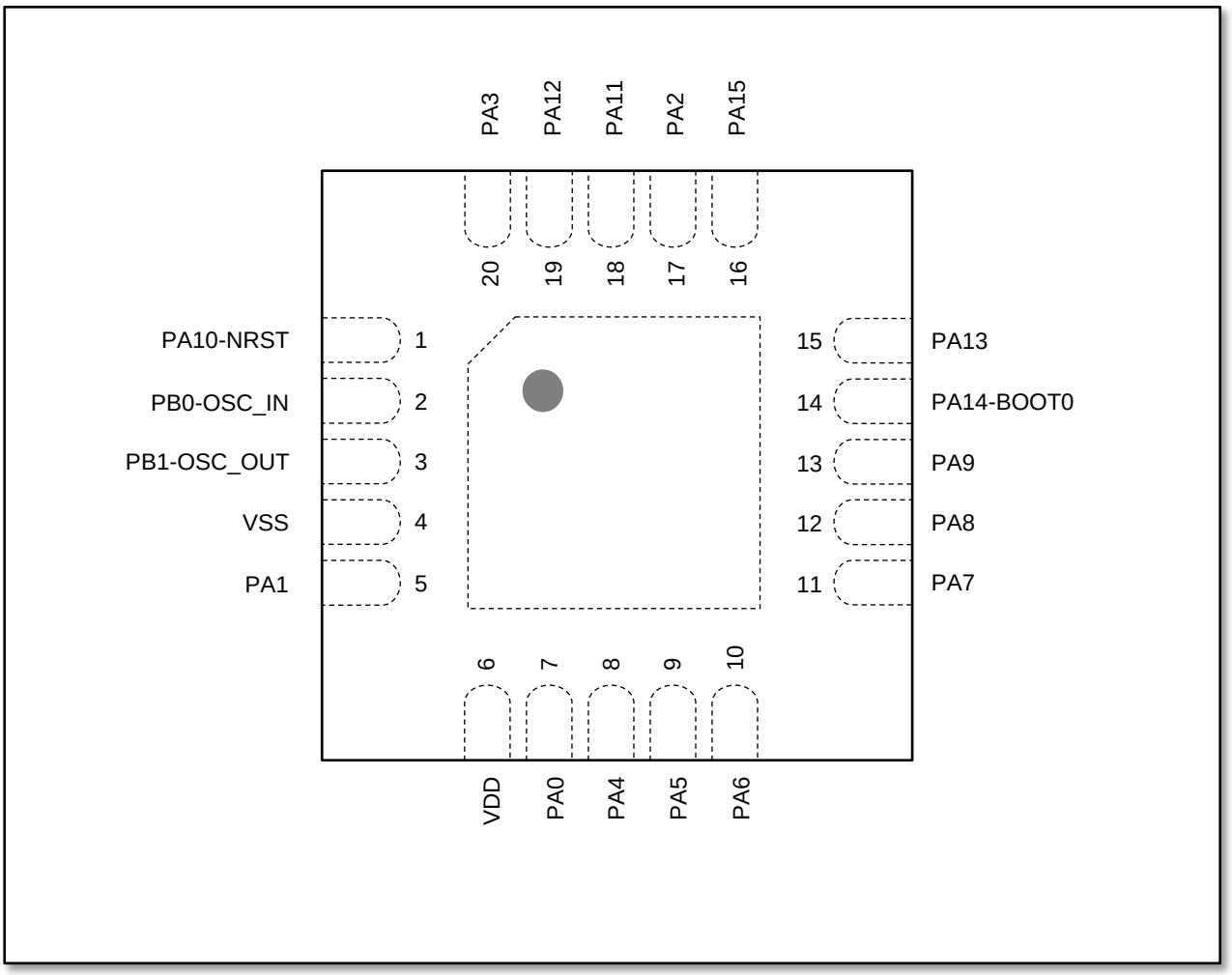

Figure 4-2 QFN20 pinout diagram

4.2 Pin assignment

Table 4-1 Pin assignment table

Pin ID		Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
QFN20	TSSOP20						
1	4	PA10 NRST	I/O	TC	PA10	UART1_TX	-
2	5	PB0 OSC_IN	I/O	TC	PB0	-	ADC1_VIN[1]
3	6	PB1 OSC_OUT	I/O	TC	PB1	-	ADC1_VIN[0]
4	7	VSS	S	-	VSS	-	-
5	8	PA1	I/O	TC	PA1	SPI_MISO UART2_TX I2C_SDA	-
6	9	VDD	S	-	VDD	-	-
7	10	PA0	I/O	TC	PA0	SPI_NSS UART1_RX TIM1_CH3N I2C_SCL TIM3_CH3	-
8	11	PA4	I/O	TC	PA4	TIM1_BKIN I2C_SDA	-
9	12	PA5	I/O	TC	PA5	SPI_SCK I2C_SCL	-
10	13	PA6	I/O	TC	PA6	SPI_MOSI TIM1_CH1 TIM1_CH1N TIM1_CH3	-
11	14	PA7	I/O	TC	PA7	SPI_MISO TIM1_CH1N TIM1_CH2N MCO TIM1_CH4	ADC1_VIN[7]
12	15	PA8	I/O	TC	PA8	SPI_SCK TIM1_CH2 TIM3_CH1	-
13	16	PA9	I/O	TC	PA9	SPI_MOSI TIM1_CH2N TIM1_CH1 TIM14_CH1	-
14	17	PA14 BOOT0	I/O	TC	PA14	SWDCLK TIM1_CH3 TIM1_CH2 SPI_MISO UART1_TX	-
15	18	PA13	I/O	TC	PA13	SWDIO UART1_RX UART2_RX I2C_SCL	-
16	19	PA15	I/O	TC	PA15	SPI_NSS TIM1_CH3N TIM3_CH3	ADC1_VIN[6]
17	20	PA2	I/O	TC	PA2	TIM1_CH2N TIM3_CH2	ADC1_VIN[5]

Pin ID		Name	Type(1)	I/O level(2)	Main function	Multiplex function	Additional function
QFN20	TSSOP20						
18	1	PA11	I/O	TC	PA11	TIM1_CH2 TIM14_CH1 TIM3_CH1	ADC1_VIN[4]
19	2	PA12	I/O	TC	PA12	UART1_TX	ADC1_VIN[3]
20	3	PA3	I/O	TC	PA3	UART1_RX	ADC1_VIN[2]

1. I = input, O = output, S = power pins, HiZ = high resistance state.
2. TC: standard IO. Input signal level should not exceed VDD.

4.3 Pin multiplexing

Table 4-2 PA port multiplexing AF0-AF4

Pin	AF0	AF1	AF2	AF3	AF4
PA0	SPI_NSS/I2S_WS	UART1_RX	TIM1_CH3N	I2C_SCL	TIM3_CH3
PA1	SPI_MISO/I2S_MCK	-	UART2_TX	I2C_SDA	-
PA2	-	-	TIM1_CH2N	-	TIM3_CH2
PA3	-	UART1_RX	-	-	-
PA4	-	-	TIM1_BKIN	I2C_SDA	-
PA5	SPI_SCK/I2S_CK	-	-	I2C_SCL	-
PA6	SPI_MOSI/I2S_SD	TIM1_CH1	TIM1_CH1N	-	TIM1_CH3
PA7	SPI_MISO/I2S_MCK	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4
PA8	SPI_SCK/I2S_CK	TIM1_CH2	-	-	TIM3_CH1
PA9	SPI_MOSI/I2S_SD	TIM1_CH2N	TIM1_CH1	TIM14_CH1	-
PA10	-	UART1_TX	-	-	-
PA11	-	-	TIM1_CH2	TIM14_CH1	TIM3_CH1
PA12	-	UART1_TX	-	-	-
PA13	SWDIO	UART1_RX	UART2_RX	I2C_SCL	-
PA14	SWDCLK	TIM1_CH3	TIM1_CH2	SPI_MISO/I2S_MCK	UART1_TX
PA15	SPI_NSS/I2S_WS	TIM1_CH3N	-	-	TIM3_CH3

Table 4-3 PB port multiplexing AF0-AF5

Pin	AF0	AF1	AF2	AF3	AF4
PB0	-	-	-	-	-
PB1	-	-	-	-	-

5 Package dimensions

5.1 QFN20

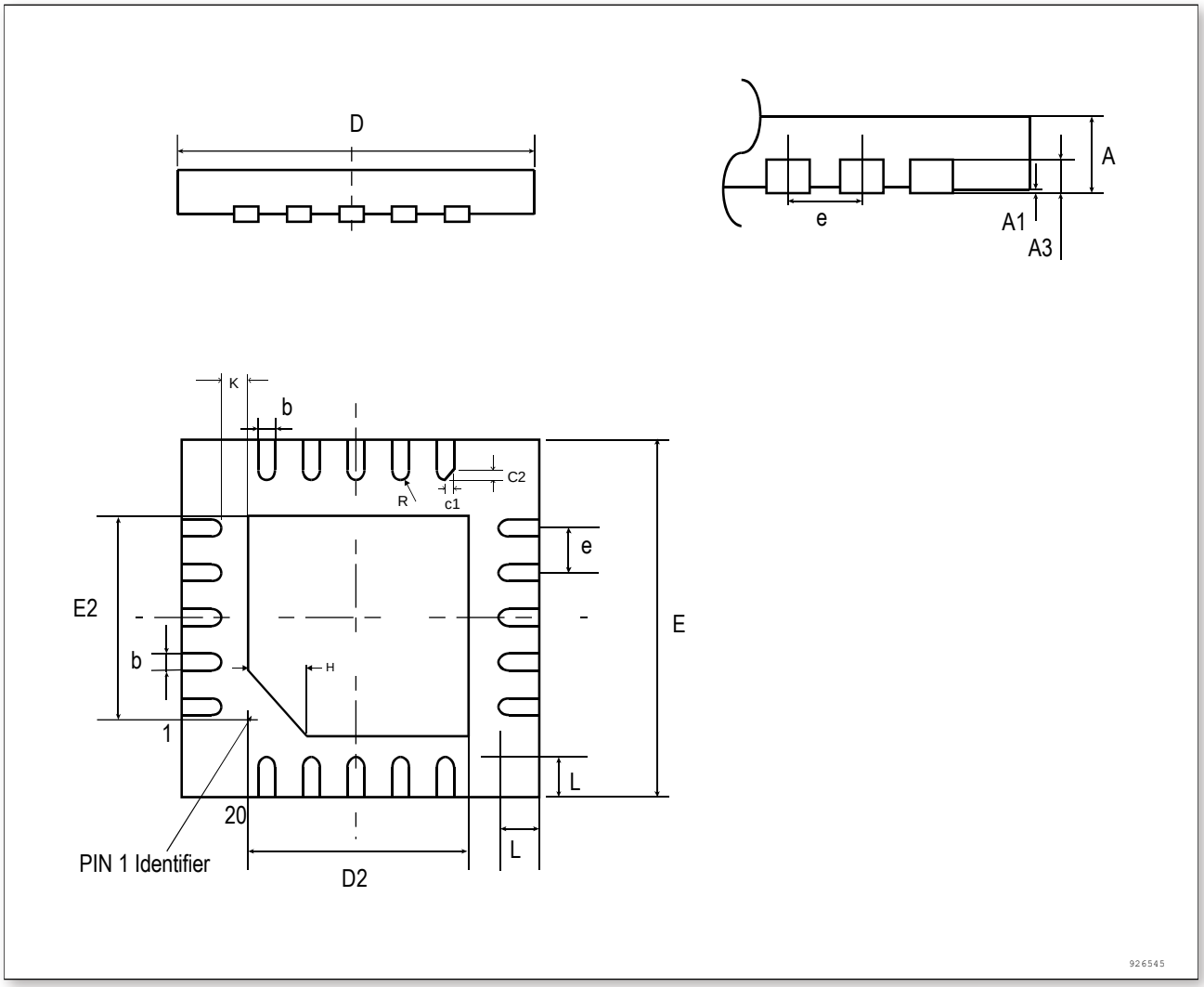

Figure 5-1 QFN20 package dimension

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Package dimensions

Table 5-1 QFN20 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e		0.40	
H		0.35REF	
K		0.40REF	
L	0.25	0.35	0.45
R	0.075		

5.2 TSSOP20

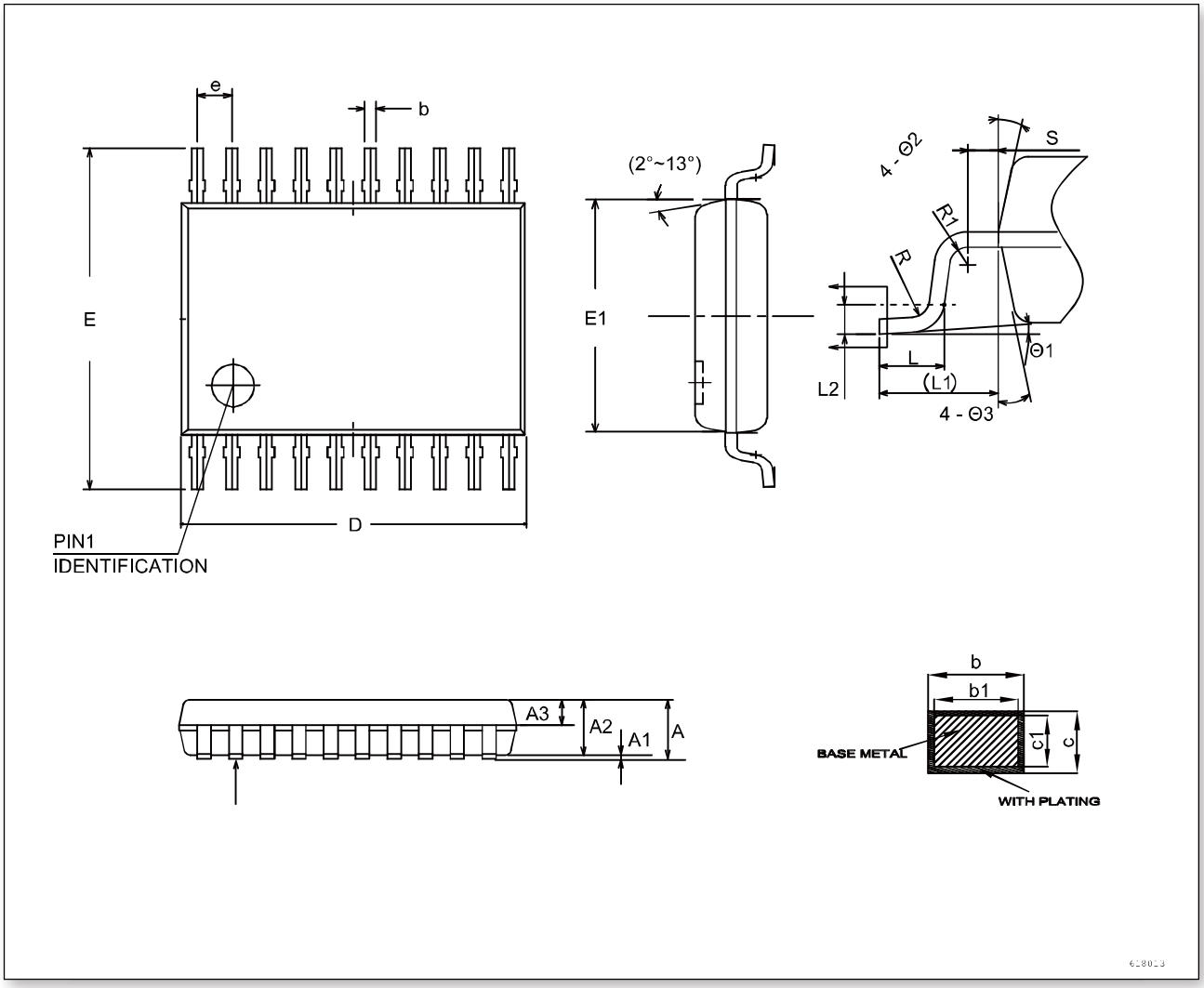

Figure 5-2 TSSOP20 package dimension

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

Package dimensions

Table 5-2 TSSOP20 package dimension details

ID	Millimeters		
	Minimum	Typical	Minimum
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50
E	6.25	6.40	6.55
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0◦	-	8◦

6 Part identification

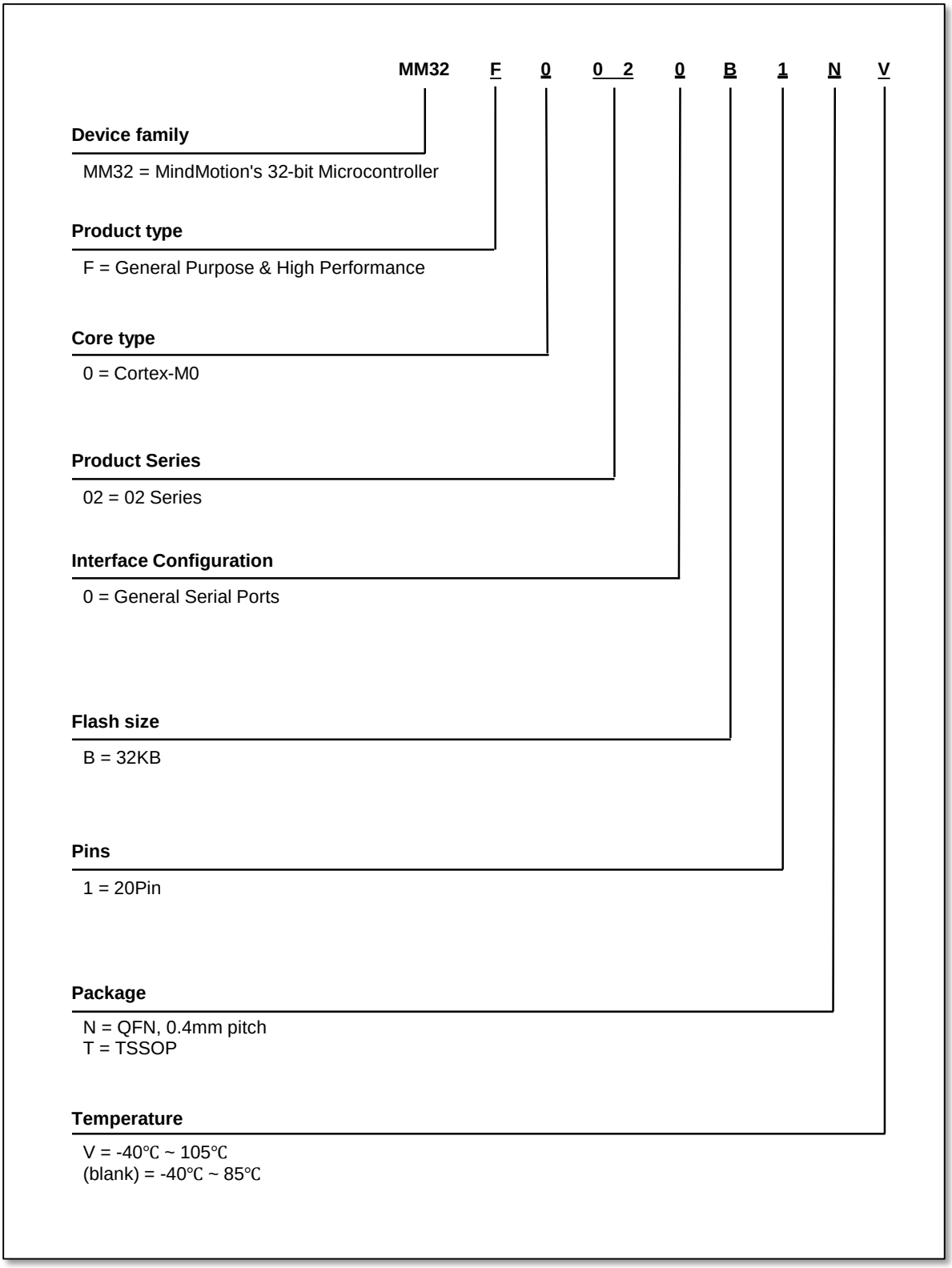

Figure 6-1 Part number naming rule

7 Revision history

Date	Revision	Description
2021/06/29	Rev1.0	Initial release