Adjustable Low Dropout 300mA Linear Regulator

Features

- **Wide Operating Voltage: 2.9 ~ 5.5V**
- **Low Dropout Voltage:**
  300mV(Typical) @ 300mA
- **Guaranteed 300mA Output Current**
- **Adjustable Output Voltage: 0.8 ~ 5V**
- **Current-Limit Protection with Foldback Current**
- **Over-Temperature Protection**
- **Stable with Low ESR Ceramic Capacitor**
- **SOT-23-5 Package**
- **Lead Free and Green Devices Available**
  (RoHS Compliant)

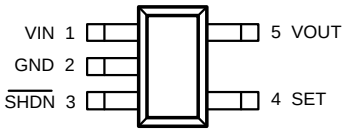
Applications

- **Cellular Phones**
- **Portable and Battery-Powered Equipment**
- **Notebook and Personal Computers**

General Description

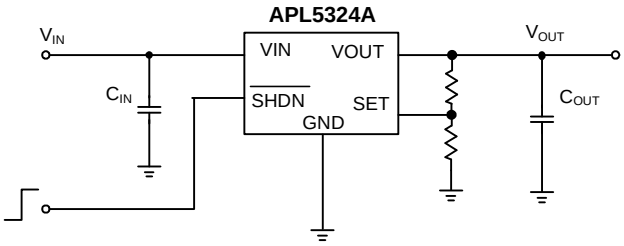
The APL5324A is a P-channel low dropout linear regulator which needs only one input voltage from 2.9 to 5.5V, and delivers current up to 300mA to set output voltage. It also can work with low ESR ceramic capacitors and is ideal for using in the battery-powered applications such as notebook computers and cellular phones. Typical dropout voltage is only 300mV at 300mA loading.
Current limit with current foldback and thermal shutdown functions protect the device against current over-loads and over temperature. The APL5324A is available in a SOT-23-5 package.

Pin Configuration



SOT-23-5

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL5324A □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code B: SOT-23-5 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APL5324A B : 24RX	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 6.5	V
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Voltage ($\overline{SHDN}$ to GND)	-0.3 ~ 6.5	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance-Junction to Ambient (Note 2) SOT-23-5	240	°C/W
θ_{JC}	Thermal Resistance-Junction to Case SOT-23-5	130	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	2.9 ~ 5.5	V
V_{OUT}	Output Voltage	0.8 ~ 5	V
I_{OUT}	VOUT Output Current	0 ~ 300	mA
C_{IN}	Input Capacitor	0.22 ~ 100	µF
C_{OUT}	Output Capacitor	1.5 ~ 100	µF
T_J	Junction Temperature	-40 ~ 125	°C

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN} = V_{OUT}+1V, I_{OUT}=0~300mA, C_{IN} = 1µF, C_{OUT} = 2.2µF, T_A = -40 to 85°C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APL5324A			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.9	-	5.5	V
V_{OUT}	Output Voltage Range		0.8	-	5	V
I_Q	Quiescent Current	I_{OUT}=10mA~300mA	-	135	160	µA
V_{REF}	Reference Voltage	Measured on SET, V_{IN}=3V, I_{OUT}=10mA	-	0.8	-	V
	Output Voltage Accuracy	I_{OUT}=10mA	-2	-	+2	%
REG_{LINE}	Line Regulation	ΔV_{OUT}%/ΔV_{IN}, I_{OUT}=10mA	-0.06	-	+0.06	%/V
REG_{LOAD}	Load Regulation	ΔV_{OUT}%/ΔI_{OUT}	-0.2	-	+0.2	%/A
V_{DROP}	Dropout Voltage	V_{OUT}= 2.5V, I_{OUT} = 300mA	-	500	650	mV
		V_{OUT} = 3.3V, I_{OUT} = 300mA	-	300	400	
PSRR	Power Supply Ripple Rejection Ratio	f = 10kHz, I_{OUT} = 300mA	-	35	-	dB
	Noise	f = 80Hz to 100kHz, I_{OUT} = 300mA	-	160	-	μV_{RMS}
I_{LIMIT}	Current Limit		400	550	-	mA
I_{SHORT}	Foldback Current	V_{OUT}= 0V	-	45	-	mA
	$\overline{SHDN}$ Input Voltage High		1.6	-	-	V
	$\overline{SHDN}$ Input Voltage Low		-	-	0.4	
	V_{OUT} Discharge MOSFET $R_{DS(ON)}$	$\overline{SHDN}$ = Low	-	60	-	Ω
	Shutdown VIN Supply Current	$\overline{SHDN}$ = Low, V_{IN}= 5.5V	-	0.1	1	µA
	Over Temperature Threshold		-	140	-	°C
	Over Temperature Hysteresis		-	40	-	°C
	SET Input Bias Current	V_{SET}=0.8V	-100	-	100	nA

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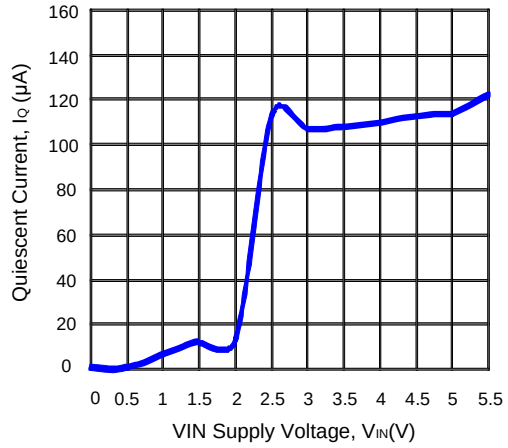
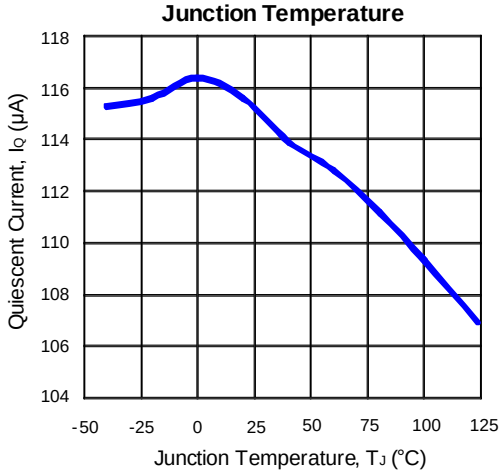
Typical Operating Characteristics

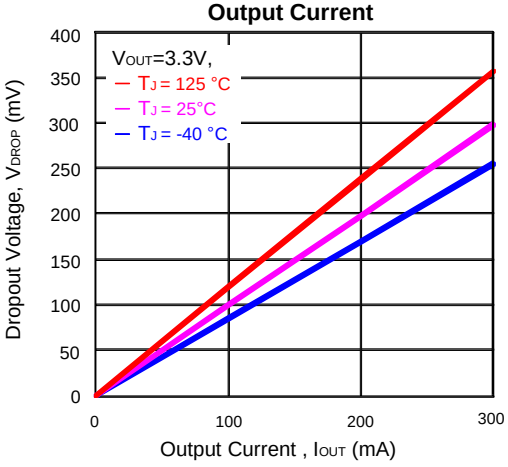
Quiescent Current vs. VIN Supply Voltage



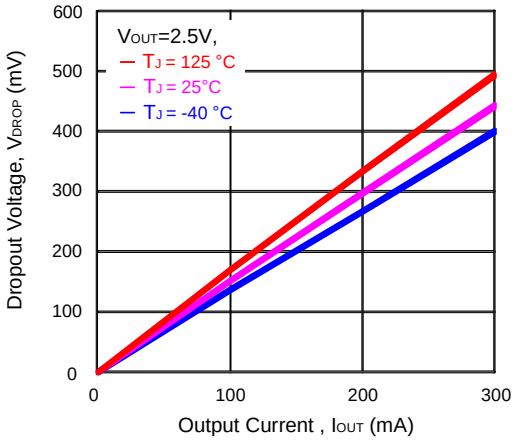
Quiescent Current vs. Junction Temperature



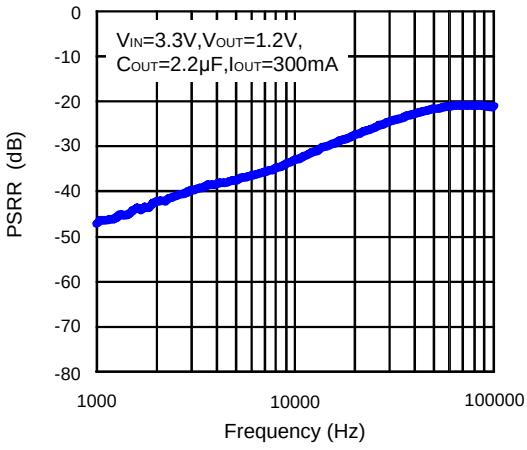
Dropout Voltage vs. Output Current



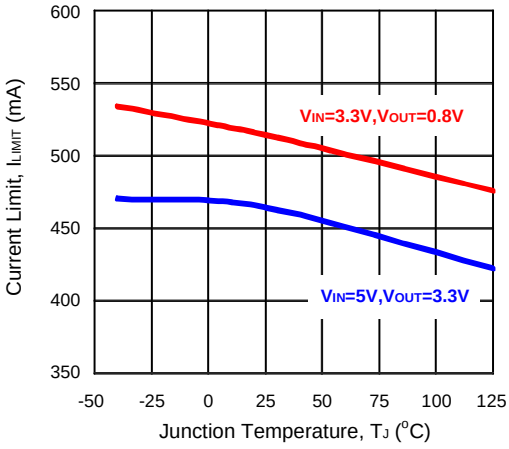
Dropout Voltage vs. Output Current



PSRR vs. Frequency



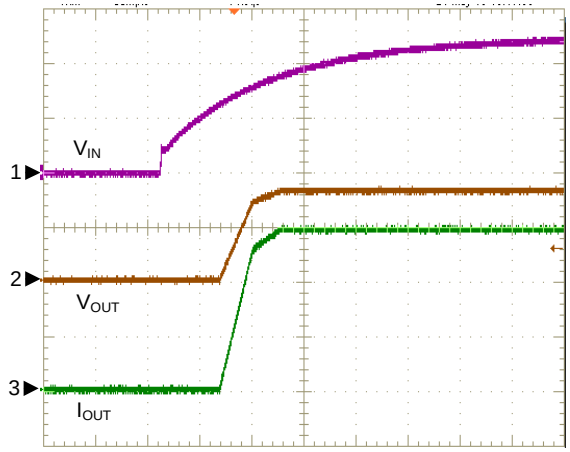
Current Limit vs. Junction Temperature



Operating Waveforms

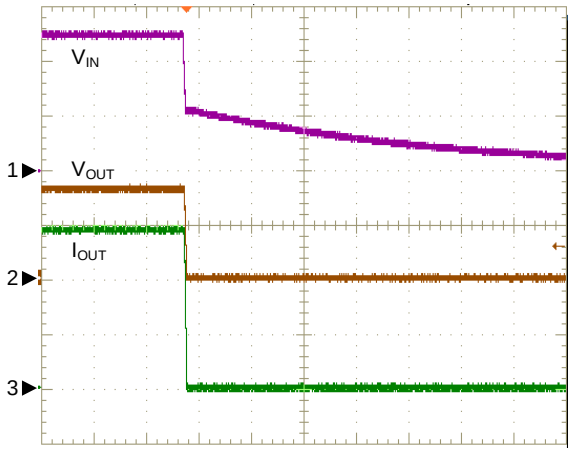
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

VIN Power ON



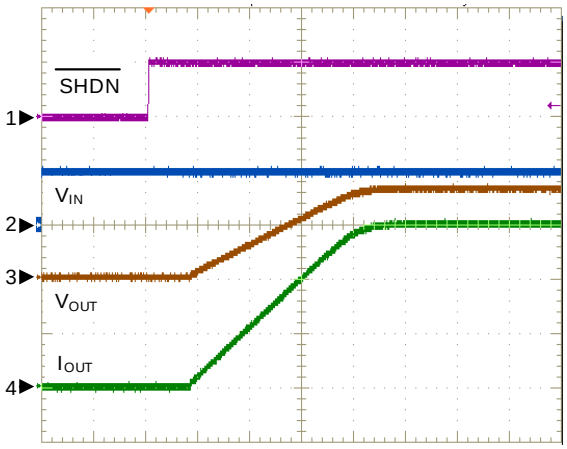
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 1ms/Div

VIN Power OFF



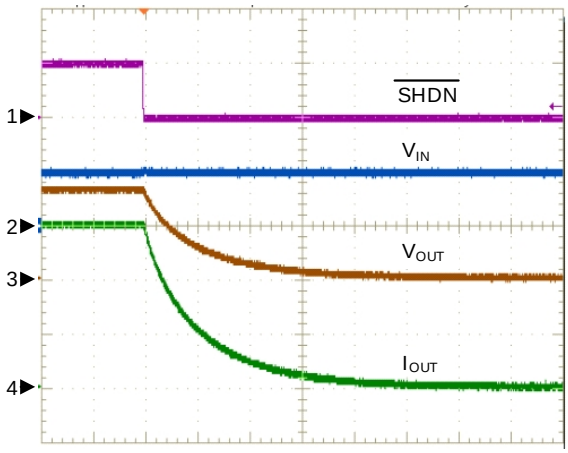
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 100mA/Div, DC
TIME: 40ms/Div

Enable Power ON



CH1: $\overline{SHDN}$, 5V/Div, DC
CH2: V_{IN}, 5V/Div, DC
CH3: V_{OUT}, 2V/Div, DC
CH4: I_{OUT}, 100mA/Div, DC
TIME: 200µs/Div

Enable Shutdown



CH1: $\overline{SHDN}$, 5V/Div, DC
CH2: V_{IN}, 5V/Div, DC
CH3: V_{OUT}, 2V/Div, DC
CH4: I_{OUT}, 100mA/Div, DC
TIME: 20µs/Div

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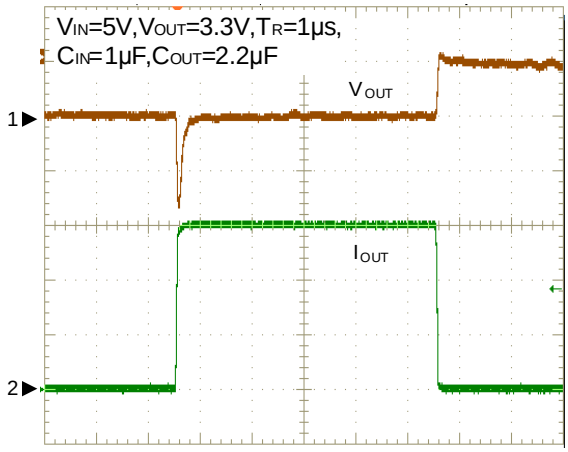
Operating Waveforms (Cont.)

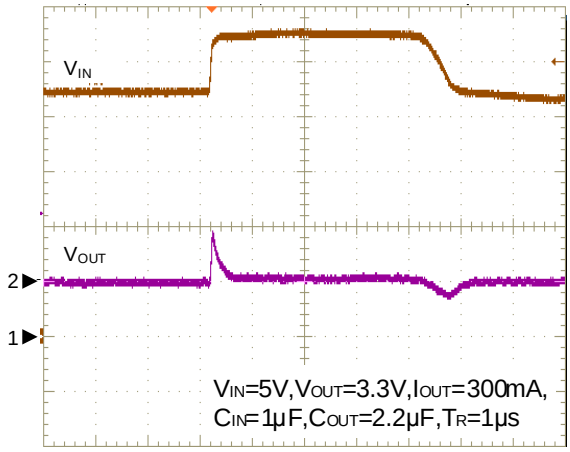
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Load Transient



CH1: V_{OUT}, 50mV/Div, DC
CH2: I_{OUT}, 100mA/Div, DC
TIME: 20µs/Div

Line Transient

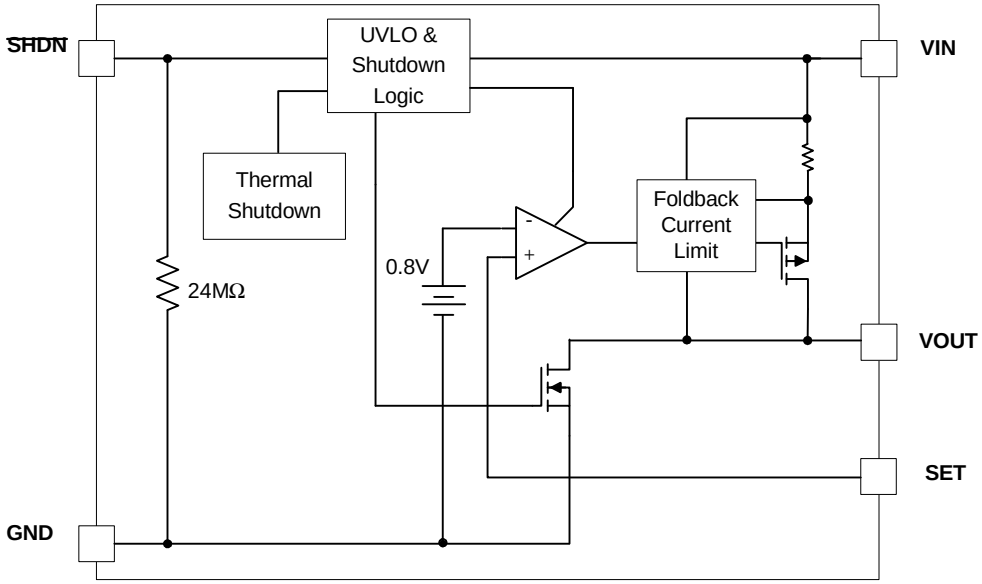


CH1: V_{IN}, 1V/Div, DC
CH2: V_{OUT}, 50mV/Div, DC
TIME: 40µs/Div

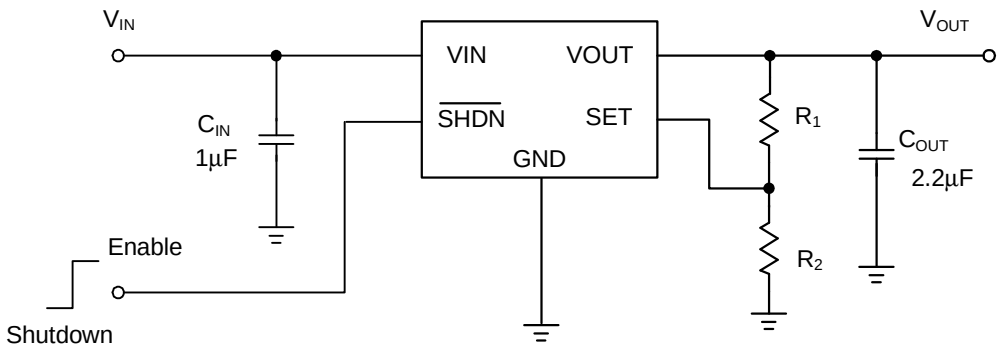
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Voltage supply input pin.
2	GND	Ground pin.
3	$\overline{SHDN}$	Shutdown control pin, logic high : enable ; logic low : shutdown.
4	SET	Connect this pin to an external resistor divider to adjust output voltage.
5	VOUT	Regulator output pin.

Block Diagram



Typical Application Circuit



$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Designation	Supplier	Part Number	Specification
C_{IN}	Murata	GRM185R61A105KE36	0603, X5R, 10V, 1µF
C_{IN}	Murata	GRM188R71A105KA61	0603, X7R, 10V, 1µF
C_{OUT}	Murata	GRM188R61A225KE34	0603, X5R, 10V, 2.2µF
C_{OUT}	Murata	GRM188R71A225KE15	0603, X7R, 10V, 2.2µF

Reference: www.murata.com

Function Description

Output Voltage Regulation

The APL5324A is an adjustable low dropout linear regulator. The output voltage set by the resistor-divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

Where R1 is connected from VOUT to SET with Kelvin sensing and R2 is connected from SET to GND. The recommended value of R2 is in the range of 100 to100kΩ. An error amplifier works with a temperature compensated 0.8V reference and an output PMOS regulates the output to the presetting voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output PMOS which provides load current from VIN to VOUT.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5324A. When the junction temperature exceeds +140°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature is cooled down by 40°C. The thermal shutdown is designed with a 40°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device.
For normal operation, device power dissipation should be externally limited so that junction temperature will not exceed 125°C.

Shutdown Control

The APL5324A has an active-low shutdown function. Force $\overline{SHDN}$ high (>1.6V) enables the V_{OUT}; force $\overline{SHDN}$ low (<0.4V) disables the V_{OUT}. SHDN is internally pulled low by a resistor (24MΩ typical). If it is not used, connect to VIN for normal operation.

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Application Information

Input Capacitor

The APL5324A requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping . Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limit the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 1µF and a minimum ceramic capacitor of 1µF is necessary.

Output Capacitor

The APL5324A needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 2.2µF. With X5R and X7R dielectrics, 2.2µF is sufficient at all operating temperatures. Large output capacitor value can reduce noise and improve load-transient response and PSRR, however, it also affects power on issue. Equation (1) shows the relationship between the maximum C_{OUT} value and the V_{OUT}.

$$C_{OUT(max)} = 101 - \frac{19.5}{V_{OUT}}$$

Where the unit of C_{OUT} is µF and V_{OUT} is V. Figure 1 shows the curve of maximum output capacitor over the output voltage. The output voltage range is from 0.8 to 5V and the output capacitor value should under the line. Output capacitors must be placed at the load and the ground pin as close as possible and the impedance of the layout must be minimized.

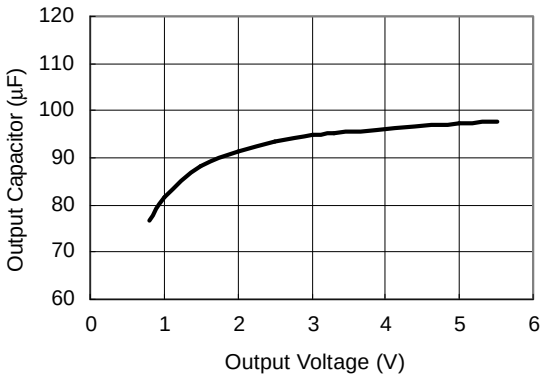

Figure 1

Operation Region and Power Dissipation

The APL5324A maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the T_A=25°C and maximum T_J=140°C (typical thermal limit threshold), the maximum power dissipation for SOT-23-5 is calculated as:

$$P_{D(max)}=(140-25)/240 = 0.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of T_J = 125 °C. The calculated power dissipation for SOT-23-5 should less than:

$$P_D=(125-25)/240 = 0.41(W)$$

The GND provides an electrical connection to the ground and channels heat away. Connect the GND to the ground by using a large pad or a ground plane.

Layout Consideration

Figure 2 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Ceramic capacitors for load must be placed near the load as close as possible.
3. To place APL5324A and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 2, must have wide tracks.
5. Divider resistor R1 and R2 must be placed near the SET as close as possible.

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Application Information (Cont.)

Layout Consideration (Cont.)

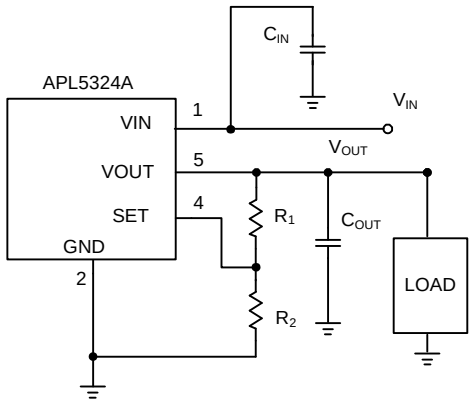
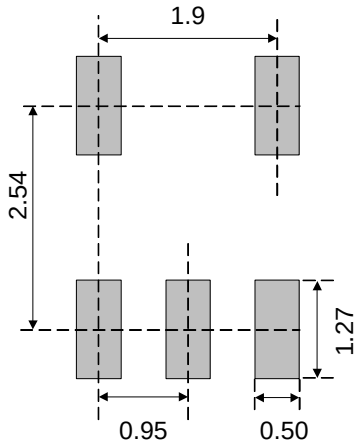


Figure 2

Recommended Minimum Footprint

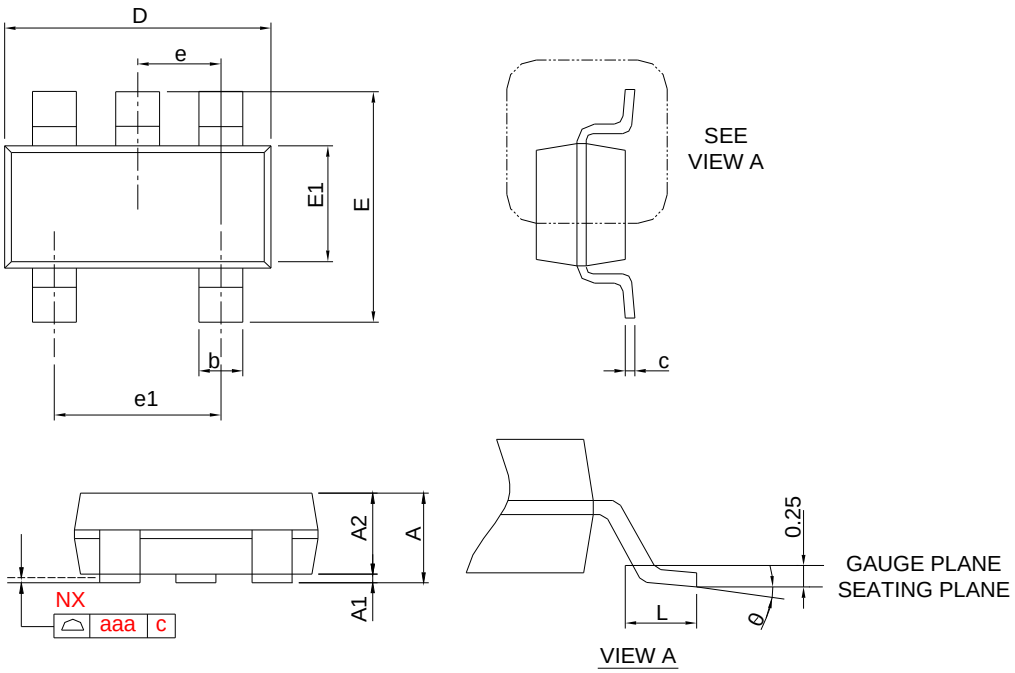
SOT-23-5



Unit : mm

Package Information

SOT-23-5



SYMBOL	SOT-23-5					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		1.16	1.45		0.046	0.057
A1	0.00	0.05	0.15	0.000	0.002	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.38	0.50	0.012	0.015	0.020
c	0.08	0.17	0.22	0.003	0.007	0.009
D	2.70	2.93	3.10	0.106	0.115	0.122
E	2.60	2.83	3.00	0.102	0.111	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037BSC		
e1	1.90 BSC			0.075BSC		
K	0.30	0.45	0.60	0.012	0.018	0.024
θ	0°	4°	8°	0°	4°	8°
aaa	0.10			0.004		

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

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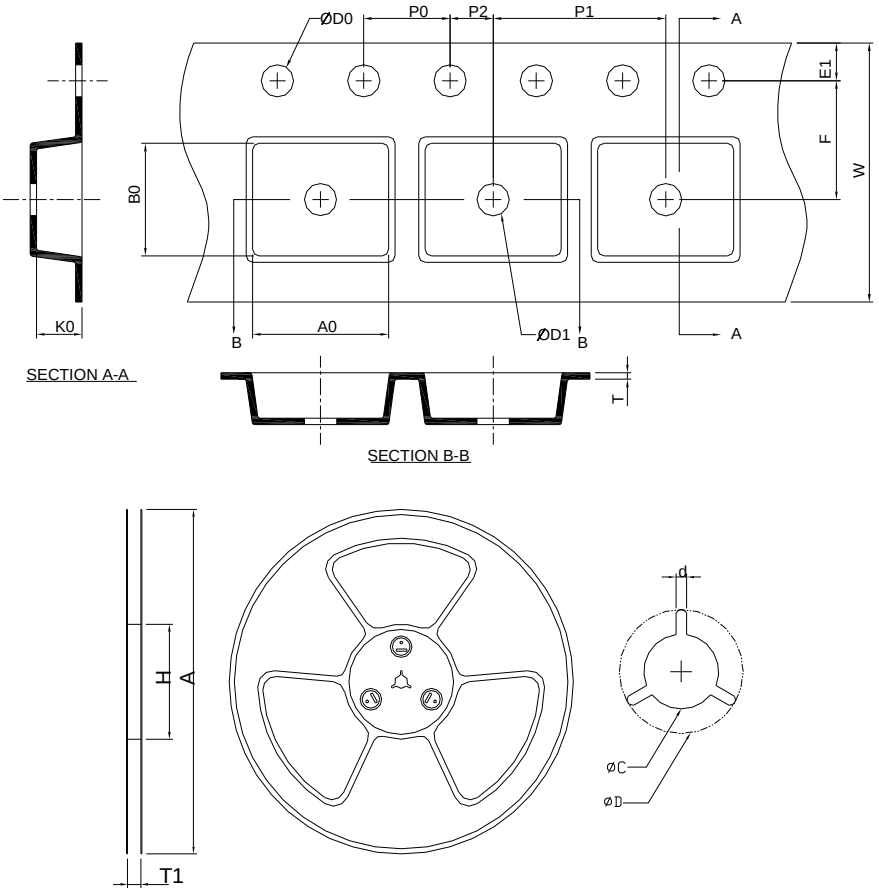
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000

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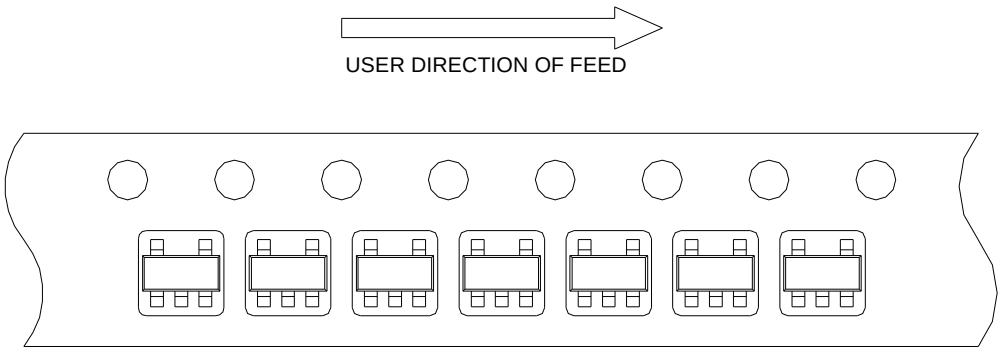
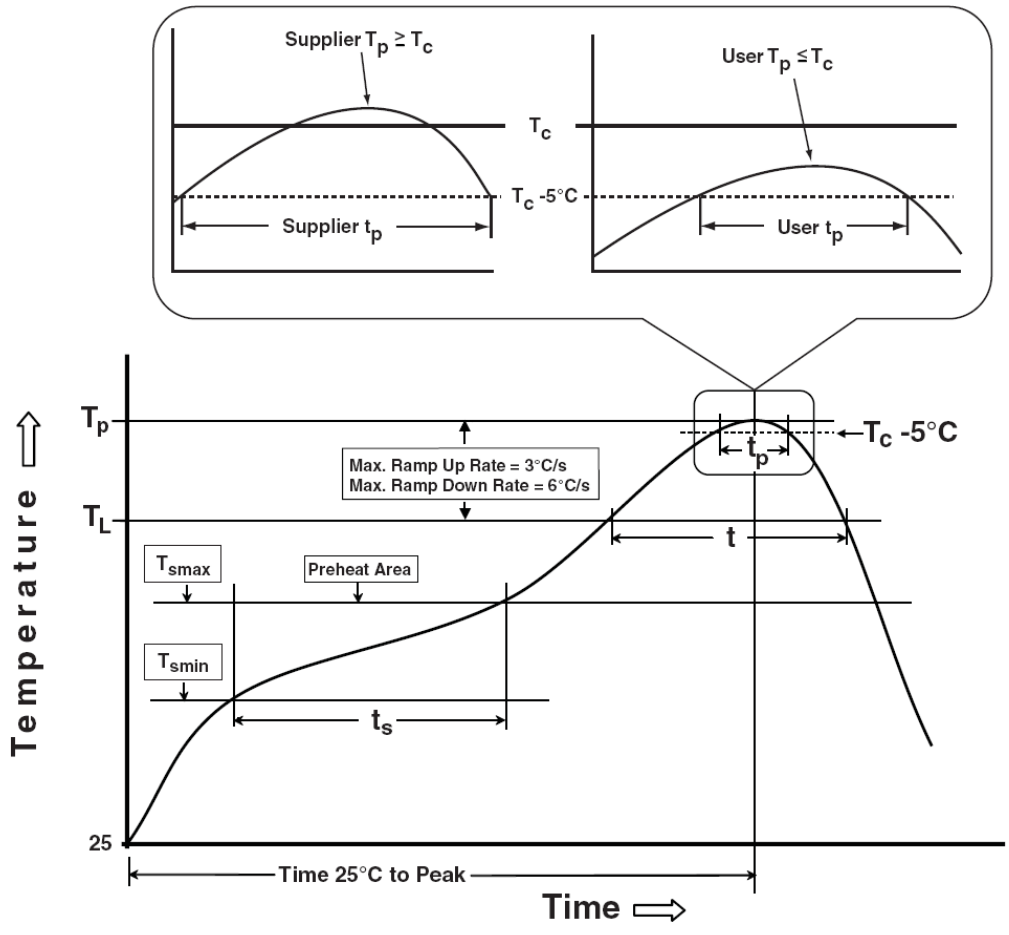
Taping Direction Information

SOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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