

Features

- **Excellent Reference Voltage Regulations**
 - 0.8V Internal Reference
 - ±1% Over Line Voltage and Temperature Range
- **Integrated Soft-Start**
- **Fixed 200kHz Operation Frequency**
- **Voltage Mode PWM Operation with Up to 90% (Max.) Duty Cycle**
- **Under-Voltage Protection**
- **Adjustable Over-Current Protection Threshold**
 - Using the $R_{DS(ON)}$ of Low-Side MOSFET
- **Over-Voltage Protection**
- **Simple SOP-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

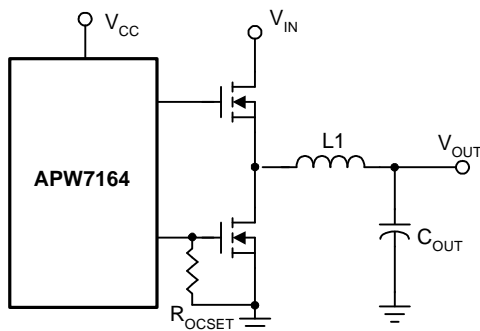
Applications

- **SMPS**

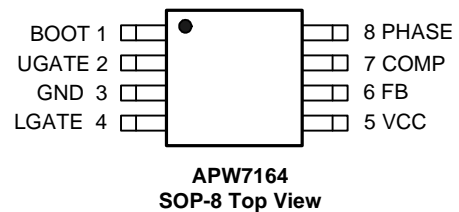
General Description

The APW7164 is a voltage mode, fixed 200kHz-switching frequency, synchronous buck converter. The APW7164 allows wide input voltage that is either a single 12V or two supply voltage(s) for various applications. A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. A built-in digital soft-start circuit prevents the output voltages from overshoot as well as limits the input current. An internal 0.8V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The APW7164 provides excellent output voltage regulations against load current variation. The controller's over-current protection monitors the output current by using the voltage drop across the $R_{DS(ON)}$ of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. The APW7164 also integrate over-voltage protection (OVP) and under-voltage protection (UVP) circuits which monitor the FB voltage to prevent the PWM output from over voltage and under voltage. The APW7164 is available in a simple SOP-8 package.

Simplified Application Circuit

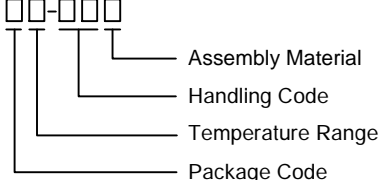
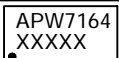


Pin Configuration



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7164		Package Code K : SOP-8 Operating Ambient Temperature Range E : -20 to 70 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7164 K:		XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit	
V_{VCC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 16	V	
V_{BOOT}	BOOT to PHASE Voltage	-0.3 ~ 16	V	
$V_{BOOT-GND}$	BOOT to GND Voltage	> 200ns	-0.3 ~ 32	V
		< 200ns	-5 ~ 40	V
V_{UGATE}	UGATE to PHASE Voltage	> 400ns	-0.3 ~ $V_{BOOT}+0.3$	V
		< 400ns	-5 ~ $V_{BOOT}+5$	V
V_{LGATE}	LGATE to GND Voltage	> 400ns	-0.3 ~ $V_{VCC}+0.3$	V
		< 400ns	-5 ~ $V_{VCC}+5$	V
V_{PHASE}	PHASE to GND Voltage	> 200ns	-0.3 ~ 16	V
		< 200ns	-10 ~ 30	V
	FB and COMP to GND (< $V_{VCC} + 0.3V$)	-0.3 ~ 7	V	
T_J	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature	-65 ~ 150	°C	
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C	

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient ^(Note 2)	80	°C/W
	SOP-8		

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V _{VCC}	VCC Supply Voltage (VCC to GND)	9~ 13.2	V
V _{OUT}	Converter Output Voltage	0.8 ~ 90%V _{IN}	V
V _{IN}	Converter Input Voltage	2.9 ~ V _{VCC}	V
I _{OUT}	Converter Output Current	0 ~ 20	A
T _A	Ambient Temperature	-20 ~ 70	°C
T _J	Junction Temperature	-20 ~ 125	°C

Note 3 : Refer to the application circuit for further information

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -20°C to 70°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7164			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY VOLTAGE AND CURRENT						
I _{VCC}	VCC Supply Current (Shutdown Mode)	UGATE and LGATE open; COMP=GND	-	3.5	6	mA
	VCC Supply Current	UGATE and LGATE open	-	4	6	
POWER-ON-RESET (POR)						
	Rising / Falling VCC POR Threshold		4.5	5	5.5	V
OSCILLATOR						
F _{OSC}	Oscillator Frequency		180	200	220	kHz
V _{OSC}	Oscillator Sawtooth Amplitude ^(Note 4)	(1.2V~2.7V typical)	-	1.5	-	V
D _{MAX}	Maximum Duty Cycle		85	-	90	%
PWM ERROR AMPLIFIER						
V _{REF}	Reference Voltage	T _A = -20 ~ 70°C	0.792	0.8	0.808	V
	Converter Load Regulation ^(Note 4)	I _{OUT} = 0mA ~ 10A	-	-	0.2	%
gm	Transconductance		-	667	-	µA/V
	FB Input Leakage Current	V _{FB} = 0.8V	-	0.1	1	µA
	COMP High Voltage	R _L = 10kΩ, to GND	-	2.5	-	V
	COMP Low Voltage	R _L = 10kΩ, to GND	-	1	-	
	Maximum COMP Source Current	V _{COMP} =2V	-	200	-	µA
	Maximum COMP Sink Current	V _{COMP} =2V	-	200	-	
GATE DRIVERS						
I _{UGATE}	High-side Gate Driver Source Current	V _{BOOT} = 12V, V _{UGATE-PHASE} = 2V	-	1.8	-	A
R _{UGATE}	High-side Gate Driver Sink Impedance	V _{BOOT} = 12V, I _{UGATE} = 0.1A	-	2.3	-	Ω
I _{LGATE}	Low-side Gate Driver Source Current	V _{VCC} = 12V, V _{LGATE} = 2V	-	1.8	-	A
R _{LGATE}	Low-side Gate Driver Sink Impedance	V _{VCC} = 12V, I _{UGATE} = 0.1A	-	1.3	-	Ω
T _D	Dead-time ^(Note 4)		-	30	-	ns

Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over $V_{VCC} = 12V$, $T_A = -20^{\circ}C$ to $70^{\circ}C$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.

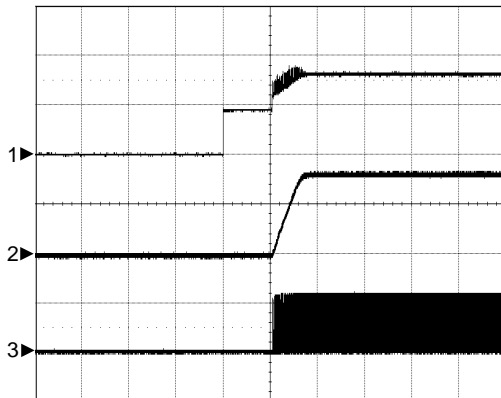
Symbol	Parameter	Test Conditions	APW7164			Unit
			Min.	Typ.	Max.	
PROTECTIONS						
V_{FB_UV}	FB Under-Voltage Protection Trip Point	V_{FB} Falling	45	50	55	%
V_{FB_OV}	FB Over-Voltage Protection Trip Point	V_{FB} Rising	120	125	130	%
	FB Over-Voltage Protection Hysteresis		-	5	-	%
V_{OCP_MAX}	Built-in Maximum OCP Voltage		300	-	-	mV
I_{OCSET}	OCSET Current Source		19.5	21.5	23.5	μA
SOFT-START						
$V_{DISABLE}$	Shutdown Threshold of V_{COMP}		-	-	0.6	V
T_{Delay}	Soft-Start Delay Time		9	10	11	ms
T_{SS}	Internal Soft-Start Interval ^(Note 4)		6	7	8	ms

Note 4: Guaranteed by design, not production tested.

Operating Waveforms

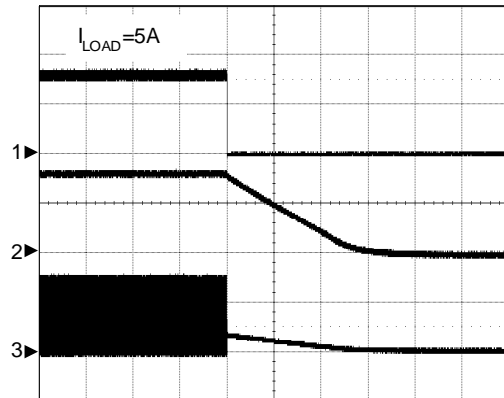
Refer to the typical application circuit. The test condition is $V_{IN}=12V$, $T_A=25^\circ C$ unless otherwise specified.

Enable



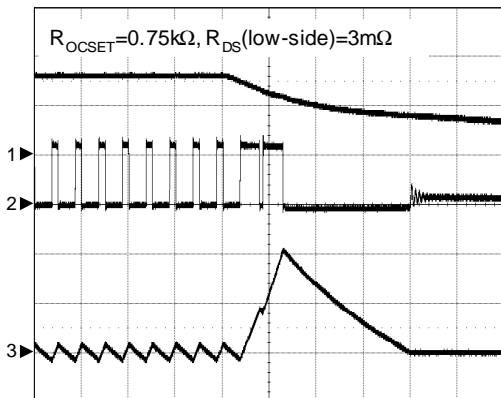
CH1: V_{COMP} , 1V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 CH3: V_{PHASE} , 10V/Div, DC
 TIME: 10ms/Div

Shutdown



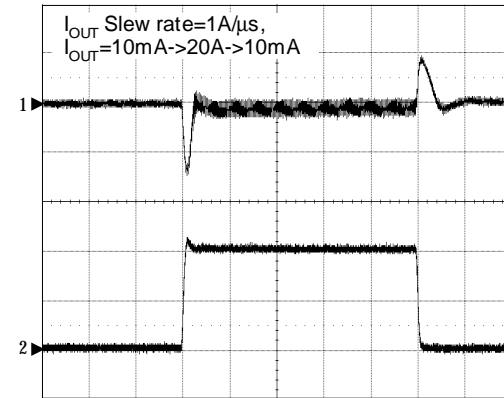
CH1: V_{COMP} , 1V/Div, DC
 CH2: V_{OUT} , 2V/Div, DC
 CH3: V_{PHASE} , 10V/Div, DC
 TIME: 1ms/Div

Short Circuit



CH1: V_{OUT} , 2V/Div, DC
 CH2: V_{PHASE} , 10V/Div, DC
 CH3: I_L , 5A/Div, DC
 TIME: 10 μ s/Div

Load Transient

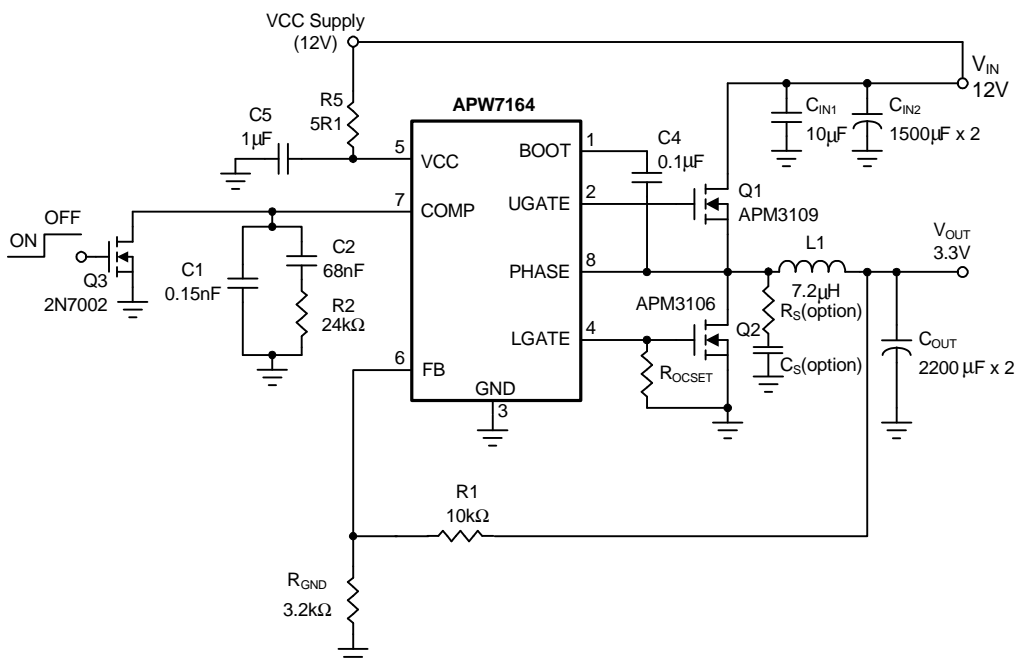


CH1: V_{OUT} , 100mV/Div, AC
 CH2: I_{OUT} , 10A/Div, DC
 TIME: 200 μ s/Div

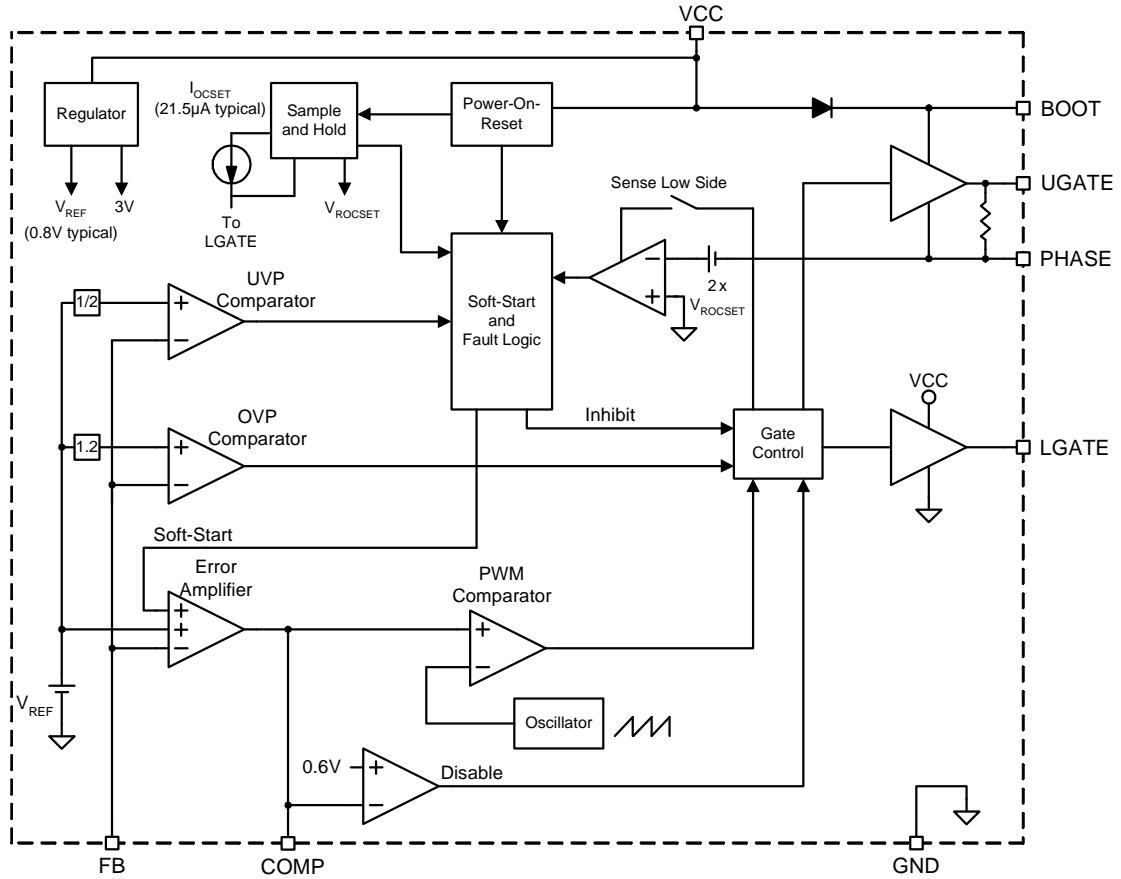
Pin Description

PIN		FUNCTION
NO.	NAME	
1	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, and the power supply voltage VCC, generates the bootstrap voltage for the high-side gate driver (UGATE).
2	UGATE	High-side Gate Driver Output. This pin is the gate driver for high-side MOSFET.
3	GND	Signal and Power ground. Connecting this pin to the system ground.
4	LGATE	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It is also used to set the maximum inductor current. Refer to the section in "Function Description" for detail.
5	VCC	Power Supply Input. Connect a nominal 5V to 12V power supply voltage to this pin. A power-on reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10µF) be connected to the GND for noise decoupling.
6	FB	Feedback Input of Converter. The converter senses feedback voltage via FB and regulates the FB voltage at 0.8V. Connecting FB with a resistor-divider from the output sets the output voltage of the converter.
7	COMP	This is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin. Pulling COMP low ($V_{DISABLE} = 0.6V$ typical) will shut down the controller. When the pull-down device is released, the COMP pin will start to rise. When the COMP pin rises above the $V_{DISABLE}$ trip point, the APW7164 will begin a new initialization and soft-start cycle.
8	PHASE	This pin is the return path for the high-side gate driver. Connecting this pin to the high-side MOSFET source and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the low-side MOSFET for over-current protection.

Typical Application Circuit



Block Diagram



Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7164 continually monitors the input supply voltage (VCC) and ensures that the IC has sufficient supply voltage and can work well. The POR function initiates a soft-start process while the VCC voltage just exceeds the POR threshold; the POR function also inhibits the operations of the IC while the VCC voltage falls below the POR threshold.

Soft-Start

The APW7164 builds in a 50-step digital soft-start to control the output voltage rise as well as limit the current surge at the start-up. During soft-start, an internal ramp voltage connected to the one of the positive inputs of the error amplifier replaces the reference voltage (0.8V typical) until the ramp voltage reaches the reference voltage. The digital soft-start circuit interval (shown as figure 1) depends on the switching frequency.

$$T_{\text{Delay}} = t_2 - t_1 = 10\text{ms}(\text{typ.})$$

$$T_{\text{SS}} = (t_3 - t_2) = \frac{1}{F_{\text{OSC}}} \cdot 1400$$

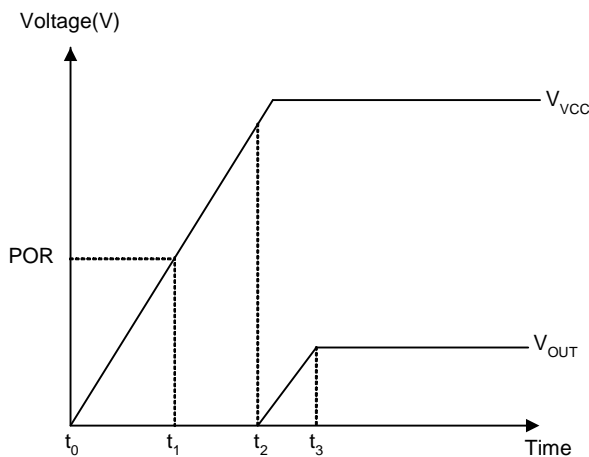


Figure 1. Soft-Start Interval

Over-Current Protection of the PWM Converter

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET

during its on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor (R_{OCSET}), connected from the LGATE to GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (21.5 μA typical), flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET} . The device holds V_{ROCSET} and stops the current source, I_{OCSET} , during normal operation. When the voltage across the low-side MOSFET exceeds the double V_{ROCSET} ($2 \times V_{\text{ROCSET}}$), the IC shuts off the converter and then device was shut down. The output of the PWM converter is latched to be floating. The APW7164 has an internal OCP voltage, $V_{\text{OCP_MAX}}$, and the value is 0.3V typical. When the $R_{\text{OCSET}} \times I_{\text{OCSET}}$ exceeds 0.3V or the R_{OCSET} is floating or not connected, the V_{ROCSET} will be the default value 0.3V. The over current threshold would be 0.3V across low-side MOSFET. The threshold of the valley inductor current is therefore given by:

$$I_{\text{LIMIT}} = \frac{2 \times I_{\text{OCSET}} \times R_{\text{OCSET}}}{R_{\text{DS(ON)}}(\text{low-side})}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

- The $R_{\text{DS(ON)}}$ of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum $R_{\text{DS(ON)}}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (19.5 μA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the low-side MOSFET; I_{LIMIT} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{\text{LIMIT}} > I_{\text{OUT(MAX)}} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ripple current

- The overshoot and transient peak current also should be considered.

Function Description (Cont.)

Under-Voltage Protection

The under-voltage function monitors the voltage on FB (V_{FB}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold ($50\% V_{REF}$), a fault signal is internally generated and the device turns off high-side and low-side MOSFETs. The converter is shutdown and the output is latched to be floating.

PHASE voltage is also monitored until it is below 1V threshold, at which time the LGATE is released to rise after a constant delay.

Over-Voltage Protection (OVP) of the PWM Converter

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 125% of the nominal output voltage, the APW7164 turns off the high-side MOSFET and low-side MOSFET until the output voltage falls below the falling OVP threshold, regulating the output voltage around the OVP threshold.

Shutdown and Enable

The APW7164 can be shut down or enabled by pulling low the voltage on COMP. The COMP is a dual-function pin. During normal operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin.

Pulling the COMP low ($V_{DISABLE} = 0.6V$ typical) places the controller into shutdown mode which UGATE and LGATE are pulled to PHASE and GND respectively.

When the pull-down device is released, the COMP voltage will start to rise. When the COMP voltage rises above the $V_{DISABLE}$ threshold, the APW7164 will begin a new initialization and soft-start process.

Adaptive Shoot-Through Protection of the PWM Converter

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the LGATE voltage is monitored until it is below 1V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE-to-

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_{GND}} \right)$$

Where R1 is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to the GND.

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately I_{OUT}/2 where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1μF to 1μF can connect between VCC and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

A tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP pin and ground should be added. The simplest loop compensation network is shown in Figure 5.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

Application Information (Cont.)

Compensation (Cont.)

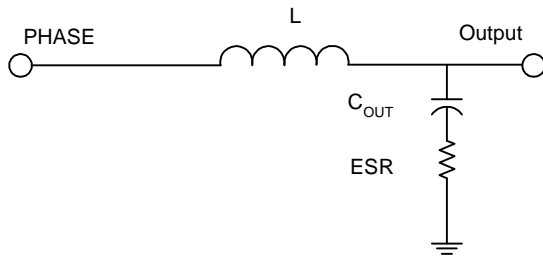


Figure 2. The Output LC Filter

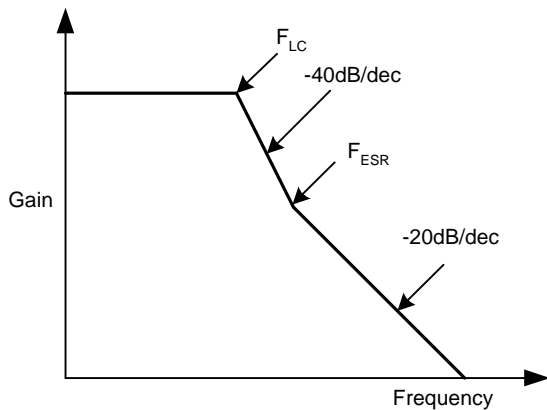


Figure 3. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

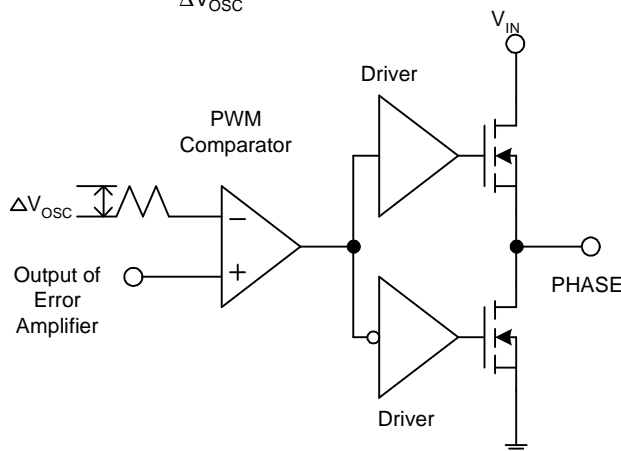


Figure 4. The PWM Modulator

The compensation circuit is shown in Figure 5. R3 and C1 introduce a zero and C2 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Z_o = gm \times \left[\left(R3 + \frac{1}{sC1} \right) // \frac{1}{sC2} \right]$$

$$= gm \times \frac{\left(s + \frac{1}{R3 \times C1} \right)}{s \times \left(s + \frac{C1 + C2}{R3 \times C1 \times C2} \right) \times C2}$$

The pole and zero of the compensation network are:

$$F_p = \frac{1}{2 \times \pi \times R3 \times \frac{C1 \times C2}{C1 + C2}}$$

$$F_z = \frac{1}{2 \times \pi \times R3 \times C1}$$

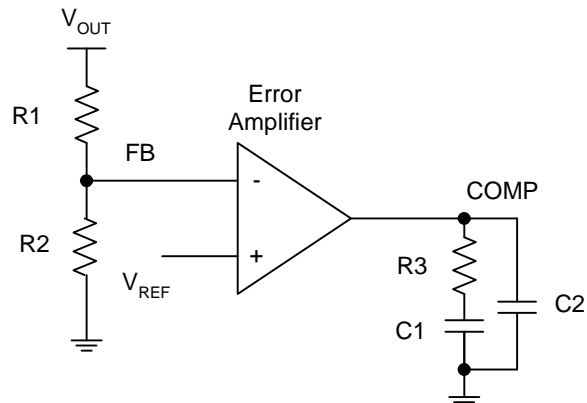


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R2}{R1 + R2} \times GAIN_{AMP}$$

Figure 6 shows the converter gain and the following guidelines will help to design the compensation network.

1. Select the desired zero crossover frequency F_o :

$$(1/5 \sim 1/10) \times F_{sw} > F_o > F_z$$

Use the following equation to calculate R3:

$$R3 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R1 + R2}{R2} \times \frac{F_o}{gm}$$

Where:

$$gm = 667 \mu A/V$$

Application Information (Cont.)

Compensation (Cont.)

2. Place the zero F_z before the LC filter double poles F_{LC} :

$$F_z = 0.75 \times F_{LC}$$

Calculate the C1 by the equation:

$$C1 = \frac{1}{2 \times \pi \times R1 \times 0.75 \times F_{LC}}$$

3. Set the pole at the half the switching frequency:

$$F_p = 0.5 \times F_{SW}$$

Calculate the C2 by the equation:

$$C2 = \frac{C1}{\pi \times R3 \times C1 \times F_{SW} - 1}$$

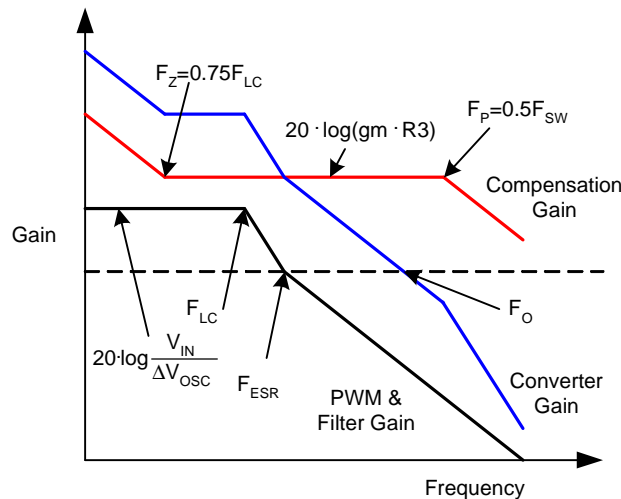


Figure 6. Converter Gain & Frequency

MOSFET Selection

The selection of the N-channel power MOSFETs is determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}), and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{out}^2 (1 + TC) (R_{DS(ON)}) D + (0.5) (I_{out}) (V_{IN}) (t_{SW}) F_{SW}$$

$$P_{LOWER} = I_{out}^2 (1 + TC) (R_{DS(ON)}) (1 - D)$$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching interval, t_{sw} , is the function of the reverse transfer capacitance C_{RSS} . Figure 7 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the " $R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

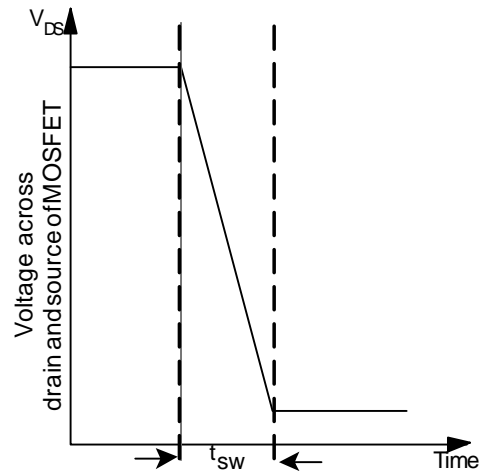


Figure 7. Switching waveform across MOSFET

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 200kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating till combined using the ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short

Application Information (Cont.)

Layout Consideration (Cont.)

and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG and LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.

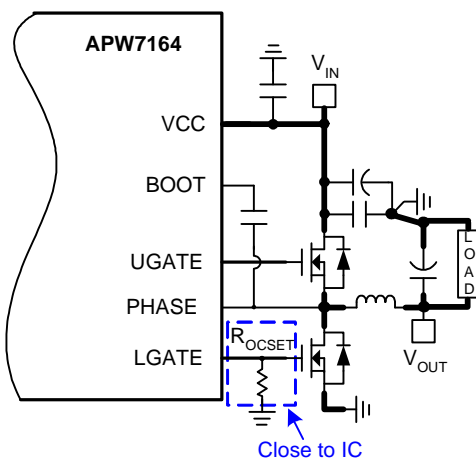
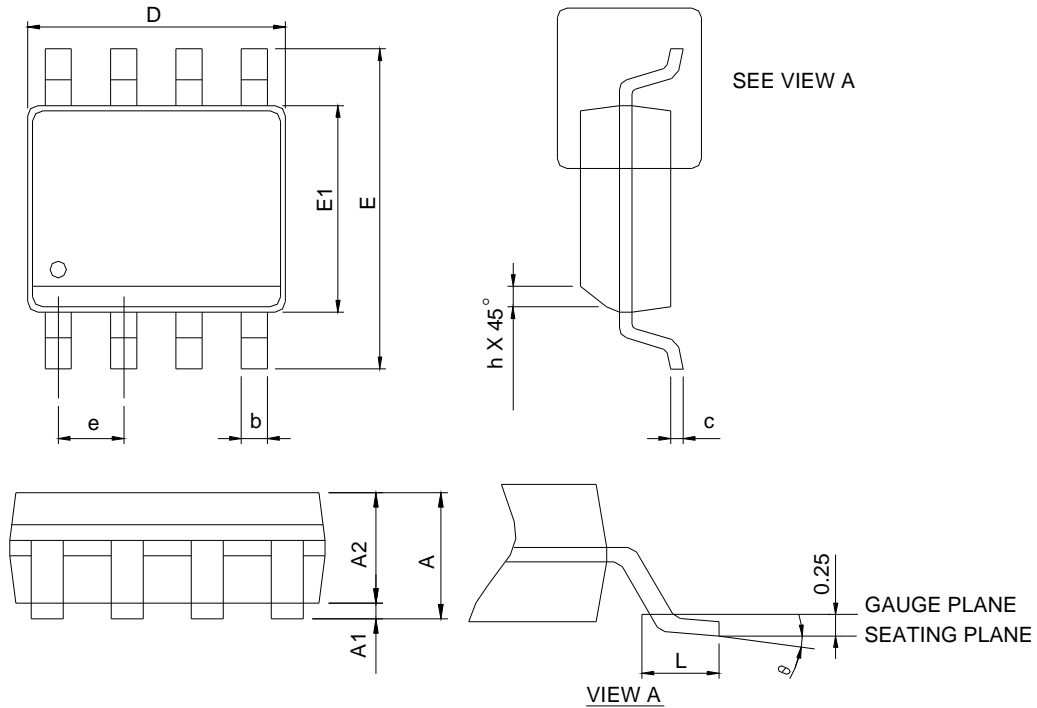


Figure 8. Layout Guidelines

Package Information

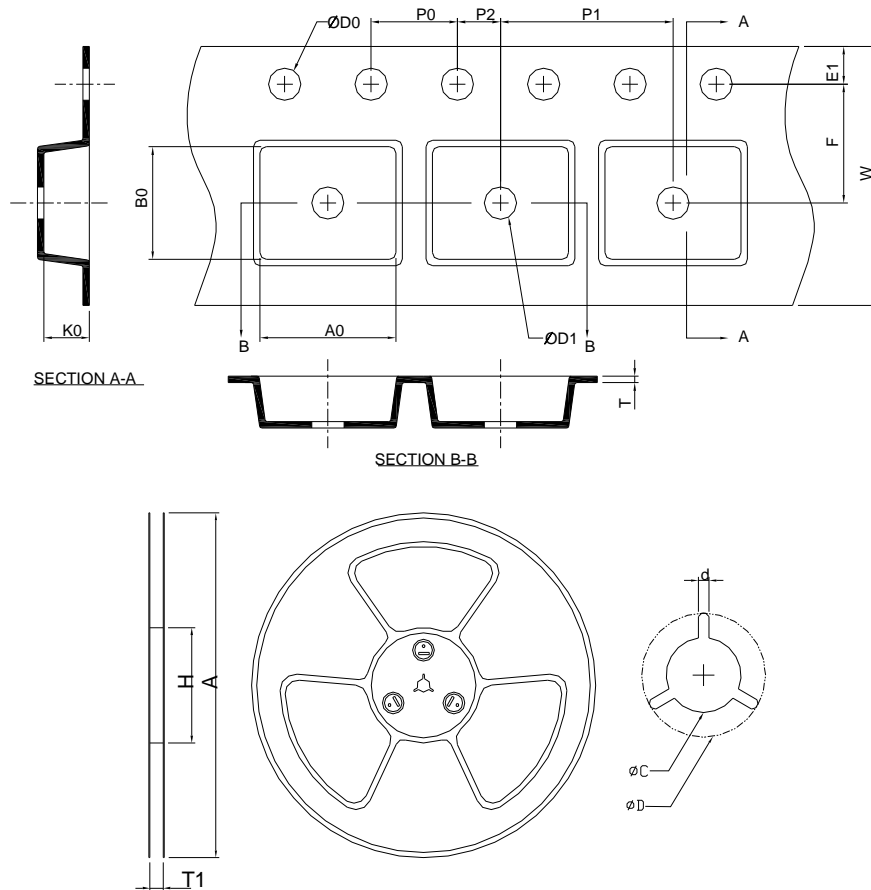
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

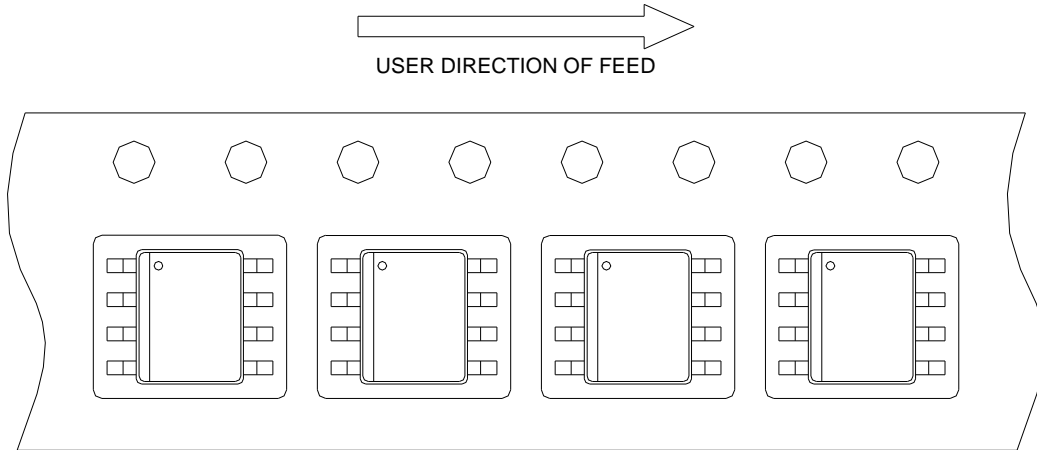
(mm)

Devices Per Unit

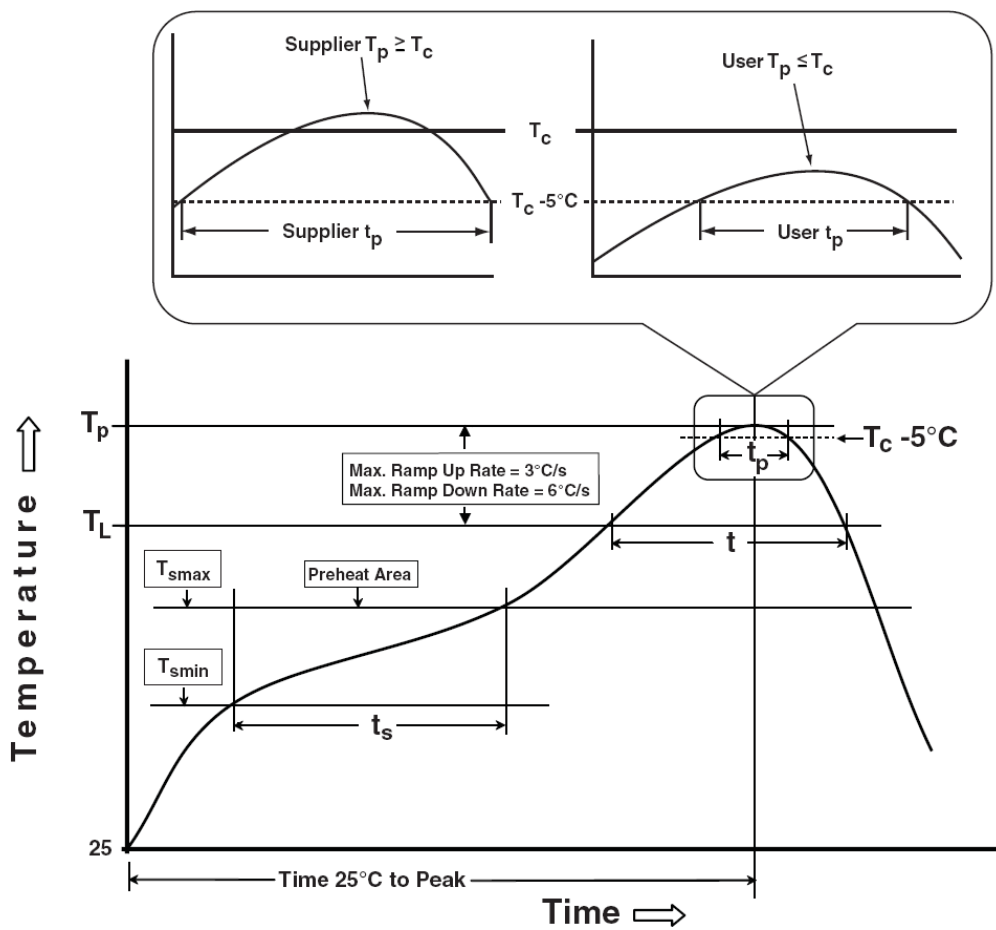
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100mA$

Customer Service

Anpec Electronics Corp.

Head Office :

No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838