# APW7178A

**ANPEC**

1.5MHz, 1A Synchronous Buck Regulator

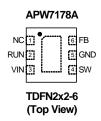## Features

- **1A Output Current**
- **Wide 2.7V~6.0V Input Voltage**
- **Fixed 1.5MHz Switching Frequency**
- **Low Dropout Operating at 100% Duty Cycle**
- **Synchronous Rectifier**
- **0.6V Reference Voltage**
- **<0.5mA Input Current During Shutdown**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Available in TDFN2x2-6 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## Applications

- **HD STB**
- **BT Mouse**
- **PND Instrument**
- **Portable Instrument**

## Pin Configuration

**APW7178A**

```
NC  [1]      [6] FB
RUN [2]      [5] GND
VIN [3]      [4] SW
```
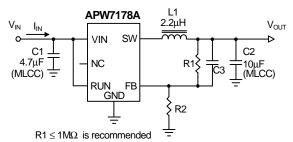
**TDFN2x2-6
(Top View)**

## General Description

APW7178A is a 1.5MHz high efficiency monolithic synchronous buck regulator. Design with current mode scheme, the APW7178A is stable with ceramic output capacitor. Input voltage from 2.7V to 6.0V makes the APW7178A ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable electrical devices. The internally fixed 1.5MHz operating frequency allows the using of small surface mount inductors and capacitors. The synchronous switches included inside increase the efficiency and eliminate the need of an external Schottky diode.

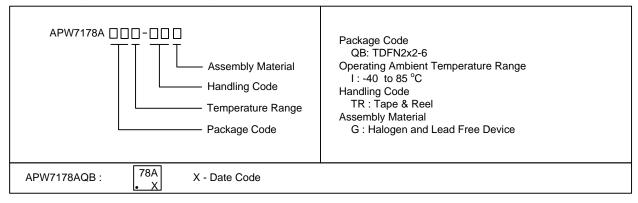The APW7178A is available in TDFN2x2-6 packages.

## Simplified Application Circuit



$R1 \leq 1M\Omega$ is recommended
$R2 \leq 200K\Omega$ is recommended
Place C1 closed VIN/GND. Without via hole is recommended.

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## Ordering and Marking Information

APW7178A ☐☐☐ – ☐☐☐

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
  QB: TDFN2x2-6
Operating Ambient Temperature Range
  I : -40 to 85 $^o$C
Handling Code
  TR : Tape & Reel
Assembly Material
  G : Halogen and Lead Free Device

| APW7178AQB : | 78A<br>▪ X | X - Date Code |
|---|---|---|

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Bias Supply Voltage (VIN to GND) | -0.3 ~ 7 | V |
| | RUN, FB, SW to GND Voltage | -0.3 ~ $V_{IN}$+0.3 | V |
| $P_D$ | Power Dissipation | Internally Limited | W |
| | Maximum Junction Temperature | 150 | $^o$C |
| $T_{STG}$ | Storage Temperature | -65 ~ 150 | $^o$C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature, 10 Seconds | 260 | $^o$C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

| Symbol | Parameter | | Typical Value | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance in Free Air [Note 2] | TDFN2x2-6 | 165 | $^o$C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Bias Supply Voltage (VIN to GND) | 2.7 ~ 6 | V |
| $V_{OUT}$ | Converter Output Voltage | 0.6 ~ $V_{IN}$ | V |
| $I_{OUT}$ | Converter Output Current | 0 ~ 1 | A |
| L1 | Converter Output Inductor | 1.0 ~ 10 | µH |

## Recommended Operating Conditions (Note 3) **(Cont.)**

| Symbol | Parameter | Range | Unit |
|--------|-----------|-------|------|
| $C_{IN}$ | Converter Input Capacitor | 4.7 ~100 | μF |
| $C_{OUT}$ | Converter Output Capacitor | 4.7 ~100 | μF |
| $T_A$ | Ambient Temperature | -40 ~ 85 | °C |
| $T_J$ | Junction Temperature | -40 ~ 125 | °C |

Note 3: Refer to the typical application circuit

## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=3.6V and $T_A$= 25 °C.

| Symbol | Parameter | Test Conditions | APW7178A Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | |
| $V_{IN}$ | Input Voltage Range | | 2.7 | - | 6 | V |
| $I_{SD}$ | Shutdown Input Current | RUN = GND | - | - | 0.5 | μA |
| **POWER-ON-RESET (POR) and LOCKOUT VOLTAGE THRESHOLDS** | | | | | | |
| | UVLO Threshold | | 2.1 | 2.35 | 2.6 | V |
| | UVLO Hysteresis | | - | 0.1 | - | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference Voltage | $V_{IN}$=2.7V~6V, $T_A$ = -40~85 °C | 0.588 | 0.6 | 0.612 | V |
| | Output Voltage Accuracy | 0A < $I_{OUT}$ < 1A | -2.5 | - | +2.5 | % |
| $I_{FB}$ | FB Input Current | | -50 | - | 50 | nA |
| **INTERNAL POWER MOSFETS** | | | | | | |
| $F_{SW}$ | Switching Frequency | | 1.2 | 1.5 | 1.8 | MHz |
| | Foldback Frequency | $V_{FB}$ = 0.1V | - | 210 | - | kHz |
| | Foldback Threshold Voltage on FB | $V_{FB}$ Falling | - | 0.2 | - | V |
| | Foldback Hysteresis | | - | 50 | - | mV |
| $R_{P-FET}$ | High Side N-FET Switch ON Resistance | $I_{SW}$=200mA | - | 0.28 | - | Ω |
| $R_{N-FET}$ | Low Side P-FET Switch ON Resistance | $I_{SW}$=200mA | - | 0.25 | - | Ω |
| | Minimum On-Time | | - | - | 100 | ns |
| | Maximum Duty Cycle | | - | - | 100 | % |
| **PROTECTION** | | | | | | |
| $I_{LIM}$ | Maximum Inductor Current-Limit | $I_{P-FET}$, 2.7V  $V_{IN}$  6V | 1.4 | 1.6 | - | A |
| $T_{OTP}$ | Over-Temperature Protection | $T_J$ Rising | - | 150 | - | °C |
| | Over-Temperature Protection Hysteresis | $T_J$ Falling | - | 30 | - | °C |

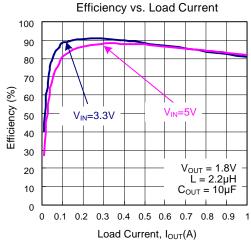## Electrical Characteristics (Cont.)

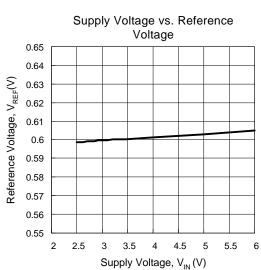Unless otherwise specified, these specifications apply over $V_{IN}$=3.6V and $T_A$= 25 °C.

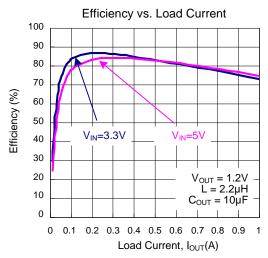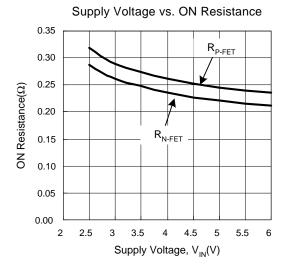| Symbol | Parameter | Test Conditions | APW7178A | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| **START-UP AND SHUTDOWN** | | | | | | |
| $T_{SS}$ | Soft-Start Duration | (Note 4) | - | 0.7 | - | ms |
| | RUN Input High Threshold | $V_{IN}$ = 2.7V~6V | - | - | 1 | V |
| | RUN Input Low Threshold | $V_{IN}$ = 2.7V~6V | 0.4 | - | - | V |
| | RUN Leakage Current | $V_{RUN}$ = 5V, $V_{IN}$ = 5V | -1 | - | 1 | μA |

# Typical Operating Characteristics

(Refer to the application circuit in the section "Typical Application Circuits", $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $T_A$=25ºC unless otherwise specified )

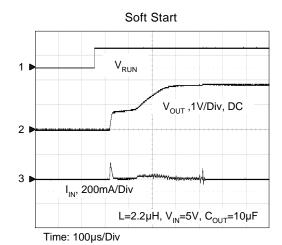**Efficiency vs. Load Current**



**Efficiency vs. Load Current**



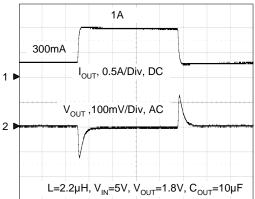**Supply Voltage vs. Reference Voltage**



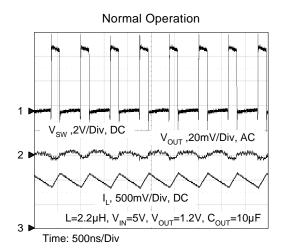**Supply Voltage vs. ON Resistance**

## Operating Waveforms

(Refer to the application circuit in the section "Typical Application Circuits", $V_{IN}$=3.6V, $V_{OUT}$=1.8V, $T_A$=25°C unless otherwise specified)

**Soft Start**



1 ▶  $V_{RUN}$

2 ▶  $V_{OUT}$ ,1V/Div, DC

3 ▶  $I_{IN}$, 200mA/Div

L=2.2µH, $V_{IN}$=5V, $C_{OUT}$=10µF

Time: 100µs/Div

**Load Transient Response**



1A

300mA

1 ▶  $I_{OUT}$, 0.5A/Div, DC

2 ▶  $V_{OUT}$ ,100mV/Div, AC

L=2.2µH, $V_{IN}$=5V, $V_{OUT}$=1.8V, $C_{OUT}$=10µF

Time: 100µs/Div

**Normal Operation**



1 ▶  $V_{SW}$ ,2V/Div, DC

2 ▶  $V_{OUT}$ ,20mV/Div, AC

$I_L$, 500mV/Div, DC

L=2.2µH, $V_{IN}$=5V, $V_{OUT}$=1.2V, $C_{OUT}$=10µF

3 ▶  Time: 500ns/Div

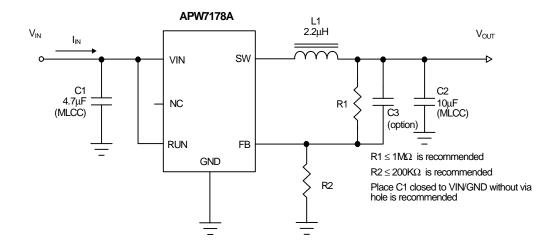## Pin Description

| PIN | | FUNCTION |
| --- | --- | --- |
| **NO.** | **NAME** | |
| 1 | NC | No Internal Connection. |
| 2 | RUN | Enable Control Input. Forcing this pin above 1.0V enables the device. Forcing this pin below 0.4V shuts it down. In shutdown, all functions are disabled to decrease the supply current below 0.5μA. **Do not leave RUN pin floating.** |
| 3 | VIN | Device and Converter Supply Pin. Must be closely decoupled to GND with a 4.7μF or greater ceramic capacitor. |
| 4 | SW | Switch Node Connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFETs switches. |
| 5 | GND | Power and Signal Ground. |
| 6 | FB | The feedback voltage is decided by an external resistive divider across the output. |

## Block Diagram

## Typical Application Circuit



R1 ≤ 1MΩ is recommended

R2 ≤ 200KΩ is recommended

Place C1 closed to VIN/GND without via hole is recommended

## Function Description

**Main Control Loop**

The APW7178A is a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal P-channel power MOSFET is turned on each cycle. The peak inductor current at which ICMP turn off the P-FET is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external resistive divider connected between $V_{OUT}$ and ground allows the EAMP to receive an output feedback voltage $V_{FB}$ at FB pin. When the load current increases, it causes a slightly decrease in $V_{FB}$ relative to the 0.6V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

**Enable/Shutdown**

Driving RUN to the ground places the APW7178A in shutdown mode. When in shutdown, the internal power MOSFETs turn off, all internal circuitry shuts down and the quiescent supply current reduces to 0.5μA maximum.

**Slope Compensation and Inductor Peak Current**

The APW7178A is a peak current mode PWM step down converter. To prevent sub-harmonic oscillations, the APW7178A sense the peak current and add slope compensation to stable the converter. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the APW7178A uses a special scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

**Over-Temperature Protection (OTP)**

The over-temperature circuit limits the junction temperature of the APW7178A. When the junction temperature exceeds 150°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature ($T_J$) during continuous thermal overload conditions, increasing the lifetime of the device.

**Dropout Operation**

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on time. Further, reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The input voltage minus the voltage drop will determine the output voltage across the P-FET and the inductor.

An important detail to remember is that on resistance of P-FET switch will increase at low input supply voltage. Therefore, the user should calculate the power dissipation when the APW7178A is used at 100% duty cycle with low input voltage.

## Application Information

### Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

### Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, $\Delta I_L$, is 40% of maximum output current. The recommended inductor value can be calculated as below:

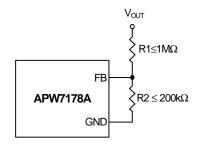$$L \geq \frac{V_{OUT}\left(1 - \dfrac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \cdot \Delta I_L}$$

$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

### Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as

shown in "Typical Application Circuits". A suggestion of maximum value of R2 is 200kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 0.6 \cdot \left(1 + \frac{R1}{R2}\right)$$
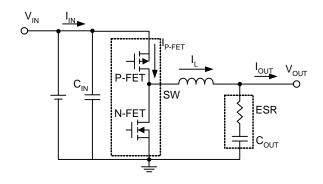


### Output Capacitor Selection

The current-mode control scheme of the APW7178A allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot \left(1 - \dfrac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)$$
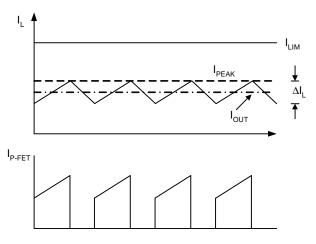
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

## Application Information (Cont.)

**Output Capacitor Selection (Cont.)**



**Thermal Consideration**

In most applications, the APW7178A does not dissipate much heat due to its high efficiency. But, in applications where the APW7178A is running at high ambient temperature with low supply voltage and high duty cycles, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the APW7178A from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The power dissipated by the part is approximated:

$$P_D \cong I_{OUT}^2 \times (R_{P\text{-FET}} \times D + R_{N\text{-FET}} \times (1-D))$$

The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

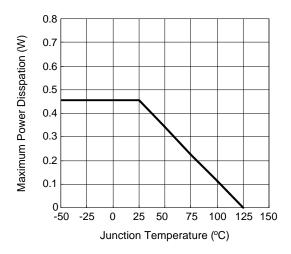Where $P_D$ is the power dissipated by the regulator, D is duty cycle of main switch

$$D = V_{OUT}/V_{IN}$$

The $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, $T_J$, is given by:

$$T_J = T_A + T_R$$

Where $T_A$ is the ambient temperature.

The maximum power dissipation on the device can be shown as the following figure:
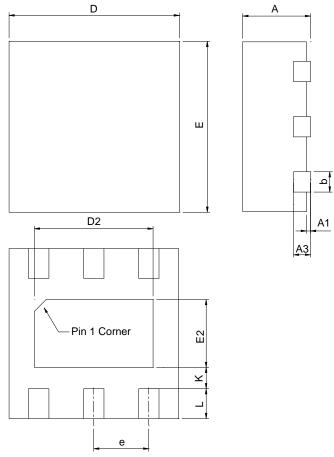


**Layout Consideration**

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor and VIN/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/GND to capacitor less than 2mm respectively is recommended.

2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.

3. The output capacitor should be place closed to VOUT and GND.

4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.
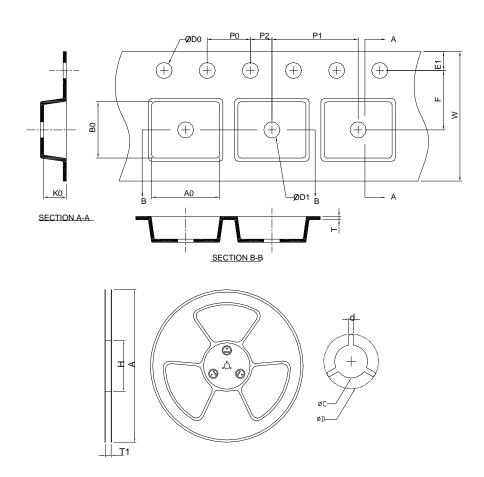
## Package Information

**TDFN2x2-6**



| S Y M B O L | TDFN2x2-6 | | | |
|---|---|---|---|---|
| | **MILLIMETERS** | | **INCHES** | |
| | **MIN.** | **MAX.** | **MIN.** | **MAX.** |
| A | 0.70 | 0.80 | 0.028 | 0.031 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D | 1.90 | 2.10 | 0.075 | 0.083 |
| D2 | 1.00 | 1.60 | 0.039 | 0.063 |
| E | 1.90 | 2.10 | 0.075 | 0.083 |
| E2 | 0.60 | 1.00 | 0.024 | 0.039 |
| e | 0.65 BSC | | 0.026 BSC | |
| L | 0.30 | 0.45 | 0.012 | 0.018 |
| K | 0.20 | | 0.008 | |

Note : 1. Followed from JEDEC MO-229 WCCC.

## Carrier Tape & Reel Dimensions



| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| | 178.0±2.00 | 50 MIN. | 8.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 8.0±0.20 | 1.75±0.10 | 3.5±0.05 |
| **TDFN2x2-6** | P0 | P1 | P2 | D0 | D1 | T | A0 | B0 | K0 |
| | 4.0±0.10 | 4.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 2.35 MIN | 2.35 MIN | 1.30±0.20 |

(mm)

## Devices Per Unit

| Package Type | Unit | Quantity |
|---|---|---|
| **TDFN2x2-6** | Tape & Reel | 3000 |

## Taping Direction Information

**TDFN2x2-6**

USER DIRECTION OF FEED

## Classification Profile

## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak** Temperature min ($T_{smin}$) Temperature max ($T_{smax}$) Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 100 °C 150 °C 60-120 seconds | 150 °C 200 °C 60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$) Time at liquidous ($t_L$) | 183 °C 60-150 seconds | 217 °C 60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume mm$^3$ <350 | Volume mm$^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume mm$^3$ <350 | Volume mm$^3$ 350-2000 | Volume mm$^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ Tj=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM   2KV |
| MM | JESD-22, A115 | VMM   200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$   100mA |

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## Customer Service

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