APW7408B

1.3A, 5V Input, 1.4MHz Synchronous Buck Converter

Features

- **Typical 0.6V Internal Reference Voltage**
- **Force PWM Mode Operation**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VIN**
- **Integrated Soft Start and Output Discharge**
- **Over-Temperature Protection**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **High/ Low Side Current Limit**
- **Enable/Shutdown Function**
- **Small SOT-23-5 packages**
- **Lead Free and Green Devices Available (RoHS compliant)**

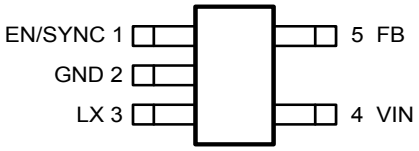
General Description

The APW7408B is a 1.3A synchronous buck converter that uses current-mode control scheme to convert wide input voltage of 2.9V to 5.5V to outputs as low as 0.6V while providing excellent output voltage regulation.
The APW7408B operates in Force PWM mode operation. The internal switching frequency is set at 1.4MHz while the EN/SYNC pin supports external clock synchronization, and is also equipped with Power-on-reset, internal soft start and complete protections (under-voltage, over-voltage, over-temperature and current-limit) into a single low cost SOT-23-5 package. The IC also provides output capacitor discharge when it is disabled via the internal low side MOSFET.

Applications

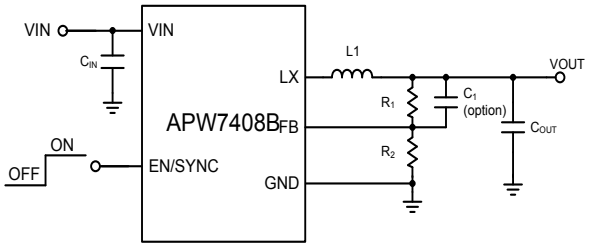
- **Notebook Computer & UMPC**
- **LCD Monitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Portable Instrument**

Pin Configuration (Top View)



SOT-23-5
Top View

Simplified Application Circuit



Ordering and Marking Information

APW7408B □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code B: SOT-23-5 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7408B : 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
VVIN	VIN to GND		-0.3 ~ 6.5	V
VLX	LX to GND Voltage	< 30ns pulse width	-3 ~ 8	V
		> 30ns pulse width	-1 ~VIN+0.3	V
VI/O	FB, EN/SYNC to GND Voltage		-0.3 ~ 6.5	V
TJ	Junction Temperature		150	°C
TSTG	Storage Temperature		-65 ~ 150	°C
TSDR	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2)	260	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Control and Driver Supply Voltage	2.9 ~ 5.5	V
I_{OUT}	Converter output current	0 ~ 1.3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

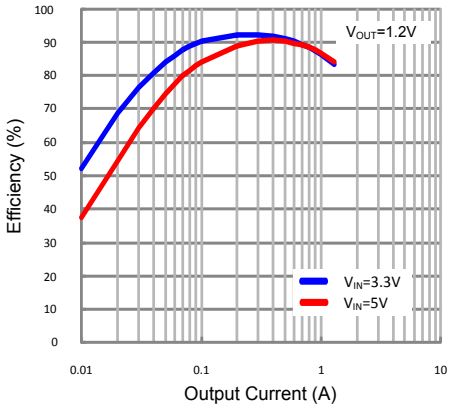
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=5V. T_A=25°C

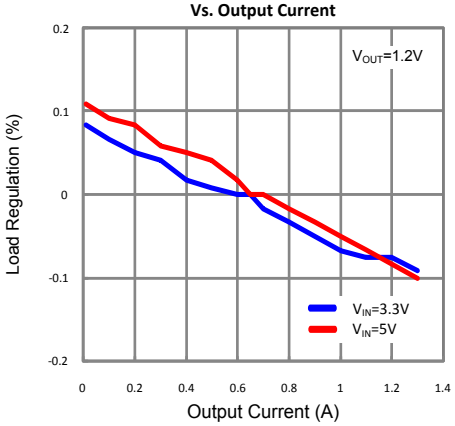
Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
Supply Current						
I_{VIN}	VIN Supply Current	V_{FB}=0.7V	-	65	-	μA
I_{SHDN}	VIN Shutdown Supply Current	EN=GND	-	-	1	μA
Power-On-Reset (POR)						
	VIN POR Voltage Threshold	VIN Rising	2.3	2.4	2.5	V
	VIN POR Hysteresis		-	0.2	-	V
EN/SYNC Threshold						
	EN Enable threshold	For Enable IC	1.5	-	-	V
	EN shutdown threshold	For Disable IC	-	-	0.4	V
	PWM/SYNC Input High Level	For SYNC Function	1.9	-	-	V
	PWM/SYNC Input Low Level	For SYNC Function	-	-	0.25	V
F_{SYNC}	SYNC Frequency Range		800	-	2000	kHz
Reference Voltage						
T_{SS}	Soft Start time		-	1	-	ms
V_{REF}	Reference Voltage		-	0.6	-	V
		T_A=25°C	-1	-	1	%
Oscillator						
F_{OSC}	Oscillator Frequency		1190	1400	1610	kHz
	Minimum Controllable on Time		-	70	-	ns
POWER MOSFET						
	High Side MOSFET Resistance	VIN=5V, I_{LX}=0.5A, T_A=25°C	-	115	-	mΩ
	Low Side MOSFET Resistance	VIN=5V, I_{LX}=0.5A, T_A=25°C	-	95	-	mΩ
	High Side MOSFET Leakage Current		-	-	10	μA
	Low Side MOSFET Leakage Current		-	-	10	μA
PROTECTIONS						
I_{LIM}	High Side MOSFET current-limit	Peak Current		1.95		A
	Over-temperature Trip Point	Guarantee by design	-	160	-	°C
	Over-temperature Hysteresis	Guarantee by design	-	50	-	°C
	Over Voltage Protection	VOUT Rising	-	125	-	%V_{REF}
	Under Voltage Protection		-	50	-	%V_{REF}
	Low Side Switch Current-Limit	From Drain to Source	-	-1	-	A

Typical Operating Characteristics

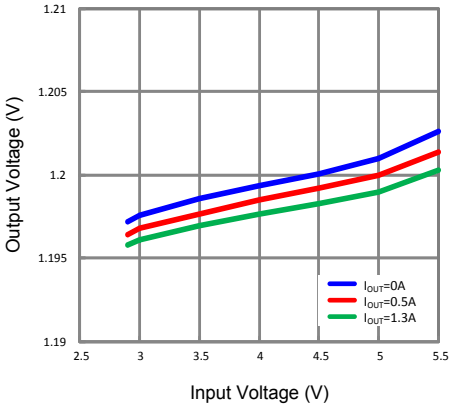
Efficiency vs. Output Current



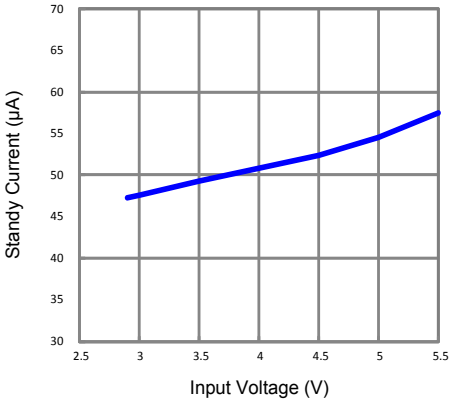
Output Voltage Regulation Vs. Output Current



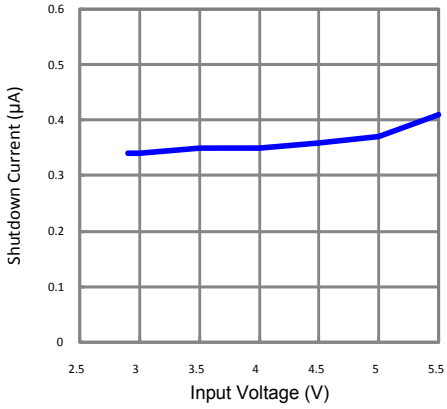
Output Voltage vs. Input Voltage



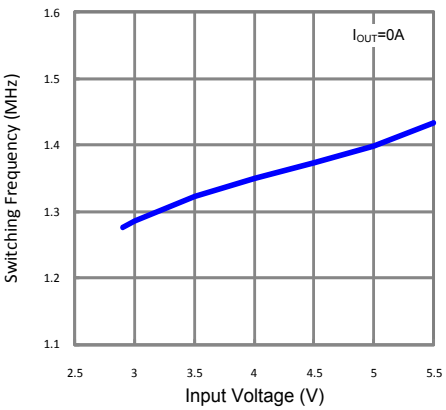
Standby Current vs. Input Voltage



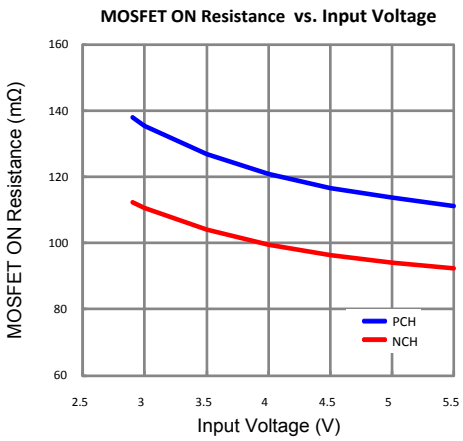
Shutdown Current vs. Input Voltage

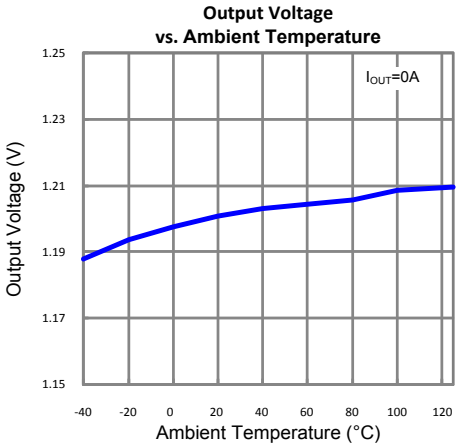


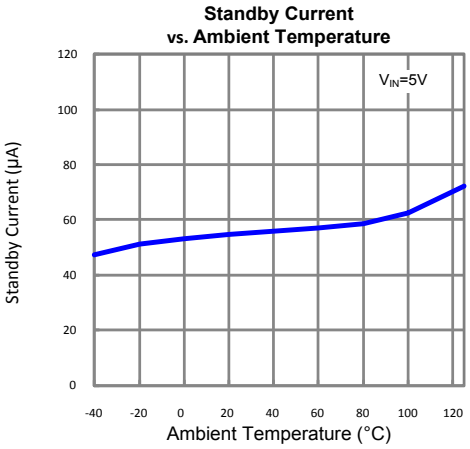
Switching Frequency vs. Input Voltage

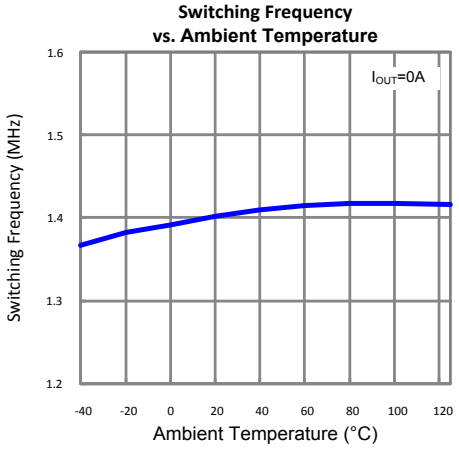


Typical Operating Characteristics (Cont.)





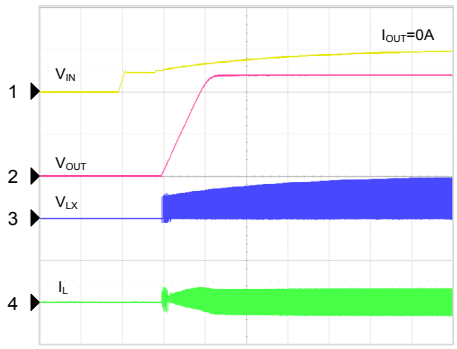




Operating Waveforms

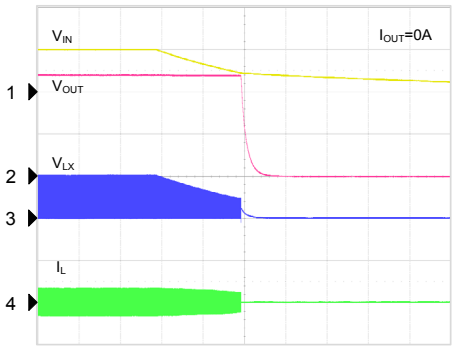
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Start-Up by VIN



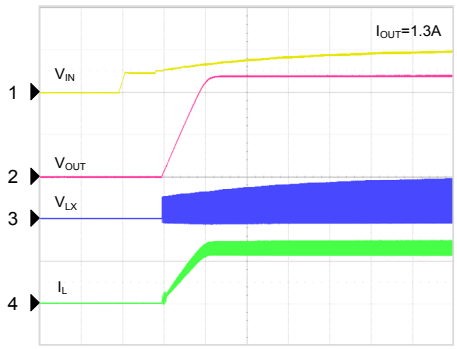
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 500mA/Div
Time: 1ms/Div

Shutdown by VIN



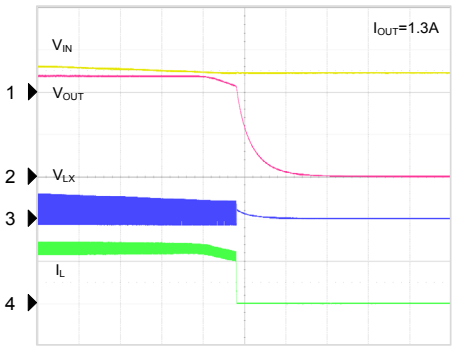
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 500mA/Div
Time: 100ms/Div

Start-Up by VIN



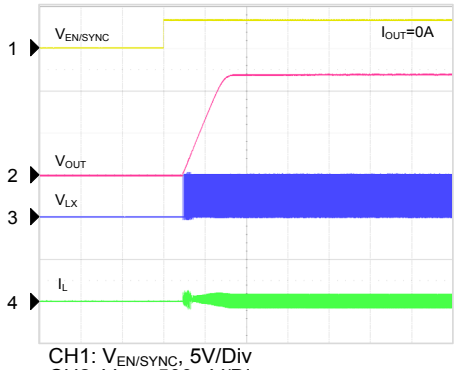
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 1ms/Div

Shutdown by VIN



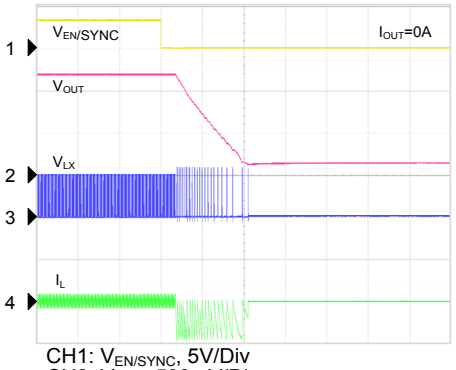
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 100µs/Div

Start-Up by Enable



CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 1ms/Div

Shutdown by Enable

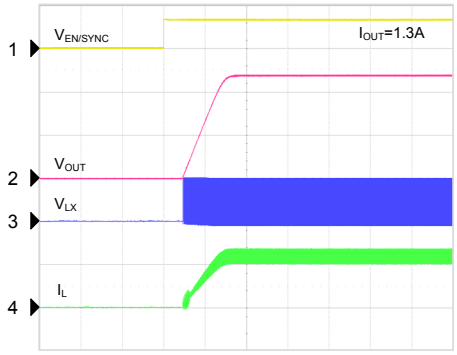


CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 50µs/Div

Operating Waveforms (Cont.)

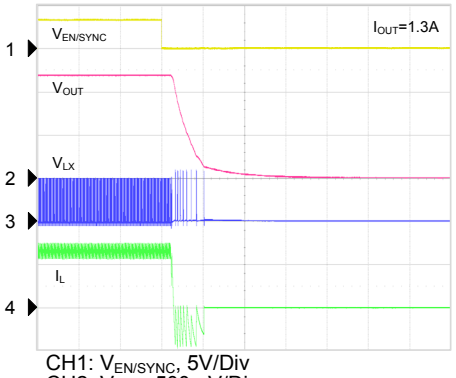
Refer to the typical application circuit. The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Start-Up by Enable



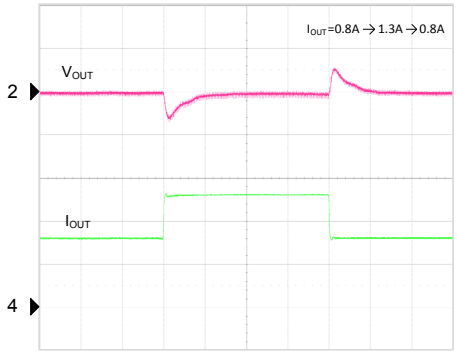
CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 1ms/Div

Shutdown by Enable



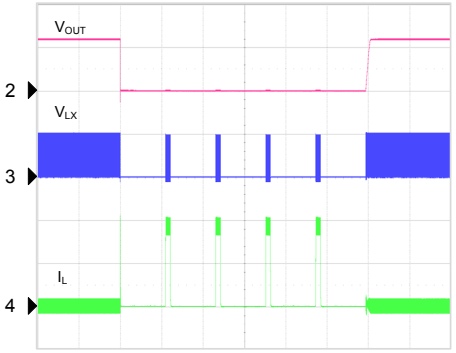
CH1: $V_{EN/SYNC}$, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 50µs/Div

Load Transient



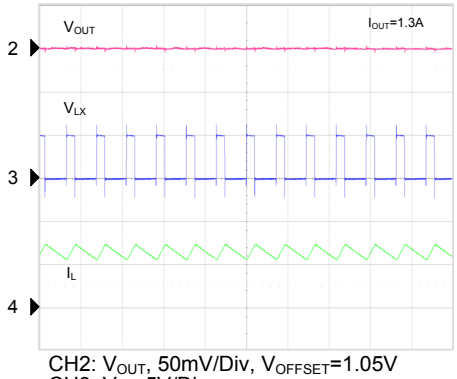
CH2: V_{OUT}, 50mV/Div, V_{OFFSET}=1.1V
CH4: I_{OUT}, 500mA/Div
Time: 20µs/Div

Short Circuit Protection



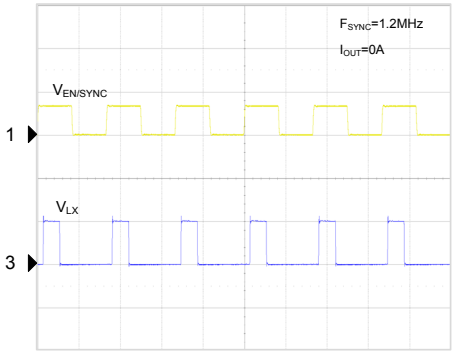
CH2: V_{OUT}, 1V/Div
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 10ms/Div

Steady State



CH2: V_{OUT}, 50mV/Div, V_{OFFSET}=1.05V
CH3: V_{LX}, 5V/Div
CH4: I_L, 1A/Div
Time: 1µs/Div

Synchronization

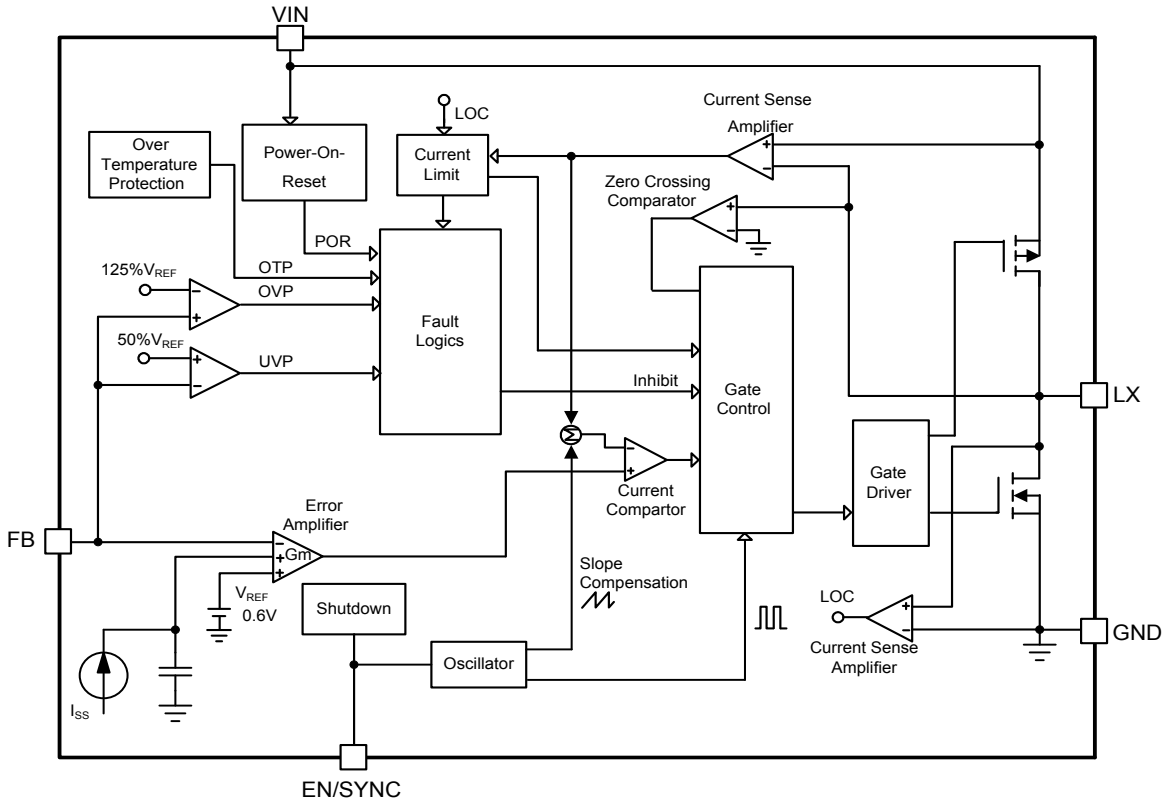


CH1: $V_{EN/SYNC}$, 5V/Div
CH3: V_{LX}, 5V/Div
Time: 500ns/Div

Pin Description

PIN		FUNCTION
NO.	NAME	
1	EN/SYNC	Enable_Synchronous Clock Input Pin. Drive EN high to turn the converter on and drive it low to turn them off. And Input an external clock signal to this pin for synchronization function.
2	GND	IC Ground Pin. This pin must be connected directly to the ground plane of the PCB.
3	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
4	VIN	Power Input Pin. VIN supplies the power to the buck converter and the the internal control circuitry.
5	FB	Output Feedback Pin. FB Pin senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.

Block Diagram



Typical Application Circuit

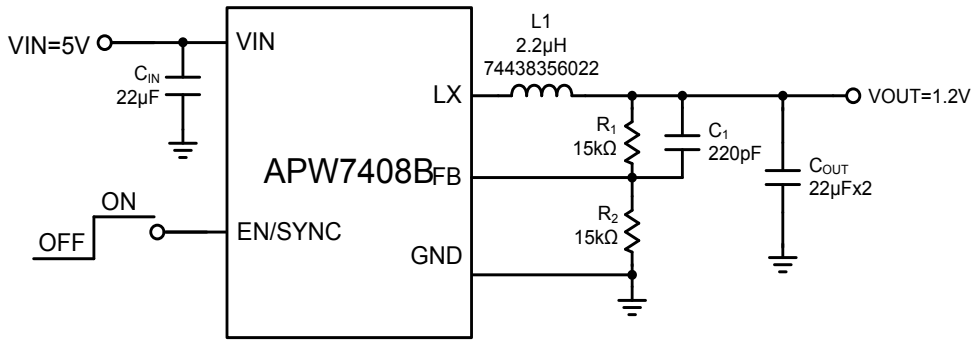


Figure 1. VOUT=1.2V

Components Selection for Different Output Voltage (Note 4)

VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
5	1.2	0 ~ 1.3A	22µ × 1	2.2µ	22µ × 2	15k (1%)	15k (1%)	220p
5	1.8	0 ~ 1.3A	22µ × 1	3.3µ	22µ × 2	30k (1%)	15k (1%)	180p
5	3.3	0 ~ 1.3A	22µ × 1	3.3µ	22µ × 2	68k (1%)	15k (1%)	100p

Note 4: This table is for internal frequency only.
Please contact the original manufacturer for the applicable specifications of the SYNC function.

Function Descriptions

VIN Power-On-Reset (POR)

The IC continuously monitors the voltage on the VIN pin. The soft start is activated when the VIN voltage and the EN voltage are above their respective POR thresholds. VIN POR is used to protect the IC from erroneous operation with insufficient VIN voltage. VIN POR also has hysteresis to resist ripple on the VIN voltage.

Output Under-Voltage Protection (UVP)

After the soft start is completed, the IC continuously monitors the output voltage through the FB pin. When the FB voltage drops below the UVP threshold due to an output short circuit, UVP is triggered.
UVP will turn off the converter to prevent the IC from being damaged in the event of a short circuit for a long time. In order to initiate a restart, remove and restore VIN power to the IC or toggle the EN pin.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Current-Limit Protection and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When any output voltage drops below the UVP threshold, UVP is triggered and both converters enter hiccup mode.
In hiccup mode, the converters will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over current condition is removed, the IC will exit the hiccup mode.

Over-Voltage Protection

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as
VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Output Discharge

When the EN signal is used to turn off the converter, the IC initiates a discharge process to cause the output voltage to drop rapidly. During output discharge, the high-side MOSFET will be turned off and the low-side MOSFET will be turned on to allow the output capacitor to discharge through the low side MOSFET until the discharge current reaches the low side MOSFET current limit, at which point the low-side MOSFET will be turned off. When the discharge current returns to zero, the low-side MOSFET will be turned on again. Until the FB voltage drops below 0.1V, the discharge process will end and the IC will be turned off.

Enable/Shutdown and Frequency synchronization

The IC provides the EN pin, which is a digital input that turns the converter on or off. Drive EN high to turn the converter on and drive it low to turn it off.
To synchronize the internal operating frequency of the IC with the external clock, connect the EN/SYNC pin to an external 50% duty cycle clock. The rising edge of the internal clock is synchronized with the rising edge of the external clock.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to “Typical Application Circuit”. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

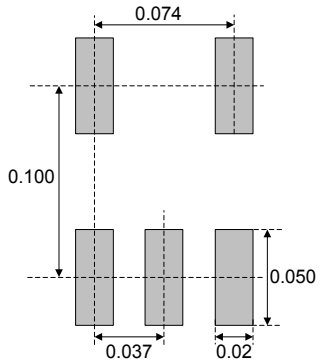
Application Information (Cont.)

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/ PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN / PGND to capacitor less than 2mm respectively is recommended.
2. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
3. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
4. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
5. For better heat dissipation, it is strongly recommended to enlarge the thermal pad area as much as possible and place a large ground plane on each PCB layer below the thermal pad position, and place as many vias as possible from the top layer to the bottom layer on the thermal pad and around the ground plane.
6. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

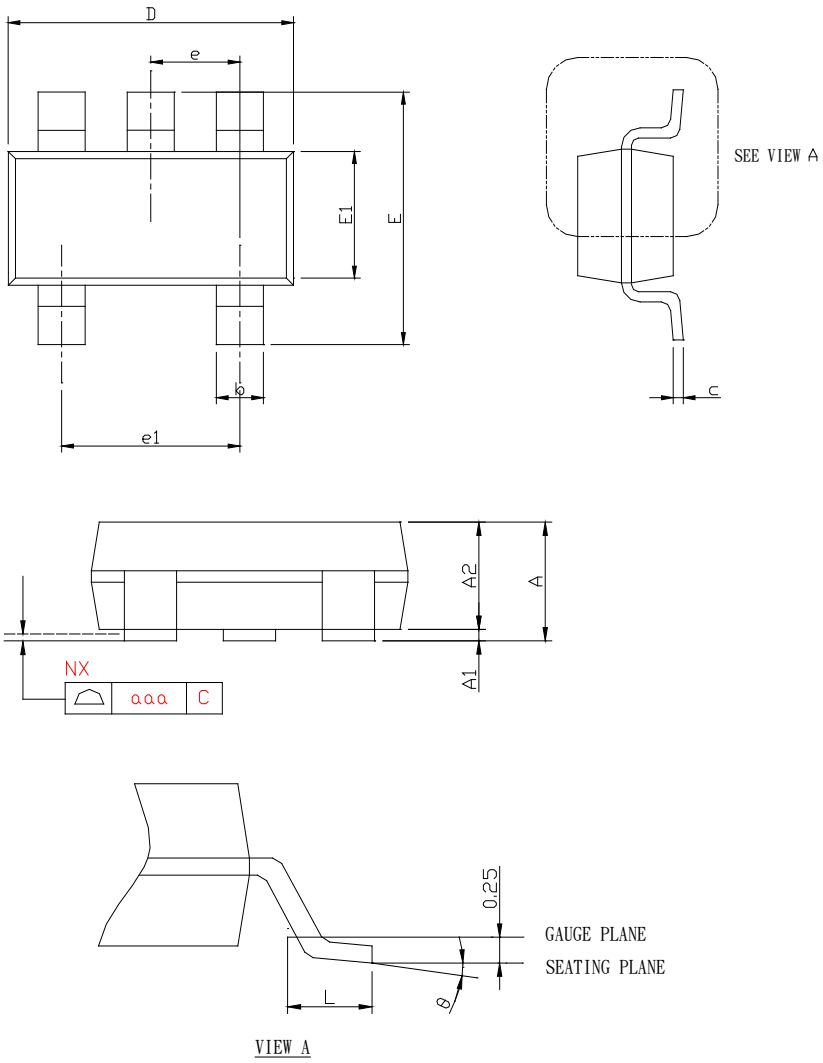
Recommended Minimum Footprint (Top View)



Unit : Inch

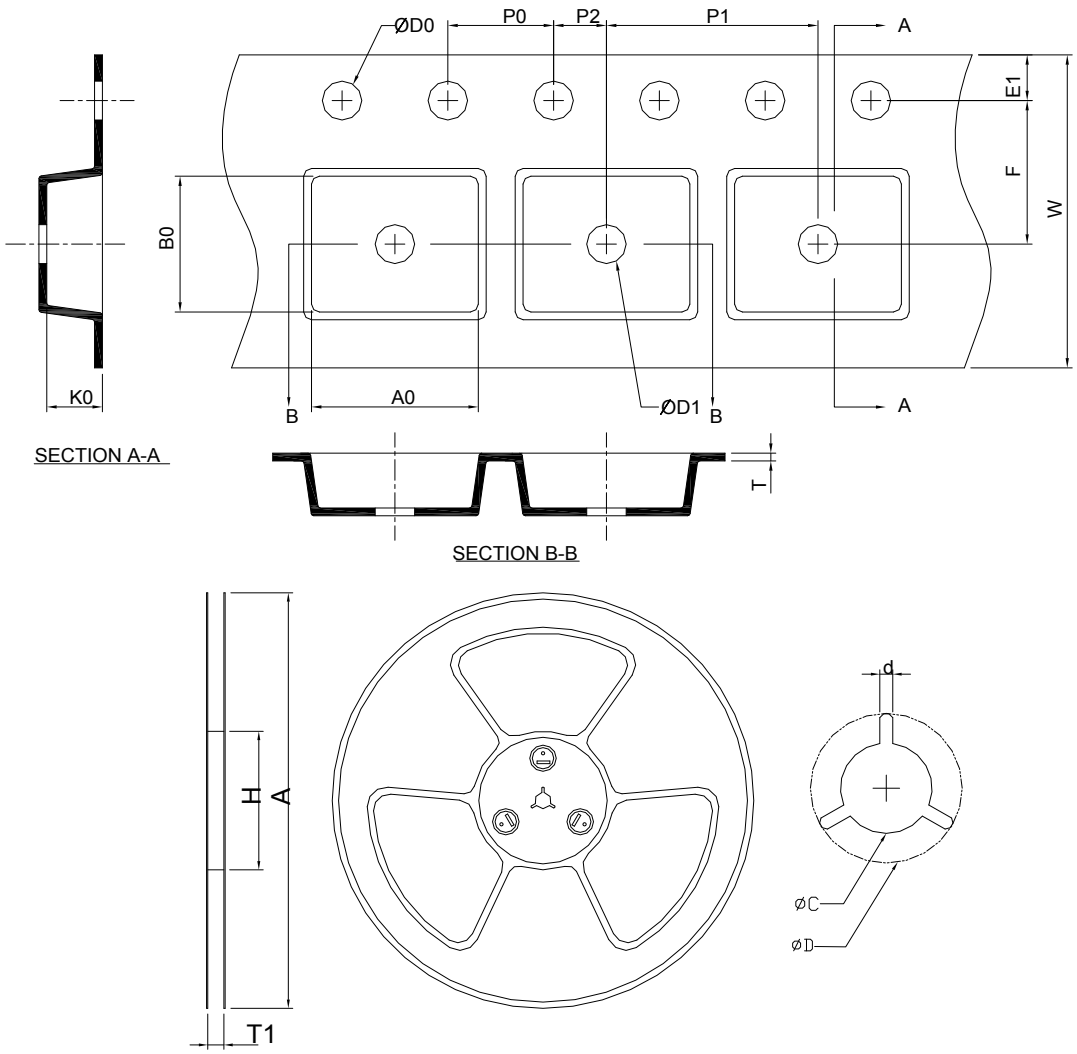
Package Information

SOT-23-5



SYMBOL	SOT-23-5					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP	MAX.
A	1.00	1.16	1.45	0.039	0.046	0.057
A1	0.00	0.05	0.15	0.000	0.002	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	0.38	0.50	0.012	0.015	0.020
c	0.08	0.17	0.22	0.003	0.007	0.009
D	2.70	2.93	3.10	0.106	0.115	0.122
E	2.60	2.83	3.00	0.102	0.111	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
θ	0°	4°	8°	0°	4°	8°
aaa	0.10			0.004		

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT 23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

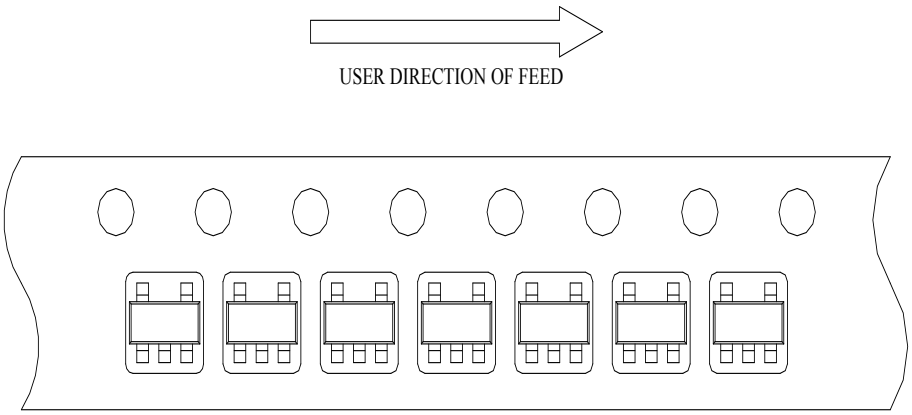
(mm)

Devices Per Unit

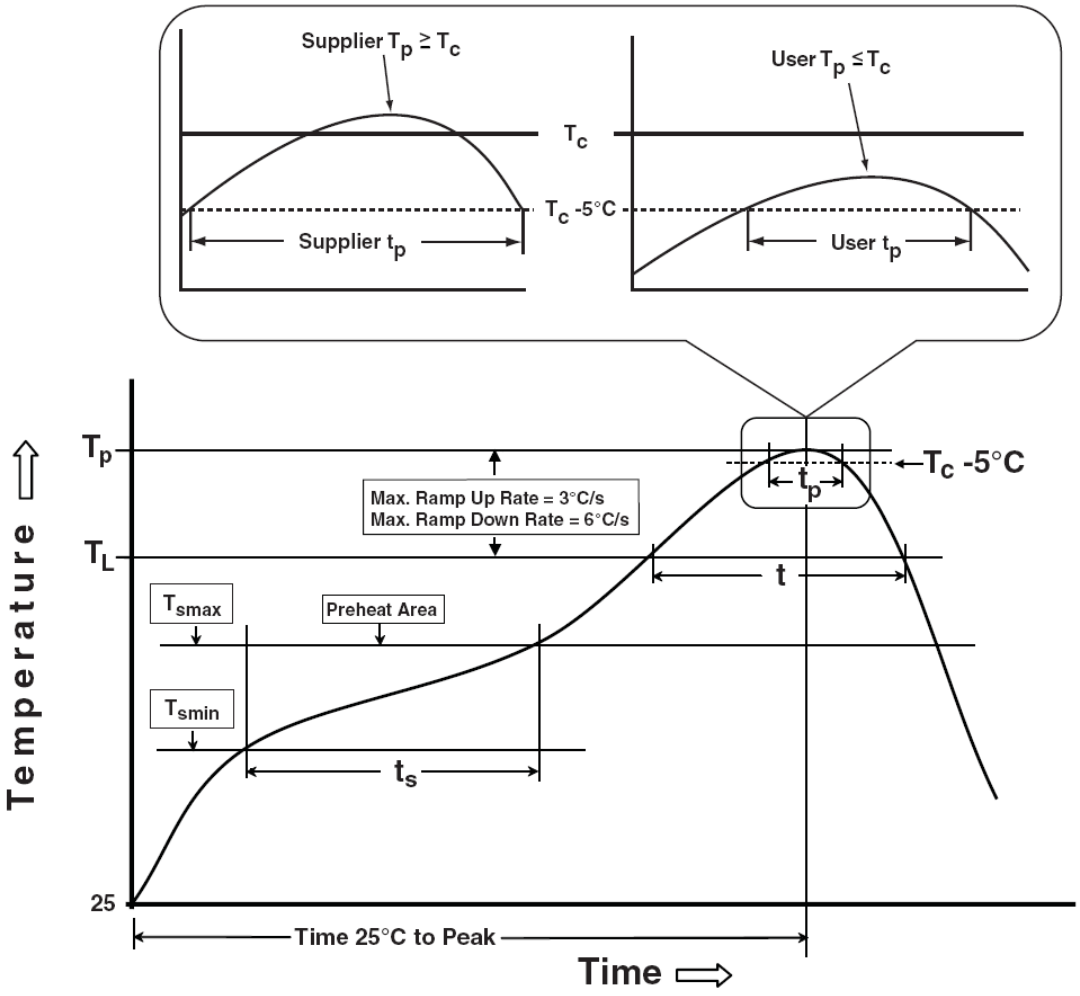
Package type	Packing	Quantity
SOT-23-5	Tape & Reel	3000

Taping Direction Information

SOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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