18V Input, Dual 6A and 3A Synchronous Buck with Sync Pin

Features

- **Wide Input Voltage from 4.5V to 18V.**
- **6A/3A Output Current on Channel 1/2.**
- **Low I_Q=150uA (typ.) per channel supply to improve Light Load Efficiency at Sync off.**
- **Typical 0.6V +1%Internal Reference Voltage.**
- **Easy to use I^2C interface**
  - **Programmable VOUT by control VFB Reference Voltage from 408~790.5mV in 1.5mV steps.**
  - **Adjustable Frequency in 4 steps, 500kHz, 600kHz, 800kHz and 1.2MHz**
  - **Adjustable Voltage Step Slew Rate in 3 steps, 0.75mV/uSec, 1.5mV/uSec, 3mV/uSec**
  - **Selectable PSM/PWM mode or PWM mode only**
  - **Support 8 sets of Slave address by an resistor.**
  - **Independent salve address for each channel.**
  - **I^2C Control Function: Soft-Enable and Soft-Reset.**
- **Sync Pin Allows Synchronization to an External Clock from 500kHz to 2MHz.**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **N-CH MOSFET (28 mW) for CH1 High Side.**
  - **N-CH MOSFET (16 mW) for CH1 Low Side.**
  - **N-CH MOSFET (70 mW) for CH2 High Side.**
  - **N-CH MOSFET (25 mW) for CH2 Low Side.**
- **Independent External Soft-Start Control for each channel.**
- **Separate EN and for Easy Sequencing.**
- **PG pin indicating both Channels Power Good.**
- **Built in OVP, UVP, Current Limit and OTP.**
- **Low Cost TQFN5x5-28 package.**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Digital Subscriber Line**
- **Passive Optical Network**
- **G.fast**
- **Set-Top-Box**

General Description

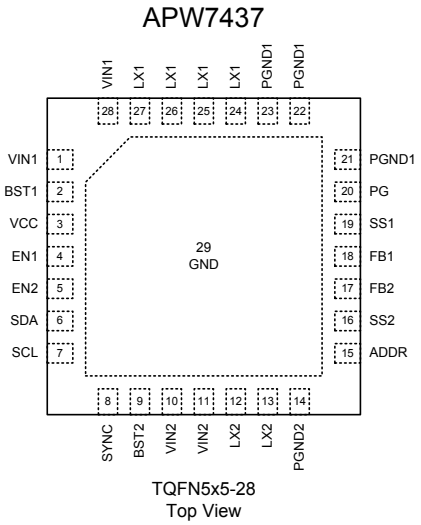
The APW7437 is a two-channel synchronous mode PWM converter with 6A continuous current capability for one channel and 3A continuous current capability for the other one.

Each channel of the APW7437 has independent enable and soft-start control pins, and It also allows the two regulators to start together by using the same enable signal and the same soft-start capacitor. In addition to changing the switching frequency through the I2C function, the APW7437 can also synchronize the switching frequency with an external clock frequency through the SYNC pin.

The APW7437 also provides a 180-degree phase shifting technique to minimize switching noise. The output voltage of each channel can be adjusted using an external resistor divider or by adjusting the internal reference voltage through I2C. Other features include UVP, current limit , and OTP.

The APW7437 is available in a TQFN5x5-28 package with small size and excellent thermal capacity.

Pin Configuration



TQFN5x5-28
Top View

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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Ordering and Marking Information

APW7437 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB: TQFN5x5-28 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7437 QB :  	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN1 to PGND1, VIN2 to PGND2	-0.3 ~ 21	V
V_{BST}	BST1 to PGND1, BST2 to PGND2	-0.3 ~ 26	V
V_{LX}	LX1 to PGND1, LX2 to PGND2	-1 ~ 20	V
$V_{I/O}$	VCC, ADDR, PG, SYNC, FB1/2, EN1/2, SS1/2, SCL, SDA to GND	-0.3 ~ 6	V
V_{GND}	PGND1, PGND2 to GND	-0.3 ~ 0.3	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
P_D	Power Dissipation @ T_A = 25 °C (Note 2)	2.78	W
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	36	°C/W
θ_{JC}	Junction-to-Ambient Case in free air (Note 2)	5	°C/W
θ_{JA}	Junction-to-Ambient Resistance (Note 3)	23.6	°C/W

Note 2: θ_{JA} is measured on 4 layers test board following the EIA/JESD51-7.
Note 3: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Range	Unit
V_{IN}	VIN supply voltage		4.5 ~ 18	V
V_{EN}	EN1 and EN2 input voltage		0 ~ 5	V
V_{OUT}	Converter output voltage		0.68 ~ 5	V
I_{OUT}	Converter output current	CH1	0 ~ 6	A
		CH2	0 ~ 3	
F_{SYNC}	Synchronization Frequency Range		500 ~ 2000	kHz
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=5V. Typical values are at T_J=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT (for CH1 and CH2)						
I_{VIN}	VIN Input Current	V_{FB}=1V, LX=NC	-	150	-	uA
I_{VIN_STB}	VIN Standby Current	CH1 and CH2 Soft_EN=1, EN=5V	-	-	40	uA
I_{VIN_SHDN}	VIN Shutdown Current	EN=GND	-	-	5	uA
POWER-ON RESET (for CH1 and CH2)						
V_{POR}	VCC POR Threshold Voltage	VCC Rising	-	4.3	-	V
V_{POR_Hys}	VCC POR Hysteresis Voltage	VCC Falling	-	0.4	-	V
T_{DB_POR}	VCC POR On Debounce Time		-	50	-	us
T_{D_POR}	VCC POR On Delay Time	When VCC POR On to LX Switching	-	600	-	us
EN Threshold (for CH1 and CH2)						
V_{EN_H}	EN Input Threshold High Voltage		1.2	-	-	V
V_{EN_L}	EN Input Threshold Low Voltage		-	-	0.5	V
T_{DB_EN}	EN Turn On Debounce Time		-	20	-	us
T_{D_EN}	EN Turn On Delay Time	When EN High to LX Switching	-	700	-	us
I_{EN}	EN Input Current	V_{EN}=5.5V	-	-	0.1	uA
REFERENCE VOLTAGE (for CH1 and CH2)						
V_{REF}	Reference Voltage	T_J=25°C, I^2C V_{REF} setting = Default	594	600	606	mV
	Load Regulation	VOUT1=1V/0~6A, VOUT2=1V/0~3A	-	0.4	-	%
	Transition Slew Rate	I^2C V_{REF} setting changed, TSR[1:0]=00	-	0.75	-	mV/us
	Reference Voltage Differential		-	1.5	-	mV
	Reference Voltage DNL		-1	-	1	LSB
	Reference Voltage INL		-4	-	4	LSB
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A	-	5	-	V
	VCC Load Regulation	I_{VCC}=10mA (Note 5)	-	3	-	%
	VCC Maximum Current	When VCC drop to 4.75V	40	-	-	mA
I_{SS}	Soft Start Current		8	10	12	uA
R_{DIS}	Internal Discharge Resistor		-	100	-	Ω
OSCILLATOR AND SYNCHRONIZATION FREQUENCY						
F_{OSC}	Oscillator Frequency	I^2C configurable by Reg0x02[1:0]=01 (default)	-	600	-	kHz
	Frequency Accuracy	T_J=-40~125°C	-20	-	+20	%
	Minimum on Time		-	70	-	ns
	Maximum Duty		-	90	-	%
V_{SYNC_H}	SYNC Input Threshold High Voltage		2.5	-	-	V
V_{SYNC_L}	SYNC Input Threshold Low Voltage		-	-	0.8	V
	Allowable SYNC Duty Cycle		40	-	60	%

Note 5: Internal use only.

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Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN}=5V. Typical values are at T_J=25°C.

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
POWER MOSFET (for CH1 and CH2)						
	CH1 High Side MOSFET Resistance		-	28	-	mΩ
	CH1 Low Side MOSFET Resistance		-	16	-	mΩ
	CH2 High Side MOSFET Resistance		-	70	-	mΩ
	CH2 Low Side MOSFET Resistance		-	25	-	mΩ
	High Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=GND	-	1	-	μA
	Low Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=VIN	-	1	-	μA
	Dead Time		-	10	-	ns
BOOTSTRAP POWER (for CH1 and CH2)						
V_{BST-LX_POR}	BST to LX Output POR Voltage	V_{BST} - V_{LX}	-	3.3	-	V
R_{BST}	BST Switch On Resistance	V_{EN}=5V, LX=-0.1V, BST Source 10mA	-	10	-	Ω
	BST Leakage Current	V_{BST-LX}=5.5V	-	-	0.1	μA
PHASE SHIFT and ADDRESS						
	CH1 and CH2 Phase Shift		-	180	-	degree
ADDR	Address Latch Time		-	600	-	us
I_{ADDR_LEAK}	ADDR Leakage Current		-	-	0.1	uA
PROTECTIONS (for CH1 and CH2)						
I_{LIM}	High Side MOSFET current-limit	For CH1	-	9	-	A
		For CH2	-	5	-	
	Over-temperature Trip Point		-	150	-	°C
	Over-temperature Hysteresis		-	30	-	°C
	FB Over Voltage Protection		120	125	130	%V_{REF}
	FB Over Voltage Protection Hysteresis		-	5	-	%V_{REF}
	Under Voltage Protection		40	50	60	%V_{REF}
	Hiccup Count Times		-	8	-	t_{ss}
POWER- GOOD INDICATOR						
	PG Low Level Threshold	VOUT Rising, PG goes High	-	90	-	%
	PG Low Level Hysteresis	VOUT Falling, PG goes Low	-	5	-	%
	PG High Level Threshold	VOUT Rising, PG goes Low	120	125	130	%
	PG High Level Hysteresis	VOUT Falling, PG goes High	-	5	-	%
	PG Leakage Current	V_{PG}=5V	-	0.1	1	uA
	PG Sink Capability	When PG pin pull low, PG sink 50mA	-	-	0.8	V
	PG goes High Debounce Time		-	20	-	us

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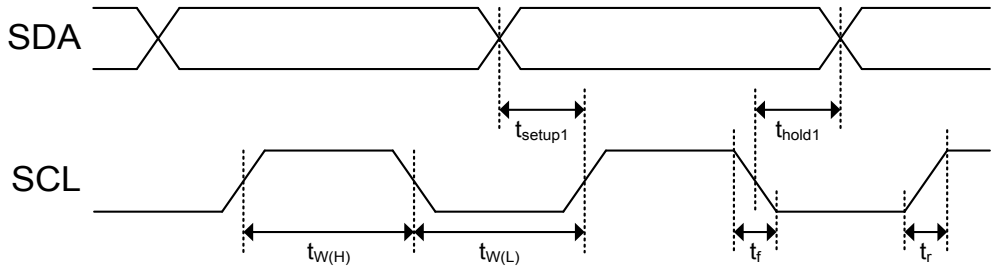
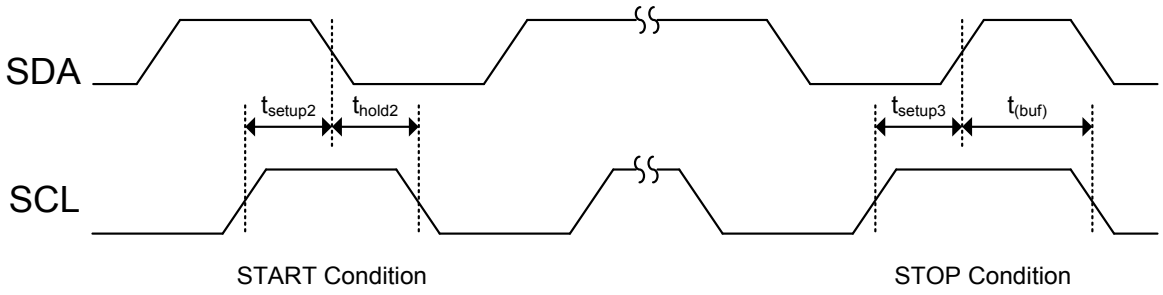
Electrical Characteristics (Cont.)

Timing characteristics for I^2C Interface signals over recommended operating conditions (unless otherwise noted).

Symbol	Parameter	Fast Speed Plus		Fast Speed		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Frequency, SCL	-	1	-	0.4	MHz
$t_{W(H)}$	Pulse Duration, SCL High	260	-	600	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low	500	-	1300	-	ns
t_r	Rise Time, SCL and SDA	-	120	20+0.1 C_L(pF)	300	ns
t_f	Fall Time, SCL and SDA	-	120	20+0.1 C_L(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	-	-	100	-	ns
t_{hold1}	Hold Time, SCL to SDA	-	-	100	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition	500	-	1300	-	ns
t_{setup2}	Setup Time, SCL to Start Condition	-	-	600	-	ns
t_{hold2}	Hold Time, Start condition to SCL	-	-	600	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition	-	-	600	-	ns
C_L	Load Capacitance for Each Bus Line	-	-	-	400	pF



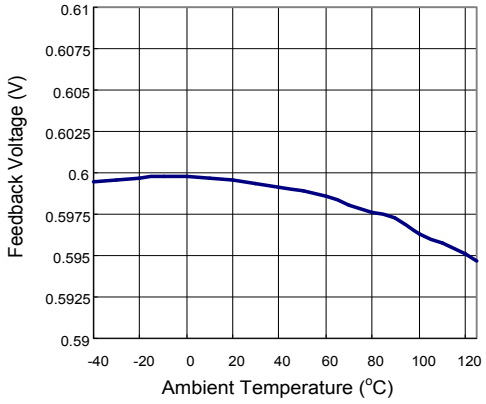
SDA and SCL Timing



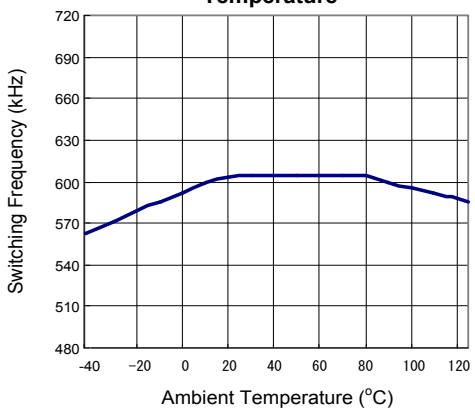
START and STOP Condition Timing

Typical Operating Characteristics

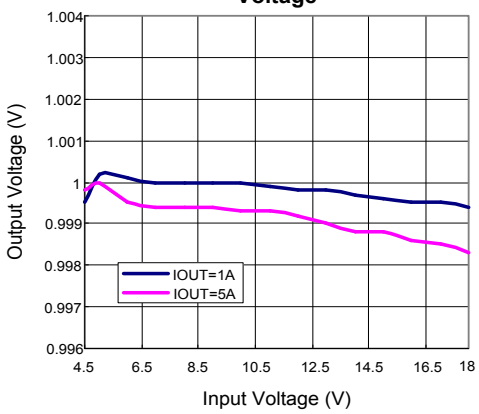
Feedback Voltage vs. Ambient Temperature



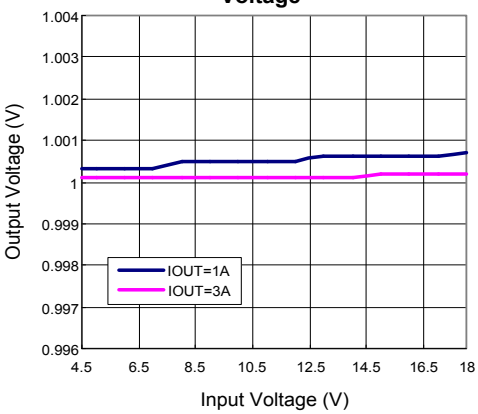
Switching Frequency vs. Ambient Temperature



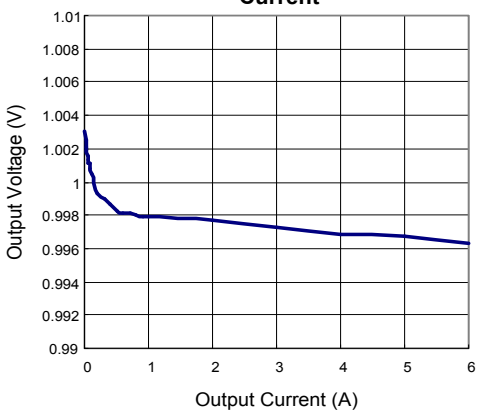
CH1 Output Voltage vs. Input Voltage



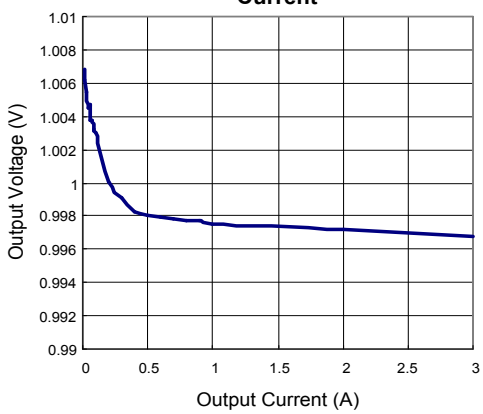
CH2 Output Voltage vs. Input Voltage



CH1 Output Voltage vs. Output Current



CH2 Output Voltage vs. Output Current



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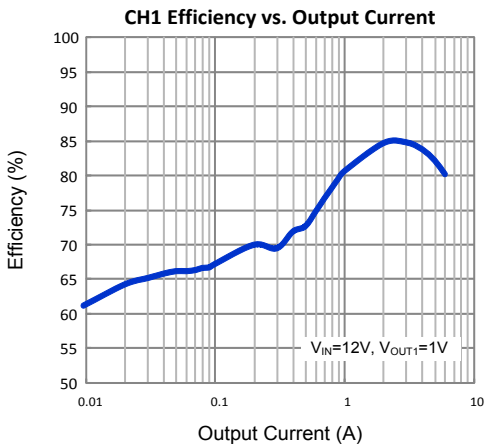
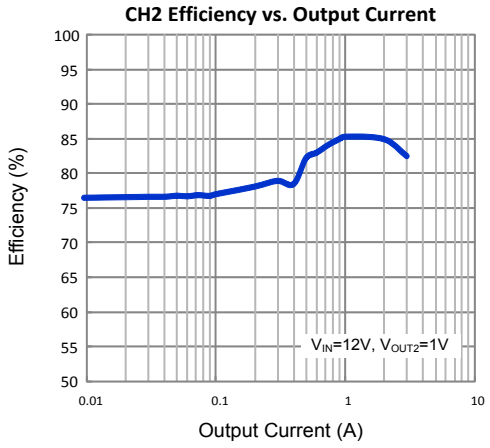
Typical Operating Characteristics (Cont.)

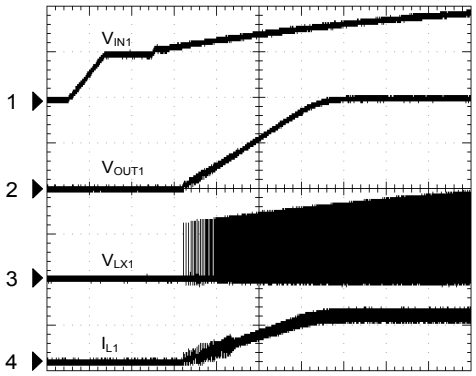




OperatingWaveforms

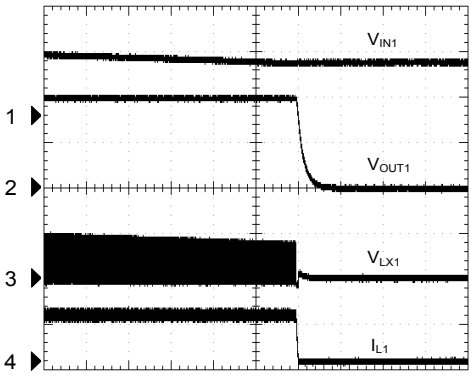
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

CH1 Power On



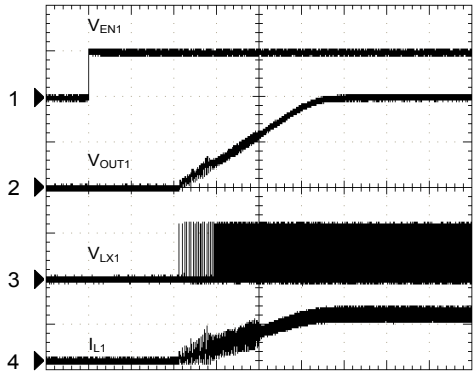
CH1: V_{IN1}, 5V/Div
CH2: V_{OUT1}, 500mV/Div
CH3: V_{LX1}, 5V/Div
CH4: I_{L1}, 5A/Div
Time: 400us/Div

CH1 Power Off



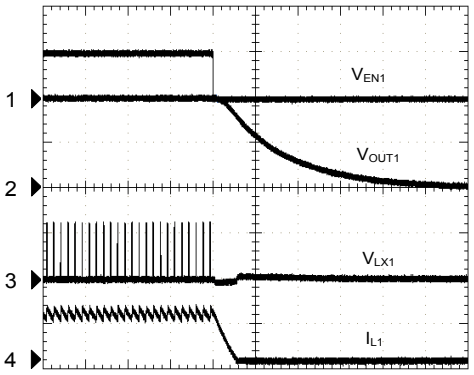
CH1: V_{IN1}, 5V/Div
CH2: V_{OUT1}, 500mV/Div
CH3: V_{LX1}, 5V/Div
CH4: I_{L1}, 5A/Div
Time: 100us/Div

CH1 Enable



CH1: V_{EN1}, 5V/Div
CH2: V_{OUT1}, 500mV/Div
CH3: V_{LX1}, 10V/Div
CH4: I_{L1}, 5A/Div
Time: 400us/Div

CH1 Disable



CH1: V_{EN1}, 5V/Div
CH2: V_{OUT1}, 500mV/Div
CH3: V_{LX1}, 10V/Div
CH4: I_{L1}, 5A/Div
Time: 10us/Div

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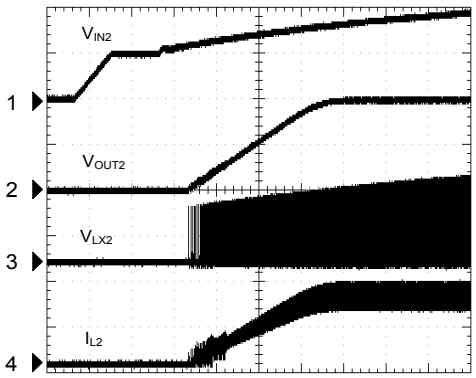
OperatingWaveforms (Cont.)

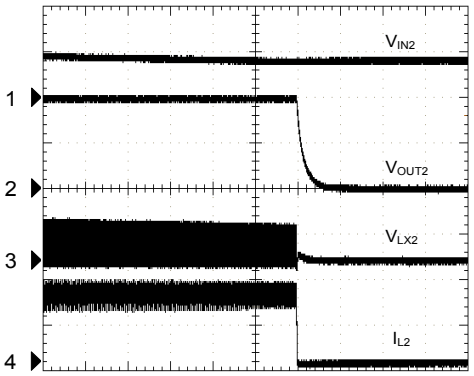
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

CH2 Power On



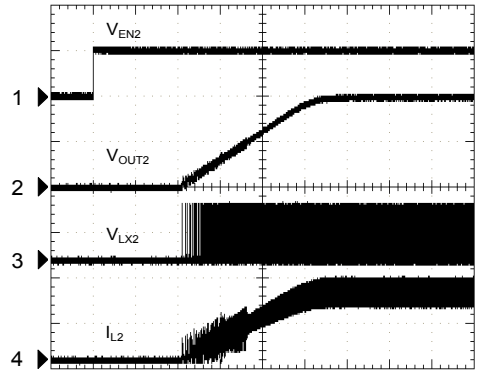
CH1: V_{IN2}, 5V/Div
CH2: V_{OUT2}, 500mV/Div
CH3: V_{LX2}, 5V/Div
CH4: I_{L2}, 2A/Div
Time: 400us/Div

CH2 Power Off



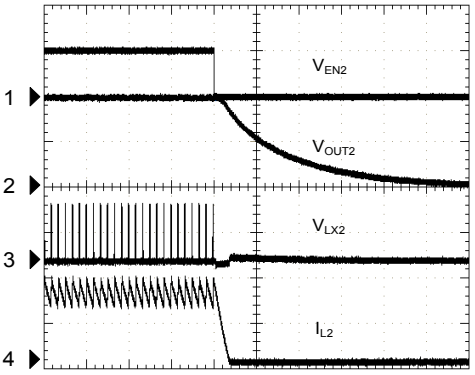
CH1: V_{IN2}, 5V/Div
CH2: V_{OUT2}, 500mV/Div
CH3: V_{LX2}, 5V/Div
CH4: I_{L2}, 2A/Div
Time: 400us/Div

CH2 Enable



CH1: V_{EN2}, 5V/Div
CH2: V_{OUT2}, 500mV/Div
CH3: V_{LX2}, 10V/Div
CH4: I_{L2}, 2A/Div
Time: 400us/Div

CH2 Disable



CH1: V_{EN2}, 5V/Div
CH2: V_{OUT2}, 500mV/Div
CH3: V_{LX2}, 10V/Div
CH4: I_{L2}, 2A/Div
Time: 10us/Div

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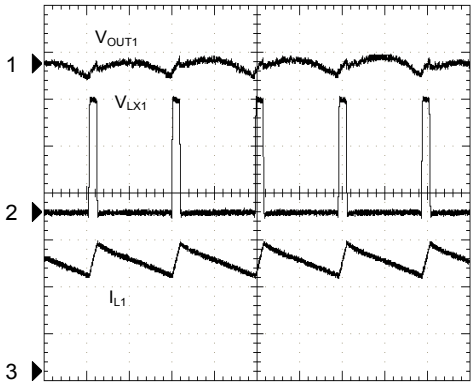
OperatingWaveforms (Cont.)

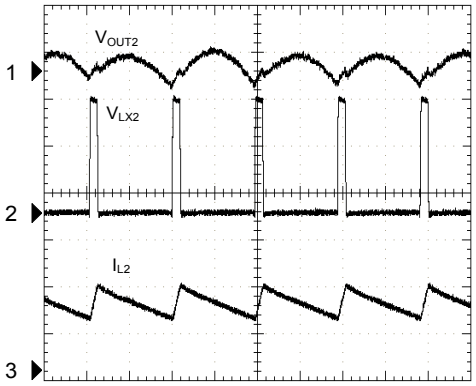
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

CH1 Output Ripple



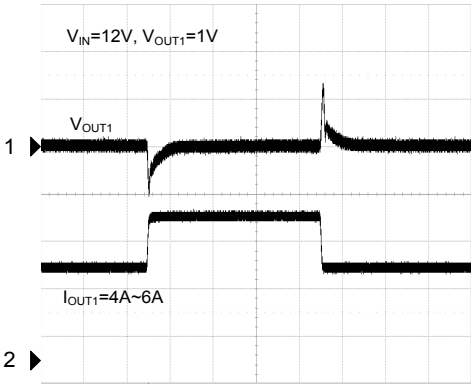
CH1: V_{OUT1}, 20mV/Div, AC
CH2: V_{LX1}, 5V/Div, DC
CH3: I_{L1}, 2A/Div
Time: 1us/Div

CH2 Output Ripple



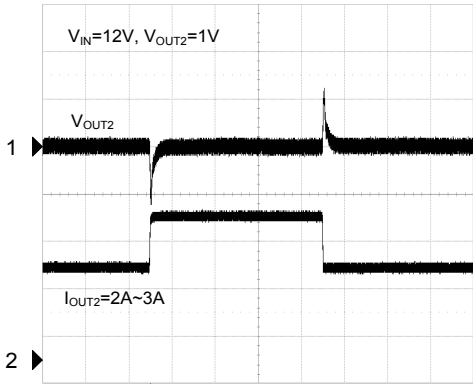
CH1: V_{OUT2}, 20mV/Div, AC
CH2: V_{LX2}, 5V/Div, DC
CH3: I_{L2}, 2A/Div
Time: 1us/Div

CH1 Load Transient



CH1: V_{OUT1}, 50mV/Div, AC
CH2: I_{OUT1}, 2A/Div
Time: 100us/Div

CH2 Load Transient

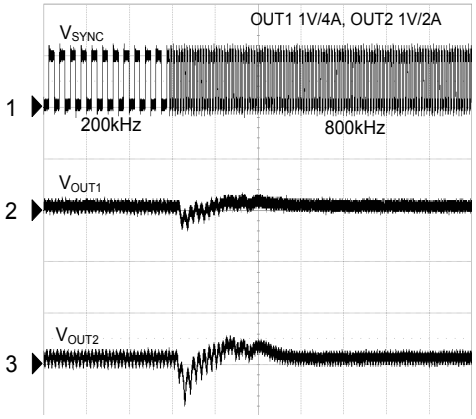


CH1: V_{OUT1}, 50mV/Div, AC
CH2: I_{OUT2}, 1A/Div
Time: 100us/Div

OperatingWaveforms (Cont.)

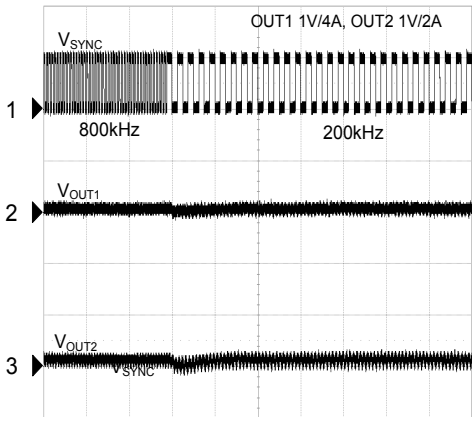
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

External SYNC Clock



CH1: V_{SYNC}, 5V/Div
CH2: V_{OUT1}, 50mV/Div, AC
CH3: V_{OUT2}, 50mV/Div, AC
Time: 20us/Div

External SYNC Clock



CH1: V_{SYNC}, 5V/Div
CH2: V_{OUT1}, 50mV/Div, AC
CH3: V_{OUT2}, 50mV/Div, AC
Time: 20us/Div

Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1, 28	VIN1	CH1 Power Input Pin. VIN1 supplies the power to the CH1 buck converter.
2	BST1	CH1 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX1 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
3	VCC	Internal Regulator Output Pin. The VCC pin is the output of an internal 5V regulator for internal control circuitry. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
4	EN1	CH1 Enable Input Pin. Drive EN1 high to turn the CH1 converter on and drive it low to turn it off. The EN1 pin cannot be left floating.
5	EN2	CH2 Enable Input Pin. Drive EN2 high to turn the CH2 converter on and drive it low to turn it off. The EN2 pin cannot be left floating.
6	SDA	I^2C Data Connection Pin.
7	SCL	I^2C Clock Signal Pin.
8	SYNC	Synchronous Clock Input Pin. Input an external 500kHz to 2MHz clock signal to this pin for synchronization function. If the SYNC pin is not used, it should be grounded.
9	BST1	CH2 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX2 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
10, 11	VIN2	CH2 Power Input Pin. VIN2 supplies the power to the CH2 buck converter.
12, 13	LX2	CH2 Power Switching Output. These pins are the junction of the high side power MOSFET and the low side power MOSFET. Connect these pins to the output inductor.
14	PGND2	CH2 Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
15	ADDR	Slave Address Setting Pin. Connect a resistor from ADDR to ground to set the slave address.
16	SS2	CH2 Soft-start Time Setting Pin. Connect a Capacitor to GND to set the soft start interval.
17	FB2	CH2 Output Feedback Pin. FB2 senses the output voltage of channel2 and regulates it. Connect the resistor divider from the output through FB2 to the ground to set the output voltage.
18	FB1	CH1 Output Feedback Pin. FB1 senses the output voltage of channel1 and regulates it. Connect the resistor divider from the output through FB1 to the ground to set the output voltage.
19	SS1	CH1 Soft-start Time Setting Pin. Connect a Capacitor to GND to set the soft-start interval.
20	PG	Output Power Good Indicator Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage for the PG function.
21, 22, 23	PGND1	CH1 Power Ground. These pins must be connected directly to the GND plane of the PCB using low inductance vias.
24, 25, 26, 27	LX1	CH1 Power Switching Output. These pins are the junction of the high side power MOSFET and the low side power MOSFET. Connect these pins to the output inductor.
29	GND	The Ground of IC.

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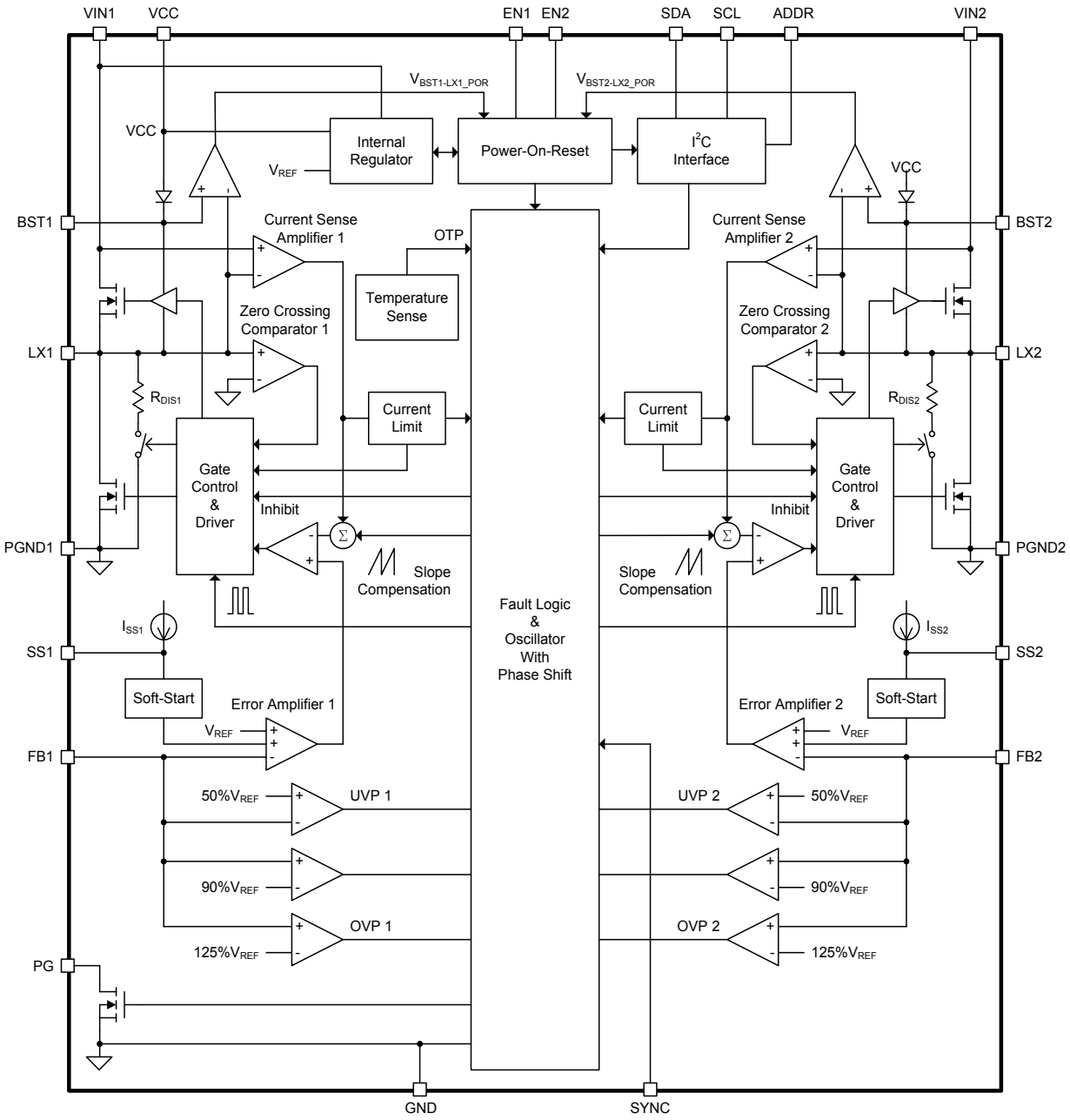
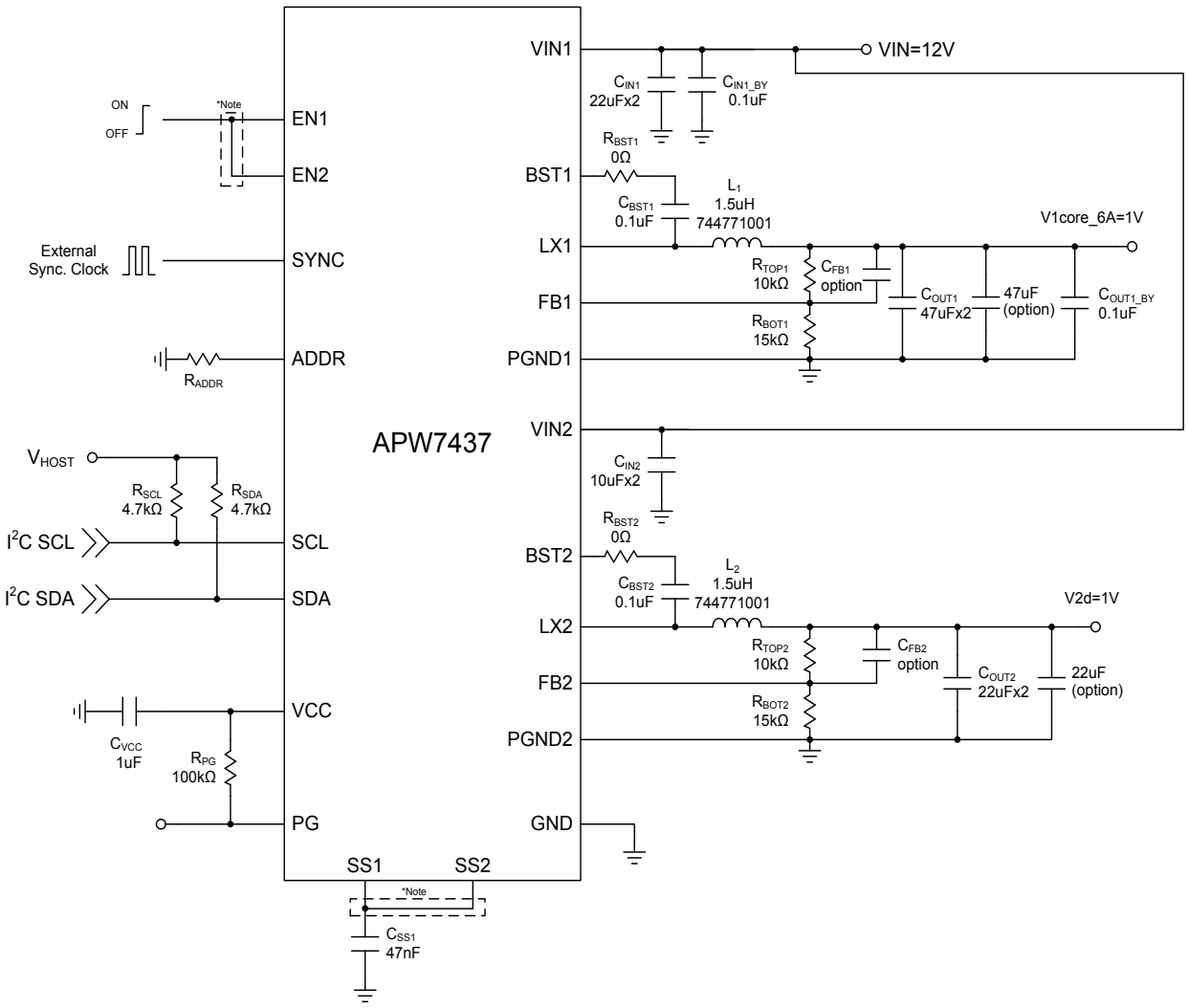
Block Diagram



Typical Application Circuit 1 : VOUT1/2 power up simultaneously

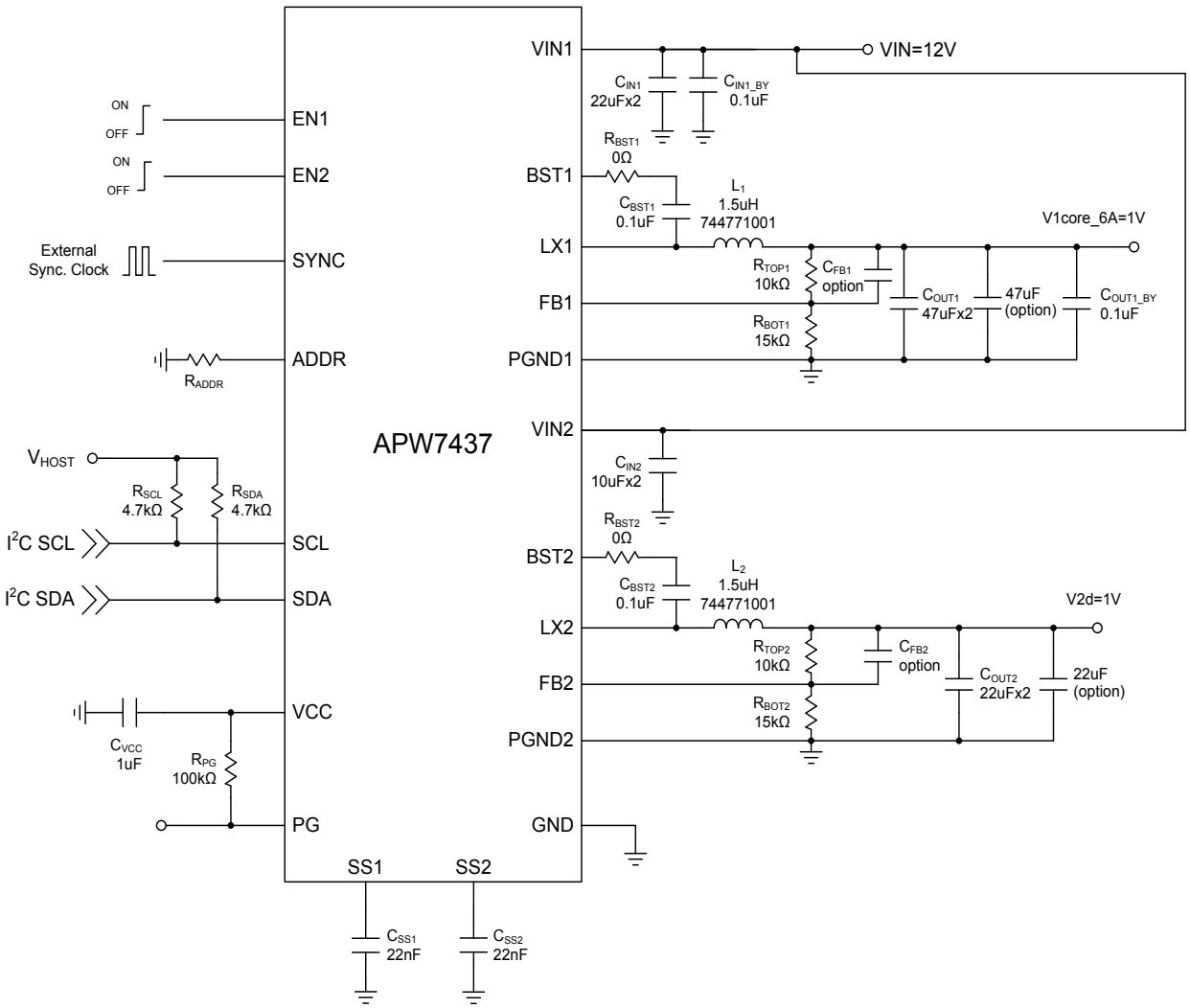


Components Selection for Different Output Voltage

Application	Channel	VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
1	1	12	1	0 ~ 6A	22u × 2	1.5u	47u × 2	10k	15k	option
	2	12	1	0 ~ 3A	10u × 2	1.5u	22u × 2	10k	15k	option
2	1	12	3.3	0 ~ 6A	22u × 2	3.5u	47u × 2	68k	15k	160p
	2	12	3.3	0 ~ 3A	10u × 2	3.5u	22u × 2	68k	15k	160p
3	1	12	5	0 ~ 6A	22u × 2	4.7u	47u × 2	110k	15k	39p
	2	12	3.3	0 ~ 3A	10u × 2	3.5u	22u × 2	68k	15k	160p

Note: If the SS1 and SS2 connect to the same capacitor, then the CH1 & CH2 I^2C soft-Enable command can't be used.

Typical Application Circuit 2 : Independent Channel Operation



Components Selection for Different Output Voltage

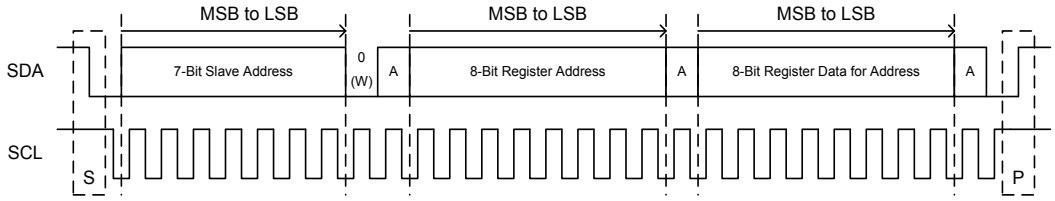
Application	Channel	VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
1	1	12	1	0 ~ 6A	22u × 2	1.5u	47u × 2	10k	15k	option
	2	12	1	0 ~ 3A	10u × 2	1.5u	22u × 2	10k	15k	option
2	1	12	3.3	0 ~ 6A	22u × 2	3.5u	47u × 2	68k	15k	160p
	2	12	3.3	0 ~ 3A	10u × 2	3.5u	22u × 2	68k	15k	160p
3	1	12	5	0 ~ 6A	22u × 2	4.7u	47u × 2	110k	15k	39p
	2	12	3.3	0 ~ 3A	10u × 2	3.5u	22u × 2	68k	15k	160p

I²C Programming

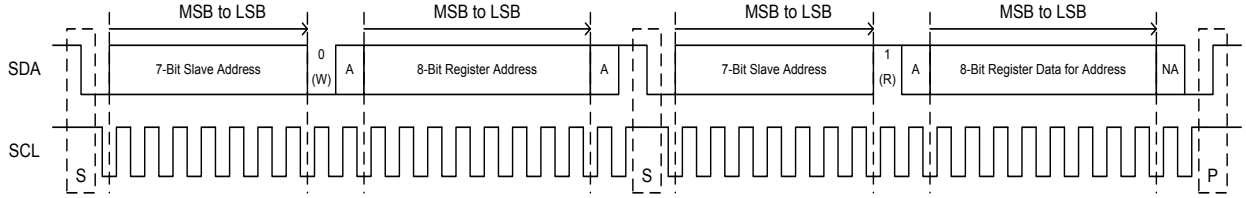
The APW7437's I²C Slave Addresses are two hard-coded 7 bit address as below table. The APW7437 supports the following write and read protocol and contains 16 registers.

ADDR Resistor Configuration Mapping to I2C Slave Address

RADDR (kΩ)	Affected Channel	7-bits Slave Address	Bits							
			D7	D6	D5	D4	D3	D2	D1	D0(R/W)
0	CH1	0x0A	0	0	0	1	0	1	0	x
	CH2	0x0B	0	0	0	1	0	1	1	x
5.1	CH1	0x1A	0	0	1	1	0	1	0	x
	CH2	0x1B	0	0	1	1	0	1	1	x
12	CH1	0x2A	0	1	0	1	0	1	0	x
	CH2	0x2B	0	1	0	1	0	1	1	x
24	CH1	0x3A	0	1	1	1	0	1	0	x
	CH2	0x3B	0	1	1	1	0	1	1	x
47	CH1	0x4A	1	0	0	1	0	1	0	x
	CH2	0x4B	1	0	0	1	0	1	1	x
100	CH1	0x5A	1	0	1	1	0	1	0	x
	CH2	0x5B	1	0	1	1	0	1	1	x
200	CH1	0x6A	1	1	0	1	0	1	0	x
	CH2	0x6B	1	1	0	1	0	1	1	x
400	CH1	0x7A	1	1	1	1	0	1	0	x
	CH2	0x7B	1	1	1	1	0	1	1	x



Master Write to a Slave Register Example



Master Read from a Slave Register Example

(S=START, P=STOP, A=ACK from Slave, NA=Non-ACK)

I²C Programming (Cont.)

I²C Registers Index

Affected Channel	Slave Address	Register Address	Register Name	Read/Write	Default Value
CH1	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})	0x00	CH1 Feedback Reference Voltage Setting Register (1.5mV/LSB)	R/W	0x80 (600mV)
		0x01	CH1 Fault Flag Register (OVP1, UVP1, CL1, OTP)	R	0x00
		0x03	CH1 Soft Enable (Normal, Standby) (*Note)	R/W	0x00 (Normal)
		0x04	CH1 Transition Slew Rate (0.75mV/us, 1.5mV/us, 3mV/us)	R/W	0x00 (0.75mV/us)
		0x05	CH1 Force PWM Mode (PSM/PWM, Force PWM)	R/W	0x00 (PSM/PWM)
		0x2F	Clear CH1 Fault Flag to Default	W	0x00
		0x3F	CH1 Soft Reset (Clear All CH1 Register to Default Value)	W	0x00
CH2	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})	0x00	CH2 Feedback Reference Voltage Setting Register (1.5mV/LSB)	R/W	0x80 (600mV)
		0x01	CH2 Fault Flag Register (OVP2, UVP2, CL2, OTP)	R	0x00
		0x03	CH2 Soft Enable (Normal, Standby) (*Note)	R/W	0x00 (Normal)
		0x04	CH2 Transition Slew Rate (0.75mV/us, 1.5mV/us, 3mV/us)	R/W	0x00 (0.75mV/us)
		0x05	CH2 Force PWM Mode (PSM/PWM, Force PWM)	R/W	0x00 (PSM/PWM)
		0x2F	Clear CH2 Fault Flag to Default	W	0x00
		0x3F	CH2 Soft Reset (Clear All CH2 Register to Default Value)	W	0x00
Common	0x0A ~ 0x7A or 0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})	0x02	Frequency Setting Register (D[1:0]=500kHz, 600kHz , 800kHz, 1200kHz)	R/W	0x01 (600kHz)
		0x06	IC Info. (Vender ID=D[7:4], Version ID=D[3:0])	R	0xAA
		0x07	IC ID	R	0x37
		0x7F	Soft Reset All (Clear All CH1, CH2 and Common Register to Default Value)	W	0x00

Note: If the SS1 and SS2 connect to the same capacitor, then the CH1 & CH2 I²C soft-Enable command can't be used.

I²C Programming (Cont.)

The CH1 I²C Registers Programming

Register Name	CH1 Feedback Reference Voltage Setting Register							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x00							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CH1_VREF_SET							
Read/Write	R/W							
Power On Default	1	0	0	0	0	0	0	0
Bit Name	Bit Definition							
CH1_VREF_SET	CH1_VOUT = (CH1_V_{REF}) / R2 x (R_{TOP} + R_{BOT}) (Note 6) 0x00: CH1_V_{REF} = 408.0mV (CH1_VOUT=0.680V) 0x01: CH1_V_{REF} = 409.5mV (CH1_VOUT=0.6825V) 0x02: CH1_V_{REF} = 411.0mV (CH1_VOUT=0.685V) ... 0x7E: CH1_V_{REF} = 597.0mV (CH1_VOUT=0.995V) 0x7F: CH1_V_{REF} = 598.5mV (CH1_VOUT=0.9975V) 0x80: CH1_V_{REF} = 600.0mV (CH1_VOUT=1.000V) (Default) 0x81: CH1_V_{REF} = 601.5mV (CH1_VOUT=1.0025V) 0x82: CH1_V_{REF} = 603.0mV (CH1_VOUT=1.005V) ... 0xFD: CH1_V_{REF} = 787.5mV (CH1_VOUT=1.3125V) 0xFE: CH1_V_{REF} = 789.0mV (CH1_VOUT=1.315V) 0xFF: CH1_V_{REF} = 790.5mV (CH1_VOUT=1.3175V)							

Note 6: Refer to the typical application circuit.

Register Name	CH1 Fault Flag Register							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x01							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	OVP1	UVP1	CL1	OTP
Read/Write	-	-	-	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
OVP1	CH1 Output Over Voltage Protection Flag.							
UVP1	CH1 Output Under Voltage Protection Flag.							
CL1	CH1 Current Limit Flag.							
OTP	Over Temperature Protection Flag.							

Note: The Fault Flag will be cleared when: 1.Clear fault function enable. 2. Both of EN pins are "L".

Register Name	CH1 Soft Enable							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x03							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	-	Soft_EN1
Read/Write	-	-	-	-	-	-	-	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
EN1_soft	0: Normal Operation. (Default) 1: Standby Mode. (The CH1 output voltage down to 0V, but Internal Regulator and I²C Function still existing.) (If the SS1 and SS2 connect to the same capacitor, then the CH1 & CH2 I²C soft-Enable command can't be used.)							

I²C Programming (Cont.)

Register Name	CH1 Transition Slew Rate							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x04							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	TSR1	
Read/Write	-	-	-	-	-	-	R/W	
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
TSR1	00: 0.75mV/us. (Default) 01: 1.5mV/us 10: 3mV/us 11: Reversed							

Register Name	CH1 Force PWM Mode							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x05							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	-	FPWM1
Read/Write	-	-	-	-	-	-	-	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
FPWM1	0: PSM/PWM mode automatic selection. (Default) 1: Force PWM Mode							

Register Name	CH1 Fault Flag Register							
Affected Channel	CH1							
Slave Address	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x01							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	OVP1	UVP1	CL1	OTP
Read/Write	-	-	-	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
OVP1	CH1 Output Over Voltage Protection Flag.							
UVP1	CH1 Output Under Voltage Protection Flag.							
CL1	CH1 Current Limit Flag.							
OTP	Over Temperature Protection Flag.							

Register Name	CH1 Soft Reset							
Affected Channel	0x0A ~ 0x7A (Configured by R_{ADDR1} and R_{ADDR2})							
Slave Address	0x0A							
Register Address	0x3F							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST1							
Read/Write	W							
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
RST1	Write any data into the register to clear all CH1 Registers to default value.							

I²C Programming (Cont.)

The CH2 I²C Registers Programming

Register Name	CH2 Feedback Reference Voltage Setting Register							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x00							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CH2_VREF_SET							
Read/Write	R/W							
Power On Default	1	0	0	0	0	0	0	0
Bit Name	Bit Definition							
CH2_VREF_SET	CH2_VOUT = (CH2_V_{REF}) / R2 x (R_{TOP} + R_{BOT}) (Note 6) 0x00: CH2_V_{REF} = 408.0mV (CH2_VOUT=0.680V) 0x01: CH2_V_{REF} = 409.5mV (CH2_VOUT=0.6825V) 0x02: CH2_V_{REF} = 411.0mV (CH2_VOUT=0.685V) ... 0x7E: CH2_V_{REF} = 597.0mV (CH2_VOUT=0.995V) 0x7F: CH2_V_{REF} = 598.5mV (CH2_VOUT=0.9975V) 0x80: CH2_V_{REF} = 600.0mV (CH2_VOUT=1.000V) (Default) 0x81: CH2_V_{REF} = 601.5mV (CH2_VOUT=1.0025V) 0x82: CH2_V_{REF} = 603.0mV (CH2_VOUT=1.005V) ... 0xFD: CH2_V_{REF} = 787.5mV (CH2_VOUT=1.3125V) 0xFE: CH2_V_{REF} = 789.0mV (CH2_VOUT=1.315V) 0xFF: CH2_V_{REF} = 790.5mV (CH2_VOUT=1.3175V)							

Register Name	CH2 Fault Flag Register							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x01							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	OVP2	UVP2	CL2	OTP
Read/Write	-	-	-	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
OVP2	CH2 Output Over Voltage Protection Flag.							
UVP2	CH2 Output Under Voltage Protection Flag.							
CL2	CH2 Current Limit Flag.							
OTP	Over Temperature Protection Flag.							

Note: The Fault Flag will be cleared when: 1.Clear fault function enable. 2. Both of EN pins are “L”.

Register Name	CH2 Soft Enable							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x03							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	-	Soft_EN2
Read/Write	-	-	-	-	-	-	-	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
EN2_soft	0: Normal Operation. (Default) 1: Standby Mode. (The CH2 output voltage down to 0V, but Internal Regulator and I²C Function still existing.) (If the SS1 and SS2 connect to the same capacitor, then the CH1 & CH2 I²C soft-Enable command can’t be used.)							

I²C Programming (Cont.)

Register Name	CH2 Transition Slew Rate							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x04							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	TSR2	
Read/Write	-	-	-	-	-	-	R/W	
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
TSR2	00: 0.75mV/us. (Default) 01: 1.5mV/us 10: 3mV/us 11: Reversed							

Register Name	CH2 Force PWM Mode							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x05							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	-	FPWM2
Read/Write	-	-	-	-	-	-	-	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
FPWM2	0: PSM/PWM mode automatic selection. (Default) 1: Force PWM Mode							

Register Name	Clear CH2 Fault Flag to Default							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x2F							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Clear_Flag2							
Read/Write	W							
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
Clear_Flag2	Write any data into the register to clear all CH2 Fault Flag to default value.							

Register Name	CH2 Soft Reset							
Affected Channel	CH2							
Slave Address	0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x3F							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST2							
Read/Write	W							
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
RST2	Write any data into the register to clear all CH2 Registers to default value.							

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I²C Programming (Cont.)

The CH2 I²C Registers Programming

Register Name	Frequency Setting Register							
Affected Channel	CH1 & CH2							
Slave Address	0x0A ~ 0x7A or 0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x02							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	FREQ_SET	
Read/Write	-	-	-	-	-	-	R/W	
Power On Default	0	0	0	0	0	0	0	1
Bit Name	Bit Definition							
FREQ_SET	00: 500kHz 01: 600kHz. (Default) 10: 800kHz 11: 1200kHz							

Register Name	Soft Reset All							
Affected Channel	CH1 & CH2							
Slave Address	0x0A ~ 0x7A or 0x0B ~ 0x7B (Configured by R_{ADDR1} and R_{ADDR2})							
Register Address	0x7F							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST_ALL							
Read/Write	W							
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
RST_ALL	Write any data into the register to clear all CH1, CH2 and Common Registers to default value.							

Function Descriptions

MainControl Loop

The IC uses current mode control to regulate the output voltage.
The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier.
The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage.
The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VCC Regulator

The IC provides an internal 5V VCC regulator for the internal control circuitry. The VCC regulator is powered by the VIN1 voltage. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation.

VCC Power-On Reset(POR)

VCC is an internal voltage regulator that is activated when the IC is powered by VIN1.
The APW7437 continuously monitors the voltage on the VCC pin. The soft start is activated when the VCC voltage and the EN voltage are above their respective POR thresholds.
VCC POR is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC POR also has hysteresis to resist ripple on the VCC voltage.

Enable/ShutdownControls

The IC provides two independent enable controls(EN1 and EN2) for the two converters(CH1 and CH2).
The on and off of CH1 and CH2 are controlled by EN1 and EN2, respectively. Drive ENx high to turn the respective converter on and drive ENx low to turn the respective converter off.

External frequency synchronization

Although the switching frequency of the IC is fixed at 600kHz, it can also change the switching frequency via the SYNC pin.
When an external clock is input to the SYNC pin, the IC can synchronize the switching frequency of the converter with the external clock frequency, which can be synchronized from 500 Hz to 2 MHz.

Single Frequency and Phase shift

The IC has two converters that use the same operating frequency to avoid beat frequencies and improve noise immunity.
But it also increases input current and EMI, so more input capacitors and additional EMI components must be used. Therefore, the IC provides a 180-degree phase shifting technique that allows two high-side power MOSFETs to be turned on at different times to eliminate these defects.
It will greatly reduce the RMS input current, resulting in less input capacitance, EMI components and input losses.

External Soft-Start(SS)

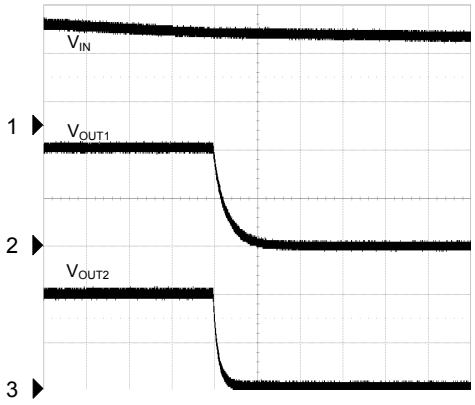
The IC has the soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.
The rise time of the output voltage (soft-start time) can be adjusted by a capacitor connected from the SS pin to ground. Each channel of the APW7437 has a separate SS pin and EN pin, when the EN1 and EN2 pins are connected together and the SS1 and SS2 pins are also connected together, it allows the two regulators to start together. The soft start time can be calculated by the fol- lowing formula:

$$T_{SS}(ms) = \frac{V_{REF}(V) \times C_{SS}(nF)}{I_{SS}(uA)}$$

Function Descriptions (Cont.)

Fast Discharge

When the EN signal goes low or the VCC voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered.
The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.
The following figure shows the Vout1 and Vout2 = 1V without load then shutdown, we can see the output can be fully discharged within 5ms.



CH1: V_{IN}, 2V/Div
CH2: V_{OUT1}, 500mV/Div
CH3: V_{OUT2}, 500mV/Div
Time: 5ms/Div

Current Limit and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When any output voltage drops below the UVP threshold, UVP is triggered and both converters enter hiccup mode. In hiccup mode, the converters will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the overcurrent condition is removed, the IC will exit the hiccup mode.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature.
The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Over-Voltage Protection (OVP)

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Power Good Indicator(PG)

The IC has an open-drain PG pin that indicates the output regulation state.
During soft start, PG goes high when both outputs reach 90% of their target value.
During normal operation, when either of the two outputs is not within the range of 85%to 125% of the target voltage, the POK signal will be pulled low immediately. When the output returns between 90% and 120% of the target value, the PG will remain high again.
Since PG is an open-drain pull-down device, it usually requires an external pull-up resistor; however, if the pin is not used, no resistor is necessary.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating.
The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.
To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to "Typical Application Circuits".
The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

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Application Information (Cont.)

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/PGND to capacitor less than 2mm respectively is recommended.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible.
3. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
4. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
5. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
6. For better heat dissipation, it is highly recommended to place a large ground plane under the thermal pad of all PCB layers and place as many vias as possible on the thermal pad from the top layer to the bottom layer.
7. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

Thermal Consideration

It highly recommends all customers to keep the maximum junction temperature under 125oC in continuous operation. The junction temperature can be calculated by following formula :

$T_J = T_A + P_D \times \theta_{JA}$

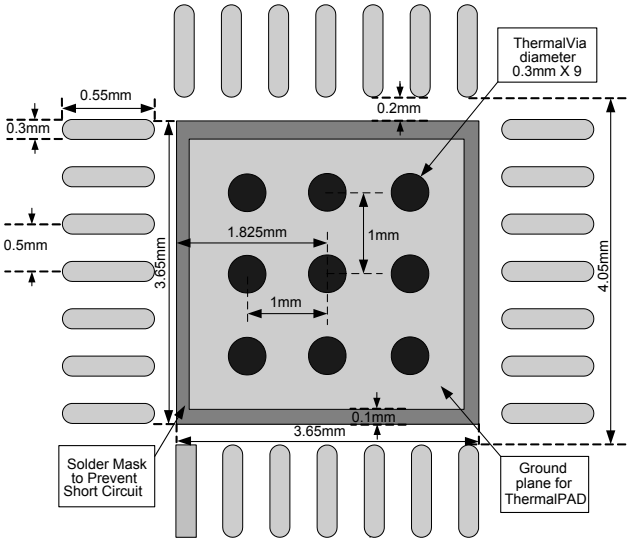
T_J : Junction temperature of APW7437
T_A : Operated ambient temperature
P_D: APW7437 power dissipation (not include inductors loss)
θ_{JA}: Junction to ambient thermal resistance

APW7437 is an optimized solution for thermal dissipation. By following the PCB layout recommendation provided in datasheet, customer can reach θ_{JA} to only 23.6°C/W. For a standard TQFN5*5 θ_{JA} is around 36°C/W.

For example:
Case 1:
θ_{JA} is 23.6°C/W, T_A is 50°C and maximum junction temperature <125°C,
The maximum power dissipation of APW7437 will be
$P_{D\,(MAX)}$ = (125°C - 50°C) / (23.6°C/W) = 3.18W

Case 2:
θ_{JA} is 36°C/W, T_A is 50°C and maximum junction temperature <125°C
The maximum power dissipation of APW7437 will be.
$P_{D\,(MAX)}$= (125°C - 50°C) / (36°C/W) = 2.08W

Recommended Minimum Footprint (Top View)

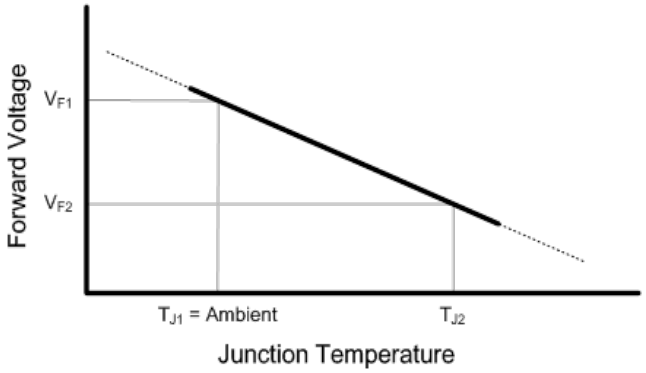


TQFN5X5-28 Land Pattern Recommendation

Application Information (Cont.)

Thermal Characteristics Measurement

Thermal characteristics table provides the thermal dissipation's ability of the device on the evaluation board following the layout consideration. The θ_{JA} is mainly dependent on the PCB layout design, the value followed the standard of JESD51 is hard to use to estimate the junction temperature in the real application.
Therefore, when testing on the Anpec's evaluation board, a method by measuring forward voltage (V_F) of diode is used to monitor junction temperature (T_J). As shown in the figure below, the relationship between T_J and V_F is nearly linear.



The relationship between TJ and VF can also be expressed equation as:

$T_J = m \times V_F + T_O$
Where
T_J = junction temperature in °C
m = slope in °C/Volt
V_F = forward voltage drop
T_J = intercept in °C

Therefore, with this equation, the junction temperature can be acquired by having the corresponding forward voltage drop V_F.
The method to know the relationship between T_J vs V_F is introducing below. First of all, puts the EVB in a chamber with still air, and connects the internal diode to the outside multi-meter. Normally, the body diode of Power Good FET can be used. Or if any pin pulls low or fixed a low voltage would not affect the normal application, their ESD diode can be used to measure the die temperature as well. Secondly, heat the ambient temperature to a specific point and record the corresponding V_F. Because thermal equilibrium is important for minimizing the error, make sure T_{case} and $T_{ambient}$ are very close. Forward voltage should be stable at that moment.

The results will be more accurate with more test data because the real curve of temperature sensitive parameter is not perfectly linear.
Once the relationship between T_J and V_F is known, it can be used to measure the actual junction temperature by knowing V_F with various conditions, such as different operating power, environment temperature, or packaging way.

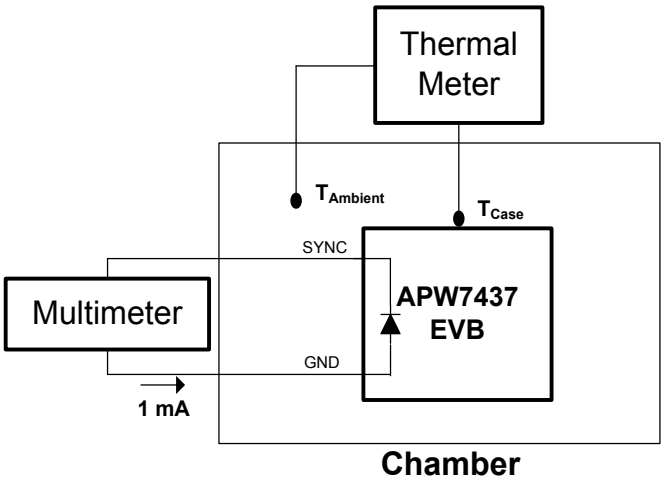
$\theta_{JA} = (T_J - T_A) / P_D$

With the actual junction temperature, the thermal resistance is easy to calculate by equation above. The device power dissipation is given by:

$P_D = (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT}) - (L_{AC\_LOSS} + L_{DC\_LOSS})$
L_{AC_LOSS} and L_{DC_LOSS} can be calculated from the inductor vendor's website.

Application Information (Cont.)

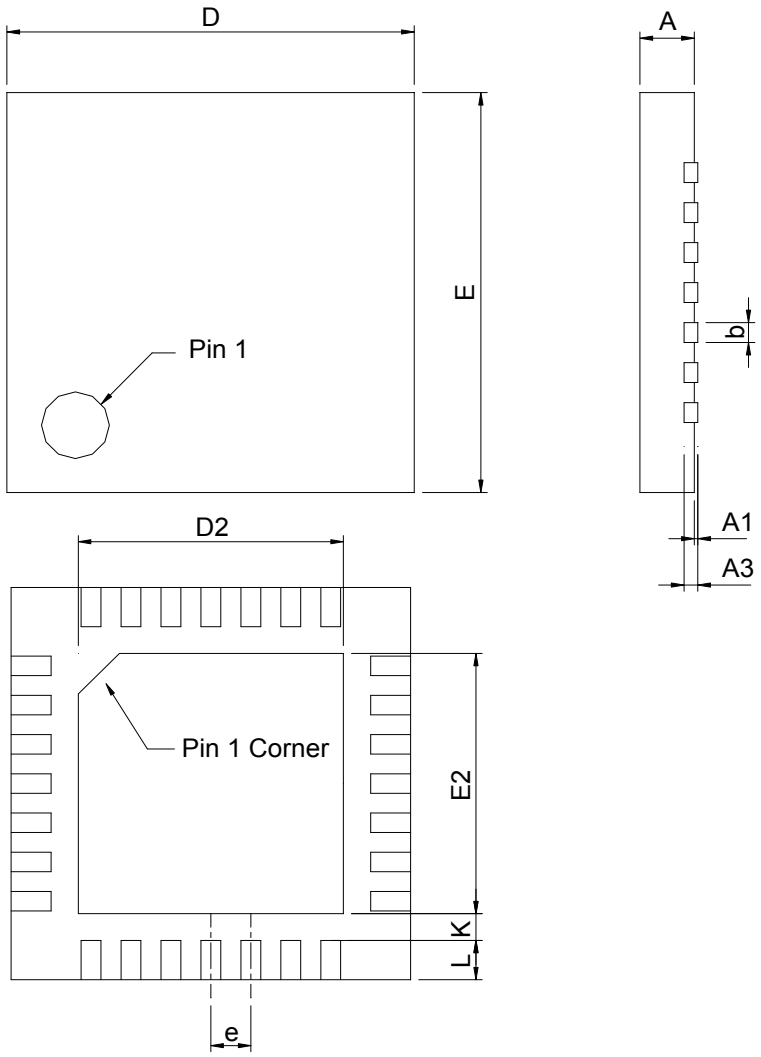
Setup for measuring forward voltage



For the APW7437 EVB, the ESD diode of the SYNC pin (from the GND pin to the SYNC) can be used to measure the die temperature. It will not affect normal application when pulling low to SYNC pin. The current provided from multimeter is 1mA, which is exactly the most suitable value that JEDEC suggests in JESD51-1. Test current 1mA is large enough to obtain a reliable forward voltage reading not influenced by surface leakage but small enough not to cause significant self heating.
The detail measurement result can refer "ANPEC Thermal Test Report".

Package Information

TQFN5x5-28



SYMBOL	TQFN5x5-28			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.90	5.10	0.193	0.201
D2	3.50	3.80	0.138	0.150
E	4.90	5.10	0.193	0.201
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WHHD-3.

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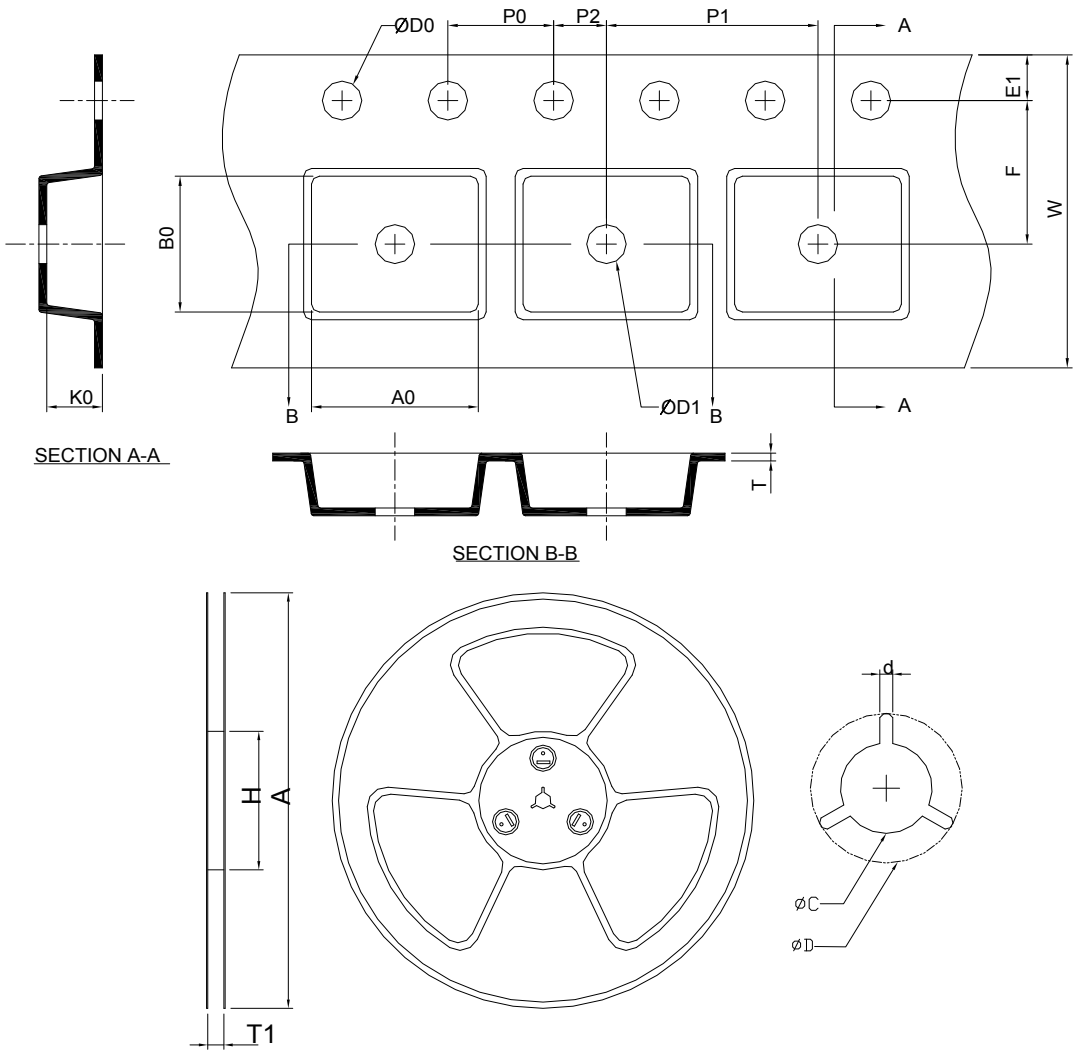
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN5x5-28	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.30±0.20

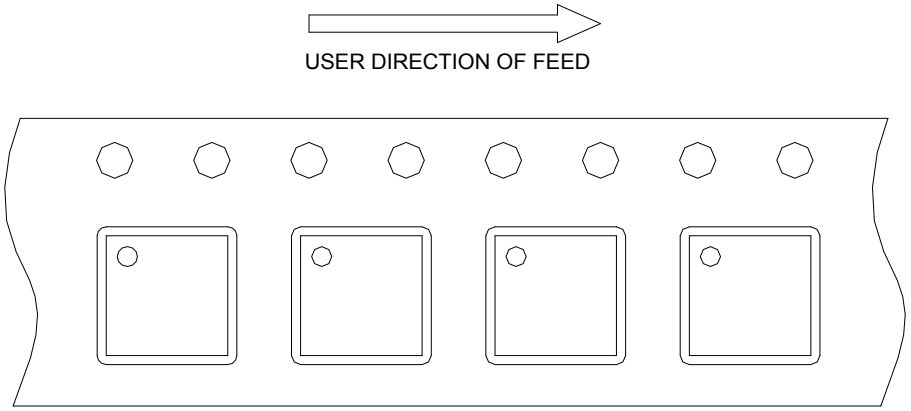
(mm)

Devices Per Unit

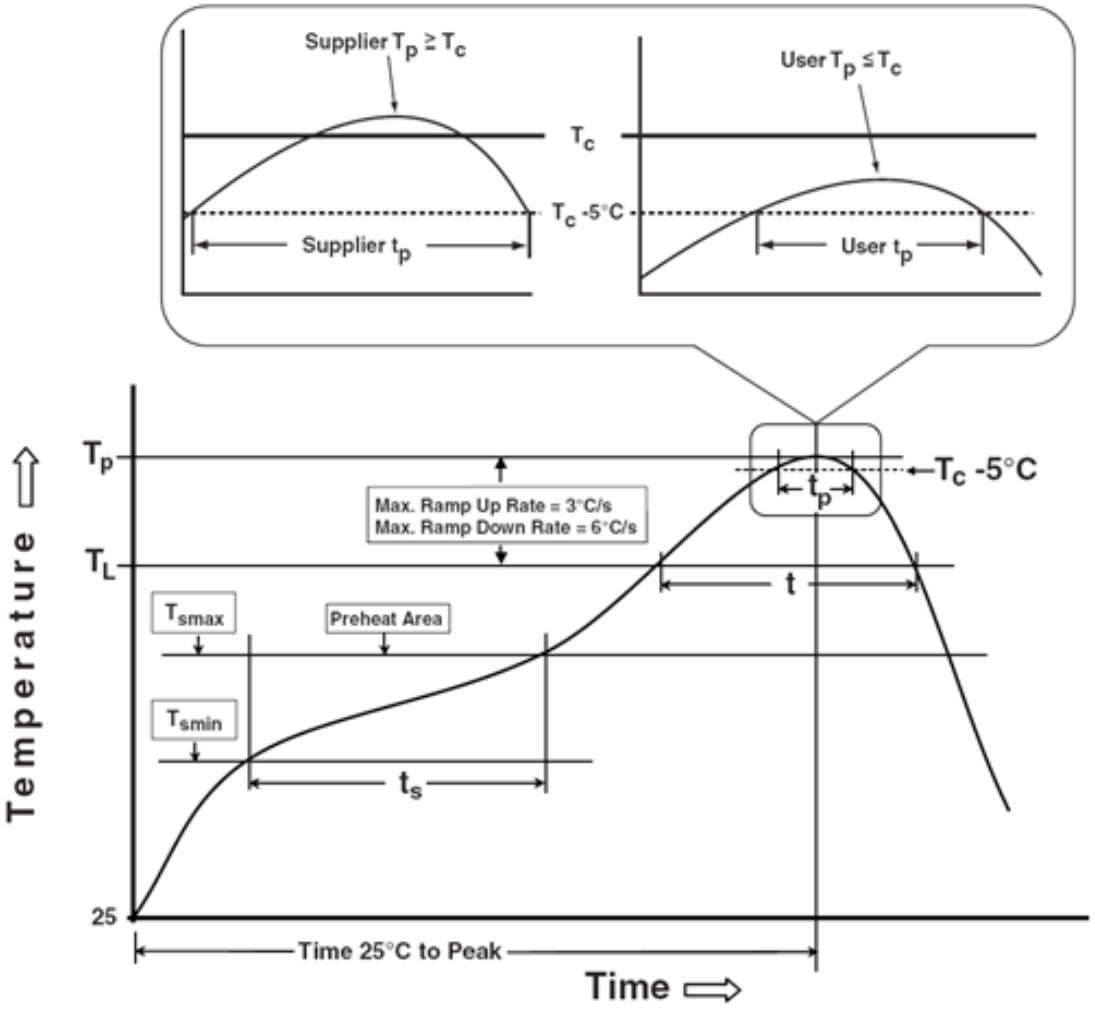
Application	Packing	Devices Per Reel
TQFN5x5-28	Tape & Reel	2500

Taping Direction Information

TQFN5x5-28



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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