5 Buck Converter+ 1 LDO PMU With Temperature Sensor

Features

- **Wide Input Operating Range: 2.7~5.5V**
- **I²C Interface**
- **Random and Sequential Read Mode**
- **Automatic Address Incrementing**
- **Regulators with Programmable DC Set Point and Soft-start**
- **Programmable Bucks and LDO and all Regulators with Auto Discharge Function and Reset**
- **±1% Feedback Voltage Accuracy**
- **Two Pins to Select Four Sets of DC Voltage**
- **Programmable VOUT, Power-up Sequence, Reset IC Delay Time and Enable**
- **Integrated Voltage Monitor with Digital Filters**
- **TQFN5x5-36 Package**
- **Lead Free Green Devices Available (RoHS Compliant)**

Applications

- **SSD**
- **Docking Station**

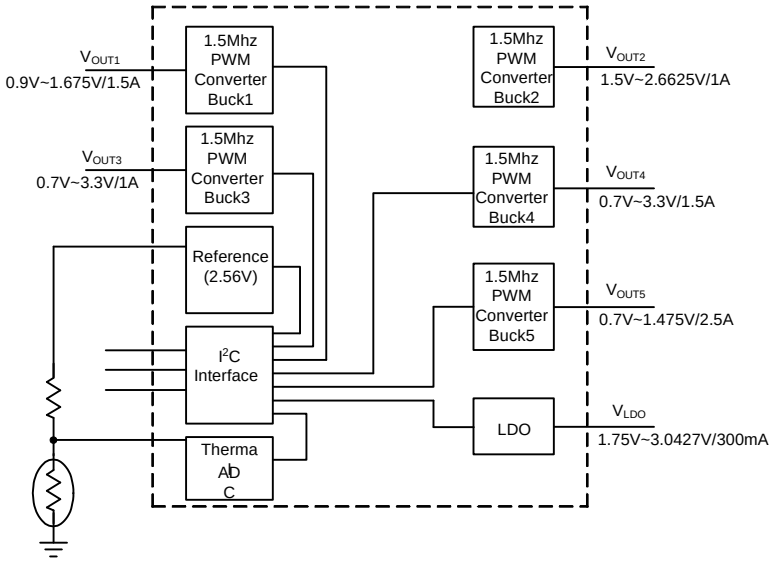
General Description

The AWP7705A/B/C/D is a PMU for SSD and Docking station application. It contains 5 buck converters, one LDO regulator and one temperature ADC. Each buck and LDO is independent with each other and the power on sequence can be programmed while their regulated voltages can be programmed too. All programming can be done via I2C interface. The ADC can get the external temperature information by TS pin and report the current temperature data to a register. The temperature/data conversion rate and the temperature high and low alert threshold can be adjusted via I2C bus.

All buck converters equip PWM/PFM mode. When in light load, the buck converter can enter PFM mode for boosting efficiency. When in PFM mode, the output ripple could slightly bigger than in PWM mode. If smaller output ripple is desired, the PFM mode can be disabled via I2C interface. Each buck converter operates in synchronous PWM mode in heavy load, the synchronous rectification MOSFET can be disabled via I²C.

The AWP7705A/B/C/D is available in TQFN5x5-36 package.

Simplified Application Circuit

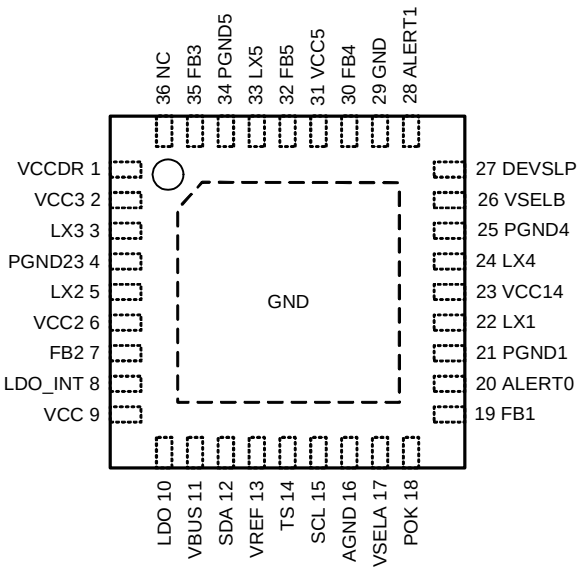


Ordering and Marking Information

APW7705 □□□□-□□□ Assembly Material Handling Code Temperature Range Package Code Configuration	Package Code QB: TQFN5x5-36 Operating Ambient Temperature Range I: -40 ~ 85°C Handling Code TR: Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7705□ QB : □:A/B/C/D APW7705□ XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN5x5-36
(Top View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VCC}	VCC, VCC14, VCC2, VCC3, VCCDR to GND Voltage	-0.3 ~ 7	V
V_{VBUS}	VBUS Supply Voltage (VBUS to GND)	-0.3 ~ 7	V
V_{LXX}	LX1, LX2, LX3, LX4, LX5 to GND Voltage	-0.3 ~ 7	V
V_{FBX}	FB1, FB2, FB3, FB4, FB5 to GND Voltage	-0.3 ~ 7	V
	SDA, SCL, POK, VSELA, VSELB	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	43	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5x5-36 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	VCC, VCC14, VCC2, VCC3, VCCDR to GND Voltage	2.7 ~ 5.5	V
V_{VBUS}	VBUS Supply Voltage (VBUS to GND)	1.72 ~ 3.63	V
T_A	Ambient Temperature	-40 ~ 85	°C
	Total Power Dissipation (Note 4)	0 ~ 2.2	W

Note 3: Refer to the typical application circuit.

Note 4: IC is mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5x5-36 is soldered directly on the PCB.

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
BIAS						
	Device Sleep Mode Quiescent Supply Current		-	80	-	μA
	Quiescent Supply Current	V_{OUT}=all output range , While in PFM Mode	-	-	1	mA
	LDO_INT Output Voltage	C_{OUT}=1μF, I_{LOAD}=0mA	-	1.8	-	V
	VREF Output Voltage	C_{OUT}=1μF, I_{LOAD}=0mA	-	2.56	-	V
	VREF Output Current		5	-	-	mA
TEMPERTURE SENSOR						
	Temperature Resolution	Monotonicity guaranteed	8	-	-	Bits
	LSB		-	1	-	°C
	Conversion Time		-	19	-	μs
	Conversion Rate		-	250	-	CONV/μs
VOLTAGE MONITOR AND POR GENERATOR						
	VCC Undervoltage Rising Threshold	VCC14, VCC2, VCC3 or VCC5 rising, enable	2.775	2.8	2.825	V
	VCC Undervoltage Falling Threshold	VCC14, VCC2, VCC3 or VCC5 falling, POK signal only.	2.675	2.7	2.725	V
	VCC Undervoltage Threshold Hysteresis		0.09	0.1	0.11	V
	Regulators Disable	VCC14, VCC2, VCC3 or VCC5 falling	2.475	2.5	2.525	V
	Delay1 POK Rising Delay	2ms step programmability	8	-	24	ms
	POK Low Level Output Voltage	I_{OL}=1mA	-	-	0.3	V
	POK Pull-up Resistance	Internal pull-up to VBUS	140	200	260	KΩ
	POK High Level Output Voltage		80% VBUS	-	-	V
BUCK1 SWITCHING REGULTOR						
	Input Voltage Range		2.7	-	5.5	V
	Consumption Current	No load, PFM mode	-	50	-	μA
	Output DC Voltage Range	Steady State, I_{LOAD}<1A	0.9	-	1.675	V
	Output Voltage Step Size	Single Step Change	-	25	-	mV
	Maximum Output Current	Internal FET, steady state	1.5	-	-	A
	Current Limit Threshold	Integrated FET current	2.2	2.5	-	A
	PFM Peak Current		-	0.7	-	A

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
BUCK1 SWITCHING REGULTOR						
	DC Line Regulation	3.3V<V_{VCC14}<5V, I_{OUT}=1A	-	0.4	-	%/V
	DC Load Regulation	While in PWM	-	0.3	-	%/A
	Switching Frequency		-	1.5	-	MHz
	Output Voltage Accuracy	While in PWM	-2	-	2	%
	Transient Response	V_{OUT}=1.5V Load Current = 0.1A to 1A	-	±5	-	%
	Soft-start Time		-	340	-	µs
	Integrated High-side P-FET On-resistance	V_{VCC14}=3.6V	-	130	-	mΩ
	Integrated Low-side N-FET On-resistance	V_{VCC14}=3.6V	-	65	-	mΩ
	Efficiency (NOTE5)	V_{OUT}=1.5V, I_{LOAD}=1A	-	80	-	%
	Discharge Resistor		-	100	-	Ω
	FB Input Impedance		-	0.2	-	MΩ
	Input Capacitor		-	4.7	-	µF
	Output Filter Capacitor		-	22	-	µF
	Output Filter Capacitor ESR		-	-	20	mΩ
	Output Filter Inductance		-	1	-	µH
	Under Voltage Protection		-	70	-	%
BUCK2 SWITCHING REGULTOR						
	Input Voltage Range		2.7	-	5.5	V
	Consumption Current	No load, PFM mode	-	50	-	µA
	Output DC Voltage Range	Steady State, I_{LOAD}<1A	1.5	-	2.664	V
	Output Voltage Step Size	Single Step Change	-	37.5	-	mV
	Maximum Output Current	Internal FET, steady state	1	-	-	A
	Current Limit Threshold	Integrated FET current	2.2	2.5	-	A
	PFM Peak Current		-	0.7	-	A
	DC Line Regulation	3.3V<V_{VCC2}<5V, I_{OUT}=1A	-	0.4	-	%/V
	DC Load Regulation	While in PWM	-	0.3	-	%/A
	Switching Frequency		-	1.5	-	MHz
	Output Voltage Accuracy	While in PWM	-2	-	2	%
	Transient Response	V_{OUT}=1.8V Load current = 0.1A to 1A	-	±5	-	%
	Soft-start Time	V_{OUT}=1.8V, 0 to 90% of V_{OUT}	-	270	-	µs

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
BUCK2 SWITCHING REGULTOR						
	Integrated High-side P-FET On-resistance	V_{VCC2}=3.6V	-	210	-	mΩ
	Integrated Low-side N-FET On-resistance	V_{VCC2}=3.6V	-	105	-	mΩ
	Efficiency (NOTE6)	V_{OUT}=1.8V, I_{LOAD}=1A	-	80	-	%
	Discharge Resistor		-	100	-	Ω
	FB Input Impedance		-	0.2	-	MΩ
	Input Capacitor		-	4.7	-	µF
	Output Filter Capacitor		-	22	-	µF
	Output Filter Capacitor ESR		-	-	20	mΩ
	Output Filter Inductance		-	1	-	µH
	Under Voltage Protection		-	70	-	%
BUCK3 SWITCHING REGULTOR						
	Input Voltage Range		2.7	-	5.5	V
	Consumption Current	No load, PFM mode	-	50	-	µA
	Output DC Voltage Range	Steady State, I_{LOAD}<0.5A	0.7	-	3.3	V
	Output Voltage Step Size	Single Step Change	-	25	-	mV
	Maximum Output Current	Internal FET, steady state	1	-	-	A
	Current Limit Threshold	Integrated FET current	2.2	2.5	-	A
	PFM Peak Current		-	0.7	-	A
	DC Line Regulation	3.3V<V_{VCC3}<5V, I_{OUT}=1A	-	0.4	-	%/V
	DC Load Regulation	While in PWM	-	0.3	-	%/A
	Switching Frequency		-	1.5	-	MHz
	Output Voltage Accuracy	While in PWM	-2	-	2	%
	Transient Response	V_{OUT}=1V, Load current from 0.1A to 1A		±5		%
	Soft-start Time	V_{OUT}=1V, 0 to 90% of V_{OUT}	-	340	-	µs
	Integrated High-side P-FET On-resistance	V_{VCC3}=3.6V	-	210	-	mΩ
	Integrated Low-side N-FET On-resistance	V_{VCC3}=3.6V	-	105	-	mΩ
	Efficiency (NOTE7)	V_{OUT}=1V, I_{LOAD}=1A	-	80	-	%
	Discharge Resistor		-	100	-	Ω
	FB Input Impedance		-	0.2	-	MΩ
	Input Capacitor		-	4.7	-	µF

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
BUCK3 SWITCHING REGULTOR						
	Output Filter Capacitor		-	22	-	µF
	Output Filter Capacitor ESR		-	-	20	mΩ
	Output Filter Inductance		-	1	-	µH
	Under Voltage Protection		-	70	-	%
BUCK4 SWITCHING REGULTOR						
	Input Voltage Range		2.7	-	5.5	V
	Consumption Current	No load, PFM mode	-	50	-	µA
	Output DC Voltage Range	Steady State, I_{LOAD}<1A	0.7	-	3.3	V
	Output Voltage Step Size	Single Step Change	-	25	--	mV
	Maximum Output Current	Internal FET, steady state	1.5	-	-	A
	Current Limit Threshold	Integrated FET current	2.7	3	-	A
	PFM Peak Current		-	0.7	-	A
	DC Line Regulation	3.3V<V_{VCC14}<5V, I_{OUT}=1A	-	0.4	-	%/V
	DC Load Regulation	While in PWM	-	0.3	-	%/A
	Switching Frequency		-	1.5	-	MHz
	Output Voltage Accuracy	While in PWM	-2	-	2	%
	Transient Response	V_{OUT}=1V, Load current = 0.1A to 1.5A	-	±5	-	%
	Soft-start Time	V_{OUT}=1V, 0 to 90% of V_{OUT}	-	470	-	µs
	Integrated High-side P-FET On-resistance	V_{VCC14}=3.6V	-	130	-	mΩ
	Integrated Low-side N-FET On-resistance	V_{VCC14}=3.6V	-	65	-	mΩ
	Efficiency (NOTE8)	V_{OUT}=1V, I_{LOAD}=1A	-	80	-	%
	Discharge Resistor		-	100	-	Ω
	FB Input Impedance		-	0.2	-	MΩ
	Input Capacitor		-	4.7	-	µF
	Output Filter Capacitor		-	22	-	µF
	Output Filter Capacitor ESR		-	-	20	mΩ
	Output Filter Inductance		-	1	-	µH
	Under Voltage Protection		-	70	-	%

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
BUCK5 SWITCHING REGULTOR						
	Input Voltage Range		2.7	-	5.5	V
	Consumption Current	No load, PFM mode	-	50	-	μA
	Output DC Voltage Range	Steady State, I_{LOAD}<1.6A	0.7	-	1.475	V
	Output Voltage Step Size	Single Step Change	-	25	-	mV
	Maximum Output Current	Internal FET, steady state	2.5	-	-	A
	Current Limit Threshold	Integrated FET current	3.7	4	-	A
	PFM Peak Current		-	0.7	-	A
	DC Line Regulation	3.3V<V_{VCC5}<5.5V, I_{OUT}=1A	-	0.4	-	%/V
	DC Load Regulation	While in PWM	-	0.3	-	%/A
	Switching Frequency		-	1.5	-	MHz
	Output Voltage Accuracy	While in PWM	-2	-	2	%
	Transient Response	V_{OUT}=1V, Load current = 0.1 to 2.5A	-	±5	-	%
	Soft-start Time	V_{OUT}=1V, 0 to 90% of V_{OUT},	-	390	-	μs
	Integrated High-side P-FET On-resistance	V_{VCC5}=3.6V	-	100	-	mΩ
	Integrated Low-side N-FET On-resistance	V_{VCC5}=3.6V	-	65	-	mΩ
	Efficiency (NOTE9)	V_{OUT}=1V, I_{LOAD}=1A	-	80	-	%
	Discharge Resistor		-	100	-	Ω
	FB Input Impedance		-	0.2	-	MΩ
	Input Capacitor		-	4.7	-	μF
	Output Filter Capacitor		-	44	-	μF
	Output Filter Capacitor ESR		-	-	20	mΩ
	Output Filter Inductance		-	1	-	μH
	Under Voltage Protection		-	70	-	%

Note 4: Guaranteed by design, not production tested.

Electrical Characteristics

Unless otherwise specified, these specifications apply over T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7705			Unit
			Min	Typ	Max	
LDO						
	Input Voltage Range		2.7	-	5.5	V
	Output Voltage Range		1.05	-	3.043	V
	Voltage Setting Step Size		-	41.7	-	mV
	Output Voltage Accuracy	V_{OUT}=all output range, I_{OUT}=1mA	-2	-	2	%
	Output Current		-	-	300	mA
	Limit Current		350	770	-	mA
	Dropout Voltage	V_{OUT} Setting= V_{IN}, I_{OUT}=300mA	-	0.3	0.7	V
	Line Regulation	3.3V<V_{IN}<5.5V, I_{OUT}=0.1mA	-	1	-	mV
	Load Regulation	1mA<I_{OUT}<300mA	-	1.5	30	mV
	Transient Response	I_{OUT}=1mA→150mA→1mA	-	50	-	mV
	Ripple Rejection	F=10kHz, C_{OUT}=4.7µF, I_{OUT}=20mA	-	65	-	DB
	Output Noise	BW=10Hz ~ 100kHz	-	100	-	µVrms
	Supply Current	I_{OUT}=0mA	-	50	-	µV
	Soft-start Time	C_{OUT}=4.7µF, I_{OUT}=250mA	-	50	-	µs
	Discharge Resistor		-	100	-	Ω
	Input Capacitor		-	4.7	-	µF
	Output Capacitor		-	4.7	-	µF
	Under Voltage Protection		-	70	-	%
OVER TEMPERATURE PROTECTION						
T_{OTP}	Over-temperature Protection Threshold (Re-soft start after OTP)		-	160	-	°C
	Over-temperature Hysteresis		-	30	-	°C

Note 5: Efficiency is measured between VCC14 and BUCK1 V_{OUT} while BUCK4 is off.

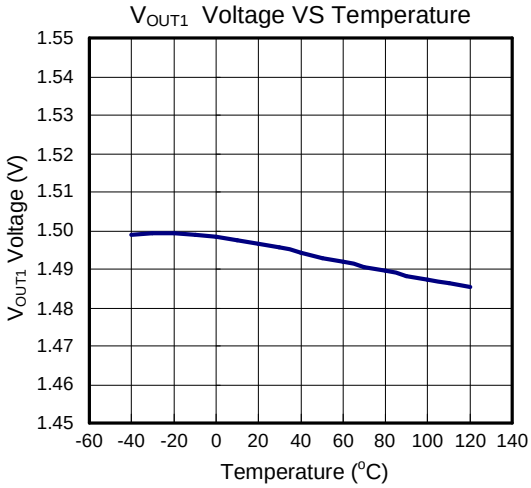
Note 6: Efficiency is measured between VCC2 and BUCK2 V_{OUT}.

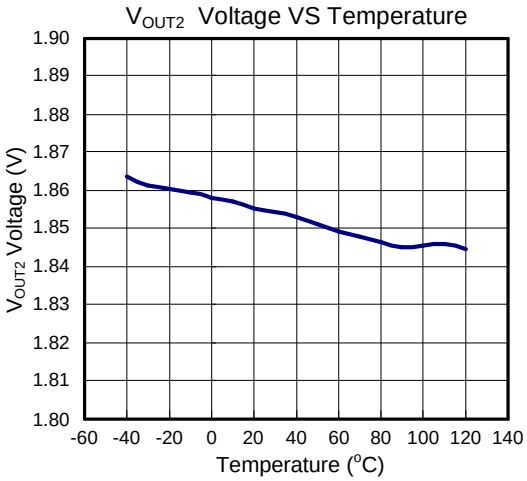
Note 7: Efficiency is measured between VCC3 and BUCK3 V_{OUT}.

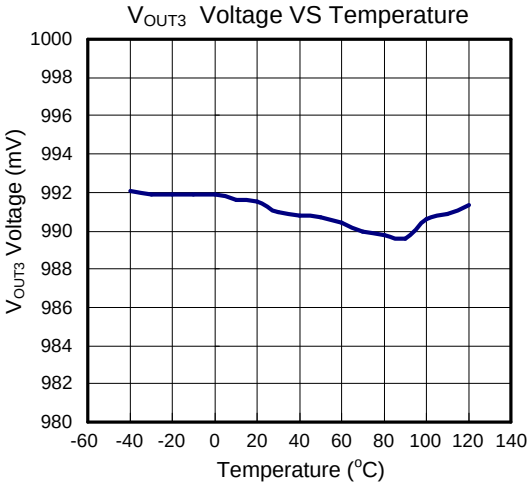
Note 8: Efficiency is measured between VCC14 and BUCK4 V_{OUT} while BUCK1 is off.

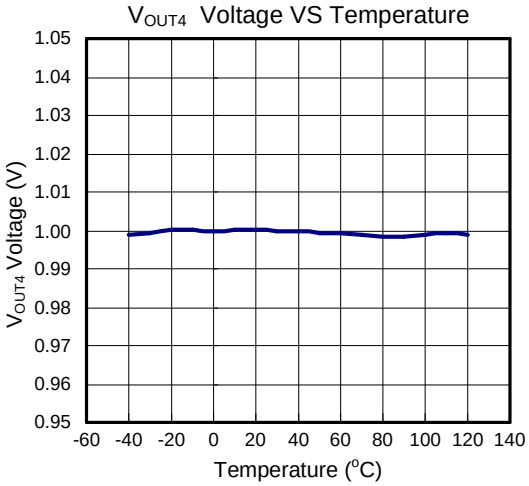
Note 9: Efficiency is measured between VCC5 and BUCK5 V_{OUT}.

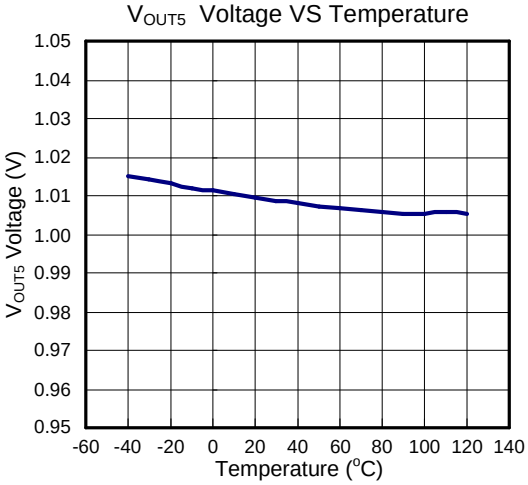
Typical Operating Characteristics

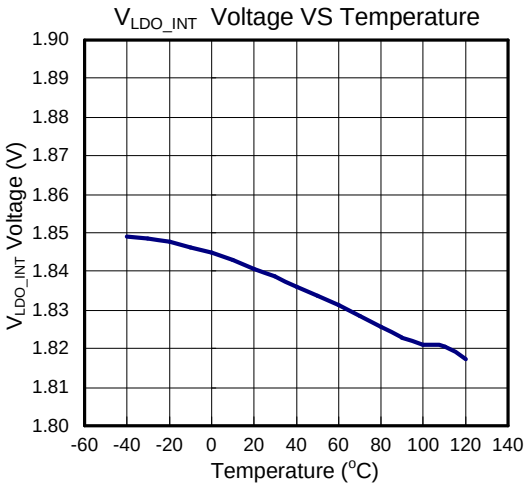




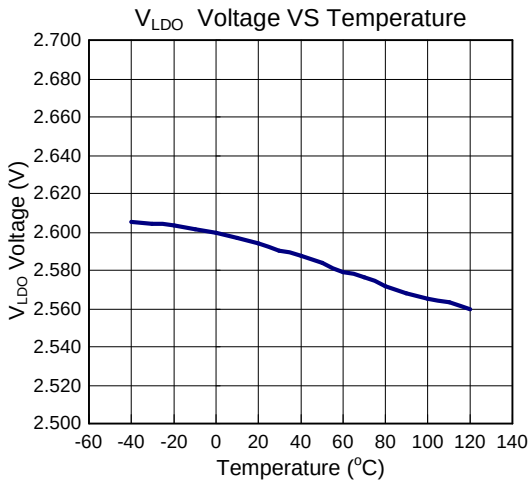


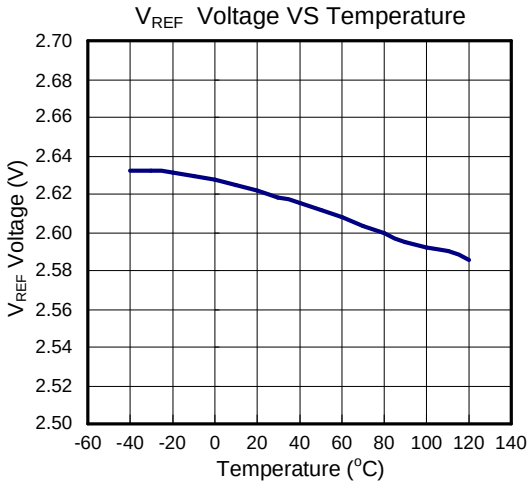






Typical Operating Characteristics (Cont.)

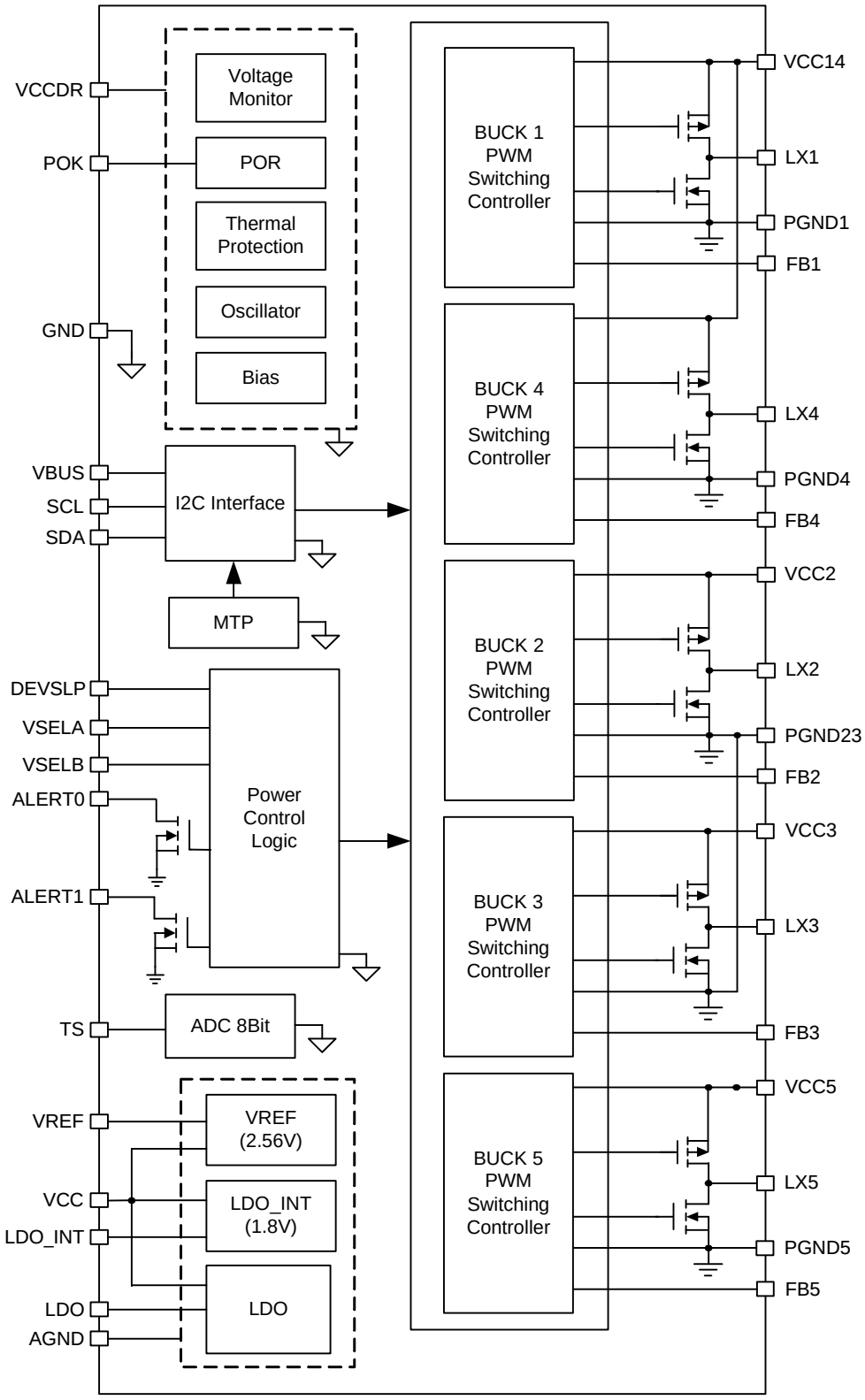




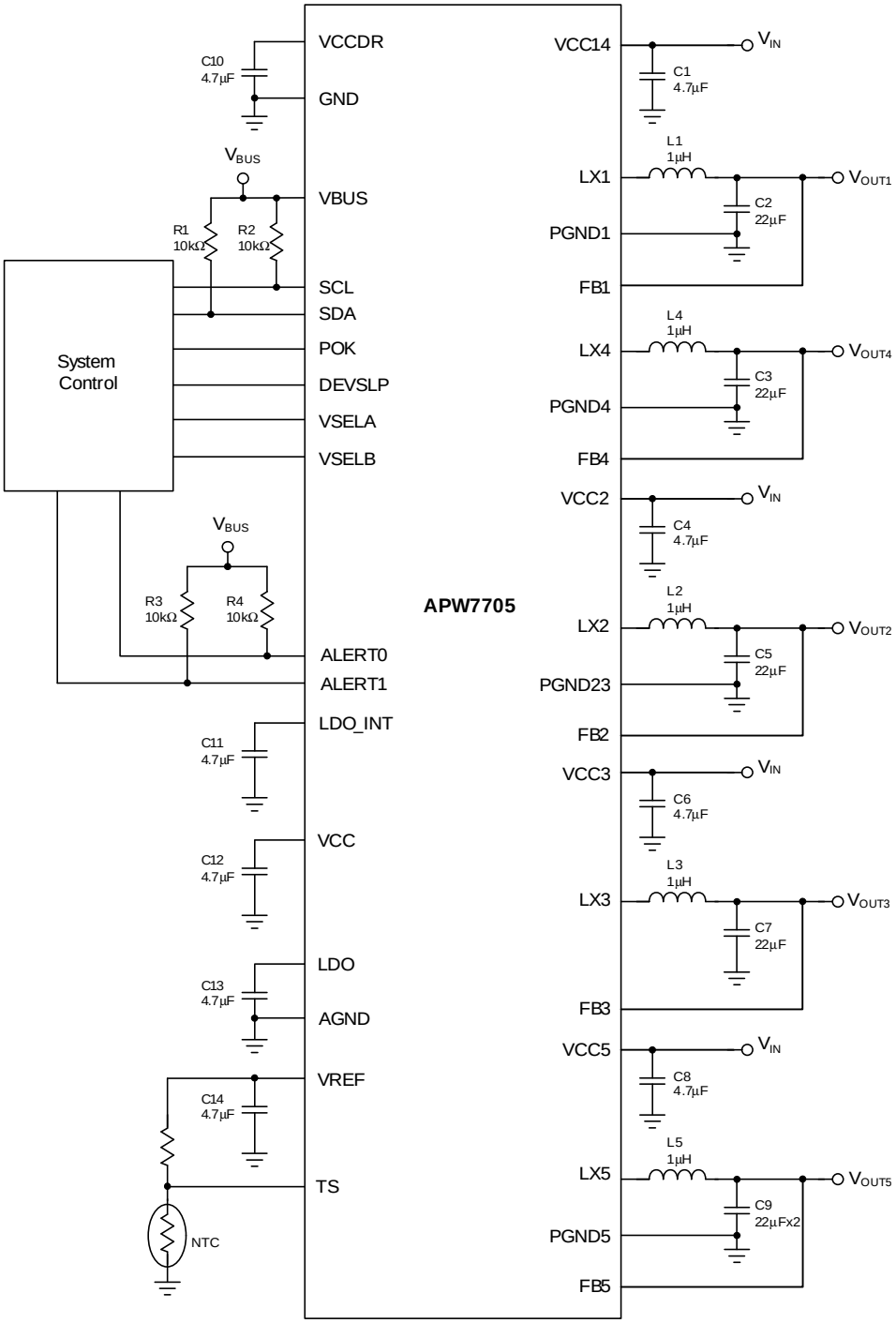
Pin Description

PIN		Function
NO.	NAME	
1	VCCDR	Power supply
2	VCC3	Power supply
3	LX3	Buck3 regulator switching node
4	PGND23	Buck2 and Buck3 ground
5	LX2	Buck2 regulator switching node
6	VCC2	Buck2 power supply
7	FB2	Buck2 regulator feedback
8	LDO_INT	1.8V LDO Output
9	VCC	Power supply
10	LDO	LDO output
11	VBUS	I2C interface power supply
12	SDA	I2C bus data line
13	VREF	Reference voltage for temperature sensor
14	TS	ADC input for temperature sensor
15	SCL	I2C bus clock line
16	AGND	Analog ground
17	VSELA	With VSELB, set A, B, C and D selection
18	POK	Power on reset output
19	FB1	Buck1 regulator feedback
20	ALERT0	Alert output 0, open drain
21	PGND1	Buck1 ground
22	LX1	Buck1 regulator switching node
23	VCC14	Buck and Buck4 power supply
24	LX4	Buck4 regulator switching node
25	PGND4	Buck4 ground
26	VSELB	With VSELA, set A, B, C and D selection
27	DEVSLP	Digital signal input for entering device sleep mode
28	ALERT1	Alert output 1, open drain
29	GND	Digital ground
30	FB4	Buck4 regulator feedback
31	VCC5	Buck5 power supply
32	FB5	Buck5 regulator feedback
33	LX5	Buck5 regulator switching node
34	PGND5	Buck5 ground
35	FB3	Buck3 regulator feedback
36	NC	Not connected internally

Block Diagram



Typical Application Circuit



Function Description

Main Control Loop

The APW7705A/B/C/D is a single chip power supplies designed to for SSD and Docking station applications. Five high efficiency DC/DC buck converters and one LDO regulator generate 0.7V~3.3V rails, programmable via I2C interface, which can support up to 1A~2.5A of output current in each buck converter and 300mA of output current in LDO regulator. The power on sequence of all rails is adjustable through the I^2C interface to accommodate specific SSD requirements.

Under-Voltage Lockout

An under-voltage lockout function prevents the device from operating if the input voltage on VCC14, VCC2, VCC3 or VCC5 is lower than approximately 2.5V. The device automatically shuts down all buck converters and LDO regulator if the voltage on the relative VCC drops below approximately 2.5V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Soft-Start

The APW7705A/B/C/D has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage until the ramp voltage reaches the reference voltage. Then the voltage on FBx regulated at reference voltage.

Power Good Indicator

POK is actively held low in shutdown and soft-start status. The POK is an open-drain with internal 200KΩ pull high. When the soft-start is finished, the POK is released. In normal operation, the POK will go low when any one of output voltage drops below 85% of the converter reference voltage or when VCC14, VCC2, VCC3 or VCC5 is lower than 2.7V typically. During normal power on sequence, the POK signal will become high after internal delay which is programmable via I^2C bus.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7705A/B/C/D. When the junction temperature exceeds 160°C, a thermal sensor turns off the all power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP designed with a 30°C hysteresis lowers the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the life time of the device.

Temperature Sensor

The APW7705A/B/C/D allows the user to take full control of the temperature sensing circuit at the expense of additional I^2C read/writes and associated software over-head in the main processor. It is designed for use with host processors that can read and write to multiple registers using standard I^2C protocol.

Current-Limit Protection

The APW7705A/B/C/D monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and over-voltage conditions.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (70% of normal output voltage), APW7705A/B/C/D shuts down the output gradually and latches off both high and low side MOSFETs. The VOUT1, VOUT2, VOUT3, VOUT4, VOUT5 or LDO is happened to UVP then IC was latched off and POK will be go low.

Function Description (Cont.)

Register setting for I²C

REG 00: LDOVL Register

The address 00 bit [7] is setting LDO output voltage level selection enable. When the address bit [7] =0 that's LDO output voltage by VSELA and VSELB. However the LDOVL [5:0] is disabled. On the contrary; the address 00 bit [7] was setting =1 then LDO output voltage was by LDOVL [5:0] setting. See the table 1.

Table 1: LDOVLEN setting register

Address	Bit	Name	Description	R/W	Note
00h	7	LDOVL	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by LDOVL [5:0]	R/W	

The address 00 bit [5:0] is setting LDO output voltage. Adjustment output voltage range is from 1.75V to 3.5014V. See the REG00 LDOVL Register of Register Map.

REG 01: PSR1VL Register

The address 01 bit [7] is setting BUCK1 output voltage level selection enable. When the address bit [7] =0 that's BUCK1 output voltage by VSELA and VSELB. However the PSR1VL [5:0] is disabled. On the contrary; the address 01 bit [7] was setting =1 then BUCK1 output voltage was by PSR1VL [5:0] setting. See the table 2.

Table 2: PSR1VLEN setting register

Address	Bit	Name	Description	R/W	Note
01h	7	PSR1VLEN	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by PSR1VL [5:0]	R/W	

The address 01 bit [6] is setting BUCK1 over current function. When the bit [6] =0 then over current is enable, On the contrary; the bit [6] was setting 1 then BUCK1 over current is disable. But, In BUCK1 over current was disabling and loading is adjustment very heavy, this condition can be caused IC damage. See the table 3.

Table 3:PSR1OCDIS setting register

Address	Bit	Name	Description	R/W	Note
01h	6	PSR1OCDIS	0:BUCK1 over current is enable 1:BUCK1 over current is disable	R/W	

The address 01 bit [5:0] is setting BUCK1 output voltage. Adjustment output voltage range is from 0.9V to 2.475V. See the REG01 PSR1VL Register of Register Map.

Function Description (Cont.)

REG 02: PSR3VL Register

The address 02 bit [7] is setting BUCK3 output voltage level selection enable. When the address bit [7] =0 that's BUCK3 output voltage by VSELA and VSELB. However the PSR3VL [5:0] is disabled. On the contrary; the address 02 bit [7] was setting =1 then BUCK3 output voltage was by PSR3VL [5:0] setting. See the table 4.

Table 4: PSR3VLEN setting register

Address	Bit	Name	Description	R/W	Note
02h	7	PSR3VLEN	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by PSR1VL [5:0]	R/W	

The address 02 bit [6] is setting BUCK3 over current function. When the bit [6] =0 then over current is enable, On the contrary; the bit [6] was setting 1 then BUCK3 over current is disable. But, In BUCK3 over current was disabling and loading is adjustment very heavy, this condition can be caused IC damage. See the table 5.

Table 5:PSR3OCDIS setting register

Address	Bit	Name	Description	R/W	Note
02h	6	PSR3OCDIS	0:BUCK3 over current is enable 1:BUCK3 over current is disable	R/W	

The address 02 bit [5:0] is setting BUCK3 output voltage. Adjustment output voltage range is from 0.7V to 3.3V. See the REG02 PSR3VL Register of Register Map.

REG 03: PSR2VL Register

The address 03 bit [7] is setting BUCK2 output voltage level selection enable. When the address bit [7] =0 that's BUCK2 output voltage by VSELA and VSELB. However the PSR2VL [4:0] is disabled. On the contrary; the address 02 bit [7] was setting =1 then BUCK2 output voltage was by PSR2VL [4:0] setting. See the table 6.

Table 6: PSR2VLEN setting register

Address	Bit	Name	Description	R/W	Note
03h	7	PSR2VLEN	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by PSR1VL [4:0]	R/W	

The address 03 bit [6] is setting BUCK2 over current function. When the bit [6] =0 then over current is enable, On the contrary; the bit [6] was setting 1 then BUCK2 over current is disable. But, In BUCK2 over current was disabling and loading is adjustment very heavy, this condition can be caused IC damage. See the table 7.

Table 7:PSR2OCDIS setting register

Address	Bit	Name	Description	R/W	Note
03h	6	PSR2OCDIS	0:BUCK2 over current is enable 1:BUCK2 over current is disable	R/W	

The address 03 bit [4:0] is setting BUCK2 output voltage. Adjustment output voltage range is from 1.5V to 2.6625V. See the REG03 PSR2VL Register of Register Map.

Function Description (Cont.)

REG 04: PSR4VL Register

The address 04 bit [7] is setting BUCK4 output voltage level selection enable. When the address bit [7] =0 that's BUCK4 output voltage by VSELA and VSELB. However the PSR4VL [5:0] is disabled. On the contrary; the address 04 bit [7] was setting =1 then BUCK4 output voltage was by PSR4VL [5:0] setting. See the table 8.

Table 8: PSR4VLEN setting register

Address	Bit	Name	Description	R/W	Note
04h	7	PSR4VLEN	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by PSR1VL [5:0]	R/W	

The address 04 bit [6] is setting BUCK4 over current function. When the bit [6] =0 then over current is enable, On the contrary; the bit [6] was setting 1 then BUCK4 over current is disable. But, In BUCK4 over current was disabling and loading is adjustment very heavy, this condition can be caused IC damage. See the table 9.

Table 9:PSR4OCDIS setting register

Address	Bit	Name	Description	R/W	Note
04h	6	PSR4OCDIS	0:BUCK4 over current is enable 1:BUCK4 over current is disable	R/W	

The address 04 bit [5:0] is setting BUCK4 output voltage. Adjustment output voltage range is from 0.7V to 3.3V. See the REG04 PSR4VL Register of Register Map.

REG 05: PSR5VL Register

The address 05 bit [7] is setting BUCK5 output voltage level selection enable. When the address bit [7] =0 that's BUCK5 output voltage by VSELA and VSELB. However the PSR5VL [5:0] is disabled. On the contrary; the address 05 bit [7] was setting =1 then BUCK5 output voltage was by PSR5VL [4:0] setting. See the table 10.

Table 10: PSR5VLEN setting register

Address	Bit	Name	Description	R/W	Note
05h	7	PSR5VLEN	0:Output voltage setting is by VSELA , VSELB 1:Output voltage setting is by PSR1VL [4:0]	R/W	

The address 05 bit [6] is setting BUCK5 over current function. When the bit [6] =0 then over current is enable, On the contrary; the bit [6] was setting 1 then BUCK5 over current is disable. But, In BUCK5 over current was disabling and loading is adjustment very heavy, this condition can be caused IC damage. See the table 11.

Table 11:PSR5OCDIS setting register

Address	Bit	Name	Description	R/W	Note
05h	6	PSR5OCDIS	0:BUCK5 over current is enable 1:BUCK5 over current is disable	R/W	

The address 05 bit [4:0] is setting BUCK5 output voltage. Adjustment output voltage range is from 0.7V to 1.475V. See the REG05 PSR5VL Register of Register Map.

Function Description (Cont.)

REG 06: LDOCFG Register

The address 06 bits [6:4] are setting LDO power on sequence. It's can adjustment LDO and BUCK1 to BUCK5 the order in power on sequence. See the table 12.

Table 12: LDOORDER [2:0] setting register

Address	Bit	Name	Description	R/W	Note
06h	[2:0]	LDOORDER	000:LDO is first power on … 101:LDO is sixth power on 111:LDO is sixth power on	R/W	

The address 06 bit [1] is setting LDO Fault Deglitch Time. See the table 13. The function is avoiding fast noise when LDO output has any irregularity.

Table 13: DEGL setting register

Address	Bit	Name	Description	R/W	Note
06h	1	DEGL	0: 10us 1: 5us	R/W	

The address 06 bit [0] is setting LDO UVM function. See the table 14. When LDO has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when LDO has happened under voltage then IC is not happened shutdown.

Table 14: UVM setting register

Address	Bit	Name	Description	R/W	Note
06h	0	UVM	0: LDO under voltage generates fault. 1: LDO under voltage does not generate fault.	R	

Function Description (Cont.)

REG 07: PSR1CFG Register

The address 07 bit [7] is setting BUCK1 regulator PFM/PWM mode. See the table 15. When address bit [7] is setting=0 then BUCK1 was PFM mode. On the contrary; that bit is setting = 1 then BUCK1 was PWM mode

Table 15: PFMDIS setting register

Address	Bit	Name	Description	R/W	Note
07h	7	PFMDIS	0: BUCK1 is PFM mode 1: BUCK1 is PWM mode	R/W	

The address 07 bits [6:4] are setting BUCK1 order in power on sequence. See the table 16. That's adjustment BUCK1 order in power on sequence from first to sixth to be powered on.

Table 16: PFR1OREDER setting register

Address	Bit	Name	Description	R/W	Note
07h	[6:4]	PSR1ORDER	000:BUCK1 is first power on … 101:BUCK1 is sixth power on 111:BUCK1 is sixth power on	R/W	

The bits [1:0] are setting driver slew rate. See the table 17. That's adjustment driver rising slew rate from 500V/us to 2000V/us.

Table 17: RSLEW setting register

Address	Bit	Name	Description	R/W	Note
07h	[3:2]	RSLEW	00: 500V/us 01: 1000V/us 10: 1500V/us 11: 2000V/us	R/W	

The bit [1] is setting low side enable or disable. See the table 18. When bit [1] =0 then BUCK1 is synchronous converter, On the contrary; that bit is setting = 1, the BUCK1 was asynchronous converter.

Table 18: LSDIS setting register

Address	Bit	Name	Description	R/W	Note
07h	[1]	LSDIS	0:BUCK1 low side enable 0:BUCK1 low side disable	R/W	

The address 07 bit [0] is setting BUCK1 UVM function. See the table 19. When BUCK1 has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when BUCK1 has happened under voltage then IC is not happened shutdown.

Table 19: UVM setting register

Address	Bit	Name	Description	R/W	Note
07h	0	UVM	0: BUCK1 under voltage generates fault. 1: BUCK1 under voltage does not generate fault.	R	

Function Description (Cont.)

REG 08: PSR3CFG Register

The address 08 bits [6:4] are setting BUCK3 order in power on sequence. See the table 20. That's adjustment BUCK3 order in power on sequence from first to sixth to be powered on.

Table 20: PFR3OREDER setting register

Address	Bit	Name	Description	R/W	Note
08h	[6:4]	PSR3ORDER	000:BUCK3 is first power on … 101:BUCK3 is sixth power on 111:BUCK3 is sixth power on	R/W	

The bits [1:0] are setting driver slew rate. See the table 21. That's adjustment driver rising slew rate from 500V/us to 2000V/us.

Table 21: RSLEW setting register

Address	Bit	Name	Description	R/W	Note
08h	[3:2]	RSLEW	00: 500V/us 01: 1000V/us 10: 1500V/us 11: 2000V/us	R/W	

The bit [1] is setting low side enable or disable. See the table 22. When bit [1] =0 then BUCK3 is synchronous converter, On the contrary; that bit is setting = 1, the BUCK3 was asynchronous converter.

Table 22: LSDIS setting register

Address	Bit	Name	Description	R/W	Note
08h	[1]	LSDIS	0:BUCK3 low side enable 0:BUCK3 low side disable	R/W	

The address 08 bit [0] is setting BUCK3 UVM function. See the table 23. When BUCK3 has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when BUCK3 has happened under voltage then IC is not happened shutdown.

Table 23: UVM setting register

Address	Bit	Name	Description	R/W	Note
08h	0	UVM	0: BUCK3 under voltage generates fault. 1: BUCK3 under voltage does not generate fault.	R	

Function Description (Cont.)

REG 09: PSR2CFG Register

The address 09 bits [6:4] are setting BUCK2 order in power on sequence. See the table 24. That's adjustment BUCK2 order in power on sequence from first to sixth to be powered on.

Table 24: PFR2OREDER setting register

Address	Bit	Name	Description	R/W	Note
09h	[6:4]	PSR2ORDER	000:BUCK2 is first power on … 101:BUCK2 is sixth power on 111:BUCK2 is sixth power on	R/W	

The bits [1:0] are setting driver slew rate. See the table 25. That's adjustment driver rising slew rate from 500V/us to 2000V/us.

Table 25: RSLEW setting register

Address	Bit	Name	Description	R/W	Note
09h	[3:2]	RSLEW	00: 500V/us 01: 1000V/us 10: 1500V/us 11: 2000V/us	R/W	

The bit [1] is setting low side enable or disable. See the table 26. When bit [1] =0 then BUCK2 is synchronous converter, On the contrary; that bit is setting = 1, the BUCK2 was asynchronous converter.

Table 26: LSDIS setting register

Address	Bit	Name	Description	R/W	Note
09h	[1]	LSDIS	0:BUCK2 low side enable 0:BUCK2 low side disable	R/W	

The address 09 bit [0] is setting BUCK2 UVM function. See the table 27. When BUCK2 has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when BUCK2 has happened under voltage then IC is not happened shutdown.

Table 27: UVM setting register

Address	Bit	Name	Description	R/W	Note
09h	0	UVM	0: BUCK2 under voltage generates fault. 1: BUCK2 under voltage does not generate fault.	R	

Function Description (Cont.)

REG 0A: PSR4CFG Register

The address 0A bits [6:4] are setting BUCK4 order in power on sequence. See the table 28. That's adjustment BUCK4 order in power on sequence from first to sixth to be powered on.

Table 28: PFR4OREDER setting register

Address	Bit	Name	Description	R/W	Note
0Ah	[6:4]	PSR4ORDER	000:BUCK4 is first power on … 101:BUCK4 is sixth power on 111:BUCK4 is sixth power on	R/W	

The bits [1:0] are setting driver slew rate. See the table 29. That's adjustment driver rising slew rate from 500V/us to 2000V/us.

Table 29: RSLEW setting register

Address	Bit	Name	Description	R/W	Note
0Ah	[3:2]	RSLEW	00: 500V/us 01: 1000V/us 10: 1500V/us 11: 2000V/us	R/W	

The bit [1] is setting low side enable or disable. See the table 30. When bit [1] =0 then BUCK2 is synchronous converter, On the contrary; that bit is setting = 1, the BUCK2 was asynchronous converter.

Table 30: LSDIS setting register

Address	Bit	Name	Description	R/W	Note
0Ah	[1]	LSDIS	0:BUCK4 low side enable 0:BUCK4 low side disable	R/W	

The address 0A bit [0] is setting BUCK4 UVM function. See the table 31. When BUCK4 has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when BUCK4 has happened under voltage then IC is not happened shutdown.

Table 31: UVM setting register

Address	Bit	Name	Description	R/W	Note
0Ah	0	UVM	0: BUCK4 under voltage generates fault. 1: BUCK4 under voltage does not generate fault.	R	

Function Description (Cont.)

REG 0B: PSR5CFG Register

The address 0B bits [6:4] are setting BUCK5 order in power on sequence. See the table 32. That's adjustment BUCK5 order in power on sequence from first to sixth to be powered on.

Table 32: PFR5OREDER setting register

Address	Bit	Name	Description	R/W	Note
0Bh	[6:4]	PSR5ORDER	000:BUCK5 is first power on … 101:BUCK5 is sixth power on 111:BUCK5 is sixth power on	R/W	

The bits [1:0] are setting driver slew rate. See the table 33. That¡¦s adjustment driver rising slew rate from 500V/us to 2000V/us.

Table 33: RSLEW setting register

Address	Bit	Name	Description	R/W	Note
0Bh	[3:2]	RSLEW	00: 500V/us 01: 1000V/us 10: 1500V/us 11: 2000V/us	R/W	

The bit [1] is setting low side enable or disable. See the table 34. When bit [1] =0 then BUCK5 is synchronous converter, On the contrary; that bit is setting = 1, the BUCK2 was asynchronous converter.

Table 34: LSDIS setting register

Address	Bit	Name	Description	R/W	Note
0Bh	[1]	LSDIS	0:BUCK5 low side enable 0:BUCK5 low side disable	R/W	

The address 0B bit [0] is setting BUCK5 UVM function. See the table 35. When BUCK5 has happened under voltage, The IC will be shutdown in the address bit [0] =0. On the contrary; that bit is setting = 1, when BUCK5 has happened under voltage then IC is not happened shutdown.

Table 35: UVM setting register

Address	Bit	Name	Description	R/W	Note
0Bh	0	UVM	0: BUCK5 under voltage generates fault. 1: BUCK5 under voltage does not generate fault.	R	

Function Description (Cont.)

REG 0C: SEQCFG Register

The address 0C bit [7] is setting POK goes high time. When the address bit [7] = 0 then POK delay time controls by DLY1 [2:0], On the contrary; that bit is setting 1 then POK goes high time always is 8ms.No matter what setting DLY1 [2:0]. See the table 36 and 37.

Table 36: DLY1 [3] setting register

Address	Bit	Name	Description	R/W	Note
0Ch	7	DLY1[3]	0: Delay 1 time is set by DLY1[2:0] 1: delay 1 time is set at 8 ms no matter what DLY1 [2:0] sets.	R/W	

Table 37: DLY1 [2:0] setting register

Address	Bit	Name	Description	R/W	Note
0Ch	[2:0]	DLY1[2:0]	000: 10ms 001: 12ms … 111: 24ms	R/W	

The address 0C bits [6:5] are setting Delay 2 time. It's setting delay time between each output channels. The delay time range is from 0ms to 2ms. See the table 38.

Table 38: DLY2 setting register

Address	Bit	Name	Description	R/W	Note
0Ch	[2:0]	DLY2	00: 0ms 01: 0.5ms 10: 1ms 11: 2ms	R/W	

In addition, the bits are setting = 01, the POK goes high is must waiting after all channels has already. That's go high time is by DLY2 [2:0] setting.
Finally, the bits are setting = 11, the delay time is both form POR rising to first channel and the last one channel to POK go high.

Table 39: DLY1CFG setting register

Address	Bit	Name	Description	R/W	Note
0Ch	[4:3]	DLY1CFG	00: No Delay 01: Delay 1 is the delay before POK rising edge 10: Delay 1 is both the delay before starting sequence and before POK rising edge 11: Delay 1 is both the delay before starting sequence and before POK rising edge	R/W	

Function Description (Cont.)

REG 0E: REGCTRL Register

The address 0E bit [7] is setting DSM (Deep Sleep Mode), the address bit is setting = 0 then DSM is disable. On the contrary; that bit is setting = 1 then DSM is enabling. In addition, Using DEVSLP pin can use external to decided DSM function. See the table 40.

Table 40: DSM setting register

Address	Bit	Name	Description	R/W	Note
0Eh	7	DSM	0: Deep Sleep Mode is disable 1: Deep Sleep Mode is enable	R/W	

The address 0E bit [6] is LDO pull down function. When the address bit is setting =0 then LDO have pull down function in not DSM, in addition to this the others has pull down capability. On the contrary; that bit is setting = 1, it's always pull down capability. See the table 41.

Table 41: LDO_PDWN setting register

Address	Bit	Name	Description	R/W	Note
0Eh	6	LDO_PDWN	0: Pull down but not in DSM 1: Always pull down	R/W	

The address 0E bit [5] is BUCK5 regulator enable function. When the bit is setting =0, it's represent the BUCK5 is enable. On the contrary; that bit is setting = 1, the BUCK5 will be turn off.
The address 0E bits [4] to [0] are respectively representing BUCK4 regulator to LDO output. See the table 42.
But, the 0E bit [5] to [1] function enable was must setting to between VCCDR=2.1V to VCCDR falling. If the VCCDR voltage exceed VCCDR rising level then this function was disable.

Table 42: PSR5DIS to PSR1DIS and LDODIS setting register

Address	Bit	Name	Description	R/W	Note
0Eh	5	PSR5DIS	0: BUCK5 is turn on 1: BUCK5 is turn off	R/W	
0Eh	4	PSR4DIS	0: BUCK4 is turn on 1: BUCK4 is turn off	R/W	
0Eh	3	PSR2DIS	0: BUCK2 is turn on 1: BUCK2 is turn off	R/W	
0Eh	2	PSR3DIS	0: BUCK3 is turn on 1: BUCK3 is turn off	R/W	
0Eh	1	PSR1DIS	0: BUCK1 is turn on 1: BUCK1 is turn off	R/W	
0Eh	0	LDODIS	0: LDO is turn on 1: LDO is turn off	R/W	

Function Description (Cont.)

REG 0F: SETCTRL Register

The address 0F bit [3] is BUSY function. It cans detection the IC status now. When the bit is reading to 0, it cans operation by all registers. On the contrary; that bit is reading to 1 then all registers was locked, all registers writing is invalid. See the table 43.

Table 43: BUSY setting register

Address	Bit	Name	Description	R/W	Note
0Fh	3	BUSY	0: New operation can be commanded. 1: No new operation can be commanded' all registers are locked; writing operation will not have effect.	R/W	

The address 0F bits [1:0] are factory mode function. It cans load to different power sequence and output voltage. See the table 44.

Table 44: CMD [1:0] setting register

Address	Bit	Name	Description	R/W	Note
0Fh	[1:0]	CMD	00:no operation 01:save data as default on register REG00~GRE0E 10:restore default on register REG00~GEG0E 11:restore factory default on REG00~GRE0E	R/W	

Function Description (Cont.)

REG 10: SETCTRL Register

The address 10 bit [6] is detection over temperature protection function. When the bit is reading to 0 then the IC is not happened over temperature protection. On the contrary; that bit is reading to 1 then the IC has happened over temperature. See the table 45.

Table 45: TEMPFL setting register

Address	Bit	Name	Description	R/W	Note
10h	6	TEMPFL	0:no fault 1:temperature fault detected	R/W	

The address 10 bit [5] is BUCK5 regulator fault function. When the bit is reading to 0 then the BUCK5 is normal work. On the contrary; that bit is reading = 1 then the BUCK5 is error status.
The address 10 bits [4] to [0] are respectively representing BUCK4 regulator to LDO output. See the table 46.

Table 46: PSR5FL to PSR1FL and LDOFL register

Address	Bit	Name	Description	R/W	Note
10h	5	PSR5FL	0: no fault 1: BUCK5 fault detected	R/W	
10h	4	PSR4FL	0: no fault 1: BUCK4 fault detected	R/W	
10h	3	PSR2FL	0: no fault 1: BUCK2 fault detected	R/W	
10h	2	PSR3FL	0: no fault 1: BUCK3 fault detected	R/W	
10h	1	PSR1FL	0: no fault 1: BUCK1 fault detected	R/W	
10h	0	LDOFL	0: no fault 1: LDO fault detected	R/W	

Function Description (Cont.)

REG 11: TEMPEN Register

The address 11 bit [4] is alert1 detection function. When the bit is reading to 0 then alert1 is not asserted. On the contrary; that bit is reading to 1 then alert1 is asserted. The alert1 was asserted.
The address 11 bit [3] is the same bit [4]. It's the alert2 detection function. But the alert1 and alert2 are asserted not effect IC operation. See the table 47.

Table 47: AL1 and AL2 setting register

Address	Bit	Name	Description	R/W	Note
11h	4	AL1	0: Alert1 is not asserted 1: Alert1 is asserted	R/W	
11h	3	AL2	0: Alert2 is not asserted 1: Alert2 is asserted	R/W	

The address 11 bits [2:1] are temperature conversion rate function. The bits are adjustment from 0.25Hz to 8Hz. It's reading TS pin output voltage sampling time and return to REG12 TEMPREG register. See the table 48.

Table 48: CR [1:0] setting register

Address	Bit	Name	Description	R/W	Note
11h	[1:0]	CR[1:0]	00: 0.25 Hz 01: 1 Hz 10: 4 Hz 11: 8 Hz	R/W	

The address 11 bit [0] is temperature conversion enable/disable function. The bit is setting = 0 then TS pin output voltage information will be return to REG 12 TEMPREG register. On the contrary; the bit is setting = 1, the TS pin output voltage information is not return to TEMPREG register. At the same time, the TEMPREG data is keeping to previous one temperature conversion data. See the table 49.

Table 49: SD setting register

Address	Bit	Name	Description	R/W	Note
11h	0	SD	0: temperature conversion is not shutdown 1: temperature conversion is shutdown	R/W	

Function Description (Cont.)

REG 12: TEMPREG Register

The address 12 bits [7:0] are temperature sensor function. It will be the TS pin output voltage transform to temperature data. The temperature sensor range is from -40°C to 125°C. See the table 50.

Table 50: TEMPREG register

Address	Bit	Name	Description	R/W	Note
12h	[7:0]	TEMPREG	1101 1000: -40℃ … 1111 1111: -1℃ 0000 0000: 0℃ 0000 0001: 1℃ … 0111 1101: 125℃	R/W	

REG 13: THIGH Register

The address 13 bits [7:0] are setting temperature high function. When the temperature is exceeded the temperature high setting, the Alert 1 was from high go to low. On the contrary; the alert 1 is keep to high. See the table 51.

Table 51: THIGH setting register

Address	Bit	Name	Description	R/W	Note
13h	[7:0]	TEMPHIGH	1101 1000: -40℃ … 1111 1111: -1℃ 0000 0000: 0℃ 0000 0001: 1℃ … 0111 1101: 125℃	R/W	

REG 14: TLOW Register

The address 14 bits [7:0] are setting temperature low function. When the temperature is exceeded the temperature low setting, the Alert 0 was from high go to low. On the contrary; the alert 0 is keep to high. See the table 52.

Table 52: THIGH setting register

Address	Bit	Name	Description	R/W	Note
14h	[7:0]	TEMPLOW	1101 1000: -40℃ … 1111 1111: -1℃ 0000 0000: 0℃ 0000 0001: 1℃ … 0111 1101: 125℃	R/W	

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔIL, is 40% of maximum output current. The recommended inductor value can be calculated as below:

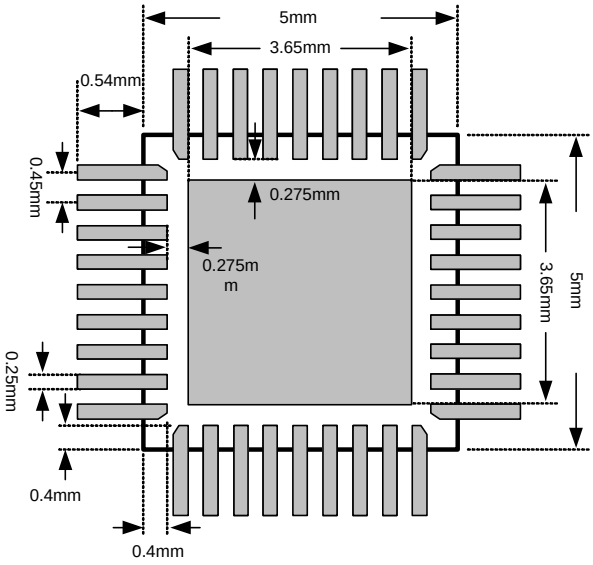
$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Capacitor Selection

The current-mode control scheme of the APW7705 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Min footprint



TDFN 5x5 - 36 * Just Recommend

I²C Programming

The APW7705's I²C Slave Address is a hard-coded 7-bit address 1111100. The APW7705 supports the following write and read protocol.

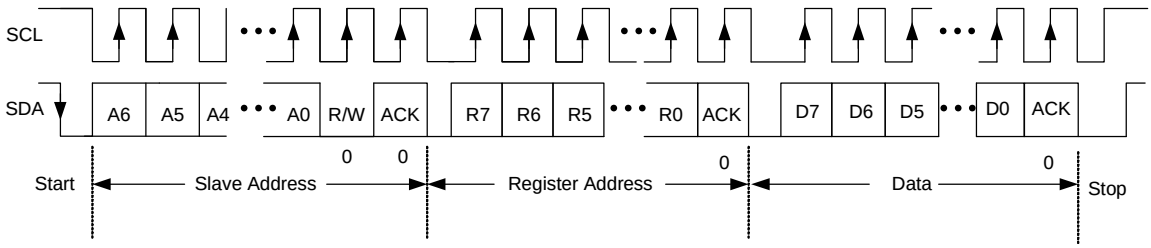


Figure 8. The Write Protocol of I2C interface writing to the APW7705

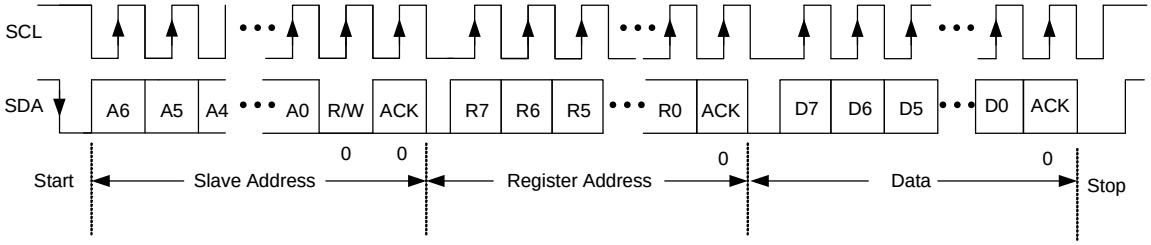


Figure 9. The Write Protocol of I2C interface writing to the APW7705

Register Map

Address	Name	Description
00h	LDOVL	LDO Regulator Voltage Level
01h	PSR1VL	Power Switching Regulator 1 Voltage Level
02h	PSR3VL	Power Switching Regulator 3 Voltage Level
03h	PSR2VL	Power Switching Regulator 2 Voltage Level
04h	PSR4VL	Power Switching Regulator 4 Voltage Level
05h	PSR5VL	Power Switching Regulator 5 Voltage Level
06h	LDOCFG	LDO Regulator Configuration
07h	PSR1CFG	Power Switcvhing Regulator 1 Configuration
08h	PSR3CFG	Power Switcvhing Regulator 3 Configuration
09h	PSR2CFG	Power Switcvhing Regulator 2 Configuration
0Ah	PSR4CFG	Power Switcvhing Regulator 4 Configuration
0Bh	PSR5CFG	Power Switcvhing Regulator 5 Configuration
0Ch	SEQCFG	Power ON/OFF Sequence Configuration
0Eh	REGCTRL	Regulator Control
0Fh	SETCTRL	Setting Control
10h	STATUS	Device Status
11h	TEMPEN	TEMP ADC Enable
12h	TEMPREG	External Temperature Register
13h	THIGH	Temperature High Limit
14h	TLOW	Temperature Low Limit

Register Definition

REG00 LDOVL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	LDOVLEN	Reserved	LDOVL[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0		Default values are power-on-strapped with VSELA, VSELB					

Bit Name	Bit Definition
LDOVLEN	LDO Output Voltage Level Selection Enable: 0: Voltage level selection register LDOVL [5:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default:APW7705A/B/C/D) 1: Voltage level selection register LDOVL [5:0] is enabled; output voltage changed according to the LDOVL [5:0] setting.
LDOVL[5:0]	LDO Output Voltage Level Selection: 000000: 1.7500V (Default :APW7705A) 000001: 1.7917V 000010: 1.8334V 000011: 1.8751V 000100: 1.9168V 000101: 1.9585V 000110: 2.0002V 000111: 2.0419V 001000: 2.0836V 001001: 2.1253V 001010: 2.1670V 001011: 2.2087V 001100: 2.2504V 001101: 2.2921V 001110: 2.3338V 001111: 2.3755V 010000: 2.4172V 010001: 2.4589V 010010: 2.5006V (Default:APW7705B/C) 010011: 2.5423V 010100: 2.5840V 010101: 2.6257V 010110: 2.6674V 010111: 2.7091V 011000: 2.7508V 011001: 2.7952V 011010: 2.8342V 011011: 2.8759V 011100: 2.9176V 011101: 2.9593V 011110: 3.0010V 011111: 3.0427V 100000: 3.0844V 100001: 3.1216V 100010: 3.1678V 100011: 3.2095V 100100: 3.2512V 100101: 3.2929V (Default:APW7705D) 100110: 3.3346V 100111: 3.3763V 101000: 3.418V 101001: 3.4597V 101010: 3.5014V

Register Definition

REG01 PSR1VL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PSR1VLEN	PSR1OCDIS	PSR1VL[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	Default values are power-on-strapped with VSELA, VSELB					

Bit Name	Bit Definition
PSR1VLEN	Buck 1 Regulator Output Voltage Level Selection Enable: 0: Voltage level selection register PSR1VL [5:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default:APW7705A/B/C/D) 1: Voltage level selection register PSR1VL [5:0] is enabled; output voltage changed according to the PSR1VL [4:0] setting.
PSR1OCDIS	Buck 1 Regulator Over-current Disable: 0: Over-current protection for Buck 1 Regulator is enabled. (Default:APW7705A/B/C/D) 1: Over-current protection for Buck 1 Regulator is disabled.
PSR1VL[5:0]	Buck 1 Regulator Output Voltage Level Selection: 000000 : 0.900V 000001 : 0.925V 000010 : 0.950V 000011 : 0.975V 000100 : 1.000V 000101 : 1.025V 000110 : 1.050V 000111 : 1.075V 001000 : 1.100V 001001 : 1.125V 001010 : 1.150V 001011 : 1.175V 001100 : 1.200V 001101 : 1.225V 001110 : 1.250V 001111 : 1.275V 010000 : 1.300V 010001 : 1.325V 010010 : 1.350V (Default:APW7705C) 010011 : 1.375V 010100 : 1.400V 010101 : 1.425V 010110 : 1.450V 010111 : 1.475V 011000 : 1.500V (Default:APW7705B/D) 011001 : 1.525V 011010 : 1.550V 011011 : 1.575V 011100 : 1.600V 011101 : 1.625V 011110 : 1.650V 011111 : 1.675V 100000 : 1.700V 100001 : 1.725V 100010 : 1.750V 100011 : 1.775V 100100 : 1.800V (Default:APW7705A) 100101 : 1.825V 100110 : 1.850V 100111 : 1.875V 101000 : 1.900V 101001 : 1.925V 101010 : 1.950V 101011 : 1.975V 101100 : 2.000V 101101 : 2.025V 101110 : 2.050V 101111 : 2.075V 110000 : 2.100V 110001 : 2.125V 110010 : 2.150V 110011 : 2.175V 110100 : 2.200V 110101 : 2.225V 110110 : 2.250V 110111 : 2.275V 111000 : 2.300V 111001 : 2.325V 111010 : 2.350V 111011 : 2.375V 111100 : 2.400V 111101 : 2.425V 111110 : 2.450V 111111 : 2.475V

Register Definition

REG02 PSR3VL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PSR3VLEN	PSR3OCDIS	PSR3VL[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	Default values are power-on-strapped with VSELA, VSELB					

Bit Name	Bit Definition
PSR3VLEN	Buck 3 Regulator Output Voltage Level Selection Enable: 0: Voltage level selection register PSR3VL [5:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default: APW7705A/B/C/D) 1: Voltage level selection register PSR3VL [5:0] is enabled; output voltage changed according to the PSR3VL [5:0] setting.
PSR3OCDIS	Buck 3 Regulator Over-current Disable: 0: Over-current protection for Buck 3 Regulator is enabled. (Default: APW7705A/B/C/D) 1: Over-current protection for Buck 3 Regulator is disabled.
PSR3VL[5:0]	Buck 3 Output Voltage Level Selection: 000000: 0.700V (Default: APW7705A/D) 000001: 0.725V 000010: 0.750V 000011: 0.775V 000100: 0.800V 000101: 0.825V 000110: 0.850V 000111: 0.875V 001000: 0.900V 001001: 0.925V 001010: 0.950V 001011: 0.975V 001100: 1.000V (Default: APW7705B) 001101: 1.025V 001110: 1.050V 001111: 1.075V 010000: 1.100V (Default: APW7705C) 010001: 1.125V 010010: 1.150V 010011: 1.175V 010100: 1.200V 010101: 1.225V 010110: 1.250V 010111: 1.275V 011000: 1.300V 011001: 1.325V 011010: 1.350V 011011: 1.375V 011100: 1.400V 011101: 1.425V 011110: 1.450V 011111: 1.475V 100000: 2.525V 100001: 2.550V 100010: 2.575V 100011: 2.600V 100100: 2.625V 100101: 2.650V 100110: 2.675V 100111: 2.700V 101000: 2.725V 101001: 2.750V 101010: 2.775V 101011: 2.800V 101100: 2.825V 101101: 2.850V 101110: 2875V 101111: 2.900V 110000: 2.925V 110001: 2.950V 110010: 2.975V 110011: 3.000V 110100: 3.025V 110101: 3.050V 110110: 3.075V 110111: 3.100V 111000: 3.125V 111001: 3.150V 111010: 3.175V 111011: 3.200V 111100: 3.225V 111101: 3.250V 111110: 3.275V 111111: 3.300V

Register Definition

REG03 PSR2VL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PSR2VLEN	PSR2OCDIS	Reserved	PSR2VL[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0		Default values are power-on-strapped with VSELA, VSELB				

Bit Name	Bit Definition
PSR2VLEN	Buck 2 Regulator Output Voltage Level Selection Enable: 0: Voltage level selection register PSR2VL [4:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default: APW7705A/B/C/D) 1: Voltage level selection register PSR2VL [4:0] is enabled; output voltage changed according to the PSR2VL [4:0] setting.
PSR2OCDIS	Buck 2 Regulator Over-current Disable: 0: Over-current protection for Buck 2 Regulator is enabled. (Default: APW7705A/B/C/D) 1: Over-current protection for Buck 2 Regulator is disabled.
PSR2VL[4:0]	Buck 2 Regulator Output Voltage Level Selection: 00000 : 1.5000V 00001 : 1.5375V 00010 : 1.5750V 00011 : 1.6125V 00100 : 1.6500V 00101 : 1.6875V 00110 : 1.7250V 00111 : 1.7625V 01000 : 1.8000V (Default:APW7705A/B/C/D) 01001 : 1.8375V 01010 : 1.8750V 01011 : 1.9125V 01100 : 1.9500V 01101 : 1.9875V 01110 : 2.0250V 01111 : 2.0625V 10000 : 2.1000V 10001 : 2.1375V 10010 : 2.1750V 10011 : 2.2125V 10100 : 2.2500V 10101 : 2.2875V 10110 : 2.3250V 10111 : 2.3625V 11000 : 2.4000V 11001 : 2.4375V 11010 : 2.4750V 11011 : 2.5125V 11100 : 2.5500V 11101 : 2.5875V 11110 : 2.6250V 11111 : 2.6625V

Register Definition

REG04 PSR4VL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PSR4VLEN	PSR4OCDIS	PSR4VL[5:0]					
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	Default values are power-on-strapped with VSELA, VSELB					

Bit Name	Bit Definition
PSR4VLEN	Buck 4 Regulator Output Voltage Level Selection Enable: 0: Voltage level selection register PSR4VL [5:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default: APW7705A/B/C/D) 1: Voltage level selection register PSR4VL [5:0] is enabled; output voltage changed according to the PSR4VL [5:0] setting.
PSR4OCDIS	Buck 4 Regulator Over-current Disable: 0: Over-current protection for Buck 4 Regulator is enabled. (Default: APW7705A/B/C/D) 1: Over-current protection for Buck 4 Regulator is disabled.
PSR4VL[5:0]	Buck 4 Output Voltage Level Selection: 000000: 0.700V 000001: 0.725V 000010: 0.750V 000011: 0.775V 000100: 0.800V 000101: 0.825V 000110: 0.850V 000111: 0.875V 001000: 0.900V 001001: 0.925V 001010: 0.950V 001011: 0.975V 001100: 1.000V (Default:APW7705B) 001101: 1.025V 001110: 1.050V 001111: 1.075V 010000: 1.100V 010001: 1.125V 010010: 1.150V 010011: 1.175V 010100: 1.200V (Default:APW7705A/C) 010101: 1.225V 010110: 1.250V 010111: 1.275V 011000: 1.300V 011001: 1.325V 011010: 1.350V 011011: 1.375V 011100: 1.400V 011101: 1.425V 011110: 1.450V 011111: 1.475V 100000: 2.525V 100001: 2.550V 100010: 2.575V 100011: 2.600V 100100: 2.625V 100101: 2.650V 100110: 2.675V 100111: 2.700V 101000: 2.725V 101001: 2.750V 101010: 2.775V 101011: 2.800V 101100: 2.825V 101101: 2.850V 101110: 2875V 101111: 2.900V 110000: 2.925V 110001: 2.950V 110010: 2.975V 110011: 3.000V 110100: 3.025V 110101: 3.050V 110110: 3.075V 110111: 3.100V 111000: 3.125V 111001: 3.150V 111010: 3.175V 111011: 3.200V 111100: 3.225V 111101: 3.250V 111110: 3.275V 111111: 3.300V (Default:APW7705D)

Register Definition

REG05 PSR5VL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PSR5VLEN	PSR5OCDIS	Reserved	PSR5VL[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0		Default values are power-on-strapped with VSELA, VSELB				

Bit Name	Bit Definition
PSR5VLEN	Buck 5 Regulator Output Voltage Level Selection Enable: 0: Voltage level selection register PSR5VL [4:0] is disabled; voltage level is selected via VSELA, VSELB pins. (Default: APW7705A/B/C/D) 1: Voltage level selection register PSR5VL [4:0] is enabled; output voltage changed according to the PSR5VL [4:0] setting.
PSR5OCDIS	Buck 5 Regulator Over-current Disable: 0: Over-current protection for Buck 5 Regulator is enabled. (Default: APW7705A/B/C/D) 1: Over-current protection for Buck 5 Regulator is disabled.
PSR5VL[4:0]	Buck 5 Regulator Output Voltage Level Selection: 00000: 0.700V 00001: 0.725V 00010: 0.750V 00011: 0.775V 00100: 0.800V 00101: 0.825V 00110: 0.850V 00111: 0.875V 01000: 0.900V (Default:APW7705A) 01001: 0.925V 01010: 0.950V 01011: 0.975V 01100: 1.000V (Default:APW7705B) 01101: 1.025V 01110: 1.050V 01111: 1.075V 10000: 1.100V (Default:APW7705C) 10001: 1.125V 10010: 1.150V 10011: 1.175V 10100: 1.200V (Default:APW7705D) 10101: 1.225V 10110: 1.250V 10111: 1.275V 11000: 1.300V 11001: 1.325V 11010: 1.350V 11011: 1.375V 11100: 1.400V 11101: 1.425V 11110: 1.450V 11111: 1.475V

Register Definition

REG06 LDOCFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	LDOORDER[2:0]			Reserved		DEGL	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0		

Bit Name	Bit Definition
LDOORDER[2:0]	Order In Power On Sequence: 000: LDO is the first regulator to be powered-on. (Default:APW7705D) 001: LDO is the second regulator to be powered-on. 010: LDO is the third regulator to be powered-on. 011: LDO is the forth regulator to be powered-on. (Default:APW7705B/C) 100: LDO is the fifth regulator to be powered-on. 101: LDO is the sixth regulator to be powered-on. 110: LDO is the sixth regulator to be powered-on. 111: LDO is the sixth regulator to be powered-on. (Default:APW7705A)
DEGL	LDO Fault Deglitch Time: 0: 10μs (Default: APW7705A/B/C/D) 1: 5μs
UVM	Under-voltage Mask: 0: LDO Under-voltage generates fault. (Default: APW7705A/B/C/D) 1: LDO Under-voltage does not generate fault.

REG07 PSR1CFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	PSR1ORDER[2:0]			RSLEW[1:0]		LSDIS	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0	0	0

Bit Name	Bit Definition
PSR1ORDER[2:0]	Order In Power On Sequence: 000: Buck 1 regulator is the first regulator to be powered-on. (Default:APW7705A) 001: Buck 1 regulator is the second regulator to be powered-on. (Default:APW7705D) 010: Buck 1 regulator is the third regulator to be powered-on. (Default:AP7705B/C) 011: Buck 1 regulator is the forth regulator to be powered-on. 100: Buck 1 regulator is the fifth regulator to be powered-on. 101: Buck 1 regulator is the sixth regulator to be powered-on. 110: Buck 1 regulator is the sixth regulator to be powered-on. 111: Buck 1 regulator is the sixth regulator to be powered-on.
RSLEW[1:0]	Buck 1 Regulator Driver Slew Rate: 00: 500V/μs 01: 1000V/μs 10: 1500V/μs 11: 2000V/μs (Default: APW7705A/B/C/D)
LSDIS	Buck 1 Regulator Low Side Disable: 0: Buck 1 regulator low side enabled. (Default:APW7705A/B/C/D) 1: Buck 1 regulator low side disabled.
UVM	Buck 1 Regualtor Under-voltage Mask: 0: Buck 1 regulator under-voltage generates fault. (Default: APW7705A/B/C/D) 1: Buck 1 regulator under-voltage does not generate fault.

Register Definition

REG08 PSR3CFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	PSR3ORDER[2:0]			RSLEW[1:0]		LSDIS	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0	0	0

Bit Name	Bit Definition
PSR3ORDER[2:0]	Order In Power On Sequence: 000: Buck 3 regulator is the first regulator to be powered-on. (Default:APW7705B/C) 001: Buck 3 regulator is the second regulator to be powered-on. 010: Buck 3 regulator is the third regulator to be powered-on. 011: Buck 3 regulator is the forth regulator to be powered-on. 100: Buck 3 regulator is the fifth regulator to be powered-on. 101: Buck 3 regulator is the sixth regulator to be powered-on. 110: Buck 3 regulator is the sixth regulator to be powered-on. 111: Buck 3 regulator is the sixth regulator to be powered-on. (Default:APW7705A/D)
RSLEW[1:0]	Buck3 Regulator Driver Slew Rate: 00: 500V/µs (Default:APW7705A/B/C/D) 01: 1000V/µs 10: 1500V/µs 11: 2000V/µs
LSDIS	Buck 3 Regualtor Low Side Disable: 0: Buck 3 regulator low side enabled. (Default:APW7705A/B/C/D) 1: Buck 3 regulator low side disabled.
UVM	Buck 3 Regulator Under-voltage Mask: 0: Buck 3 regulator under-voltage generates fault. (Default:APW7705A/B/C/D) 1: Buck 3 regulator under-voltage does not generate fault.

Register Definition

REG09 PSR2CFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	PSR2ORDER[2:0]			RSLEW[1:0]		LSDIS	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0	0	0

Bit Name	Bit Definition
PSR2ORDER[2:0]	Order In Power On Sequence: 000: Buck 2 regulator is the first regulator to be powered-on. (Default:APW7705A) 001: Buck 2 regulator is the second regulator to be powered-on. 010: Buck 2 regulator is the third regulator to be powered-on. (Default: APW7705D) 011: Buck 2 regulator is the forth regulator to be powered-on. (Default:APW7705B/C) 100: Buck 2 regulator is the fifth regulator to be powered-on. 101: Buck 2 regulator is the sixth regulator to be powered-on. 110: Buck 2 regulator is the sixth regulator to be powered-on. 111: Buck 2 regulator is the sixth regulator to be powered-on.
RSLEW[1:0]	Buck 2 Regulator Driver Slew Rate: 00: 500V/µs 01: 1000V/µs 10: 1500V/µs 11: 2000V/µs (Default:APW7705A/B/C/D)
LSDIS	Buck 2 Regulator Low Side Disable: 0: Buck 2 regulator low side enabled. (Default:APW7705A/B/C/D) 1: Buck 2 regulator low side disabled.
UVM	Buck 2 Regulator Under-voltage Mask: 0: Buck 2 regulator under-voltage generates fault. (Default:APW7705A/B/C/D) 1: Buck 2 regulator under-voltage does not generate fault.

Register Definition

REG0A PSR4CFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	PSR4ORDER[2:0]			RSLEW[1:0]		LSDIS	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0	0	0

Bit Name	Bit Definition
PSR2ORDER[2:0]	Order In Power On Sequence: 000: Buck 4 regulator is the first regulator to be powered-on. (Default:APW7705B/C) 001: Buck 4 regulator is the second regulator to be powered-on. (Default:APW7705A/D) 010: Buck 4 regulator is the third regulator to be powered-on. 011: Buck 4 regulator is the forth regulator to be powered-on. 100: Buck 4 regulator is the fifth regulator to be powered-on. 101: Buck 4 regulator is the sixth regulator to be powered-on. 110: Buck 4 regulator is the sixth regulator to be powered-on. 111: Buck 4 regulator is the sixth regulator to be powered-on.
RSLEW[1:0]	Buck 4 Regulator Driver Slew Rate: 00: 500V/µs (Default:APW7705A/B/C/D) 01: 1000V/µs 10: 1500V/µs 11: 2000V/µs
LSDIS	Buck 4 Regulator Low Side Disable: 0: Buck 4 regulator low side enabled. (Default:APW7705A/B/C/D) 1: Buck 4 regulator low side disabled.
UVM	Buck 4 Regulator Under-voltage Mask: 0: Buck 4 regulator under-voltage generates fault. (Default:APW7705A/B/C/D) 1: Buck 4 regulator under-voltage does not generate fault.

Register Definition

REG0B PSR5CFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	PSR4ORDER[2:0]			RSLEW[1:0]		LSDIS	UVM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Power On Default	0				0	0	0	0

Bit Name	Bit Definition
PSR2ORDER[2:0]	Order In Power On Sequence: 000: Buck 5 regulator is the first regulator to be powered-on. (Default:APW7705A/D) 001: Buck 5 regulator is the second regulator to be powered-on. (Default:APW7705B/C) 010: Buck 5 regulator is the third regulator to be powered-on. 011: Buck 5 regulator is the forth regulator to be powered-on. 100: Buck 5 regulator is the fifth regulator to be powered-on. 101: Buck 5 regulator is the sixth regulator to be powered-on. 110: Buck 5 regulator is the sixth regulator to be powered-on. 111: Buck 5 regulator is the sixth regulator to be powered-on.
RSLEW[1:0]	Buck 5 Regulator Driver Slew Rate: 00: 500V/µs 01: 1000V/µs (Default:APW7705A/B/C/D) 10: 1500V/µs 11: 2000V/µs
LSDIS	Buck 5 Regulator Low Side Disable: 0: Buck 5 regulator low side enabled. (Default:APW7705A/B/C/D) 1: Buck 5 regulator low side disabled.
UVM	Buck 5 Regulator Under-voltage Mask: 0: Buck 5 regulator under-voltage generates fault. (Default:APW7705A/B/C/D) 1: Buck 5 regulator under-voltage does not generate fault.

Register Definition

REG0C SEQCFG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DLY1[3]	DLY2[1:0]		DLY1CFG[1:0]		DLY1[2:0]		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	1	0	1	0	1	0	0	0
Bit Name	Bit Definition							
DLY1[3]	Delay 1 Time Setting: 0: Delay 1 time is set by DLY1[2:0]. **1: Delay 1 time is set at 8ms no matter what DLY1[2:0] sets. (Default:APW7705A/B/C/D)**							
DLY2[1:0]	Delay 2 Time Setting: 00: 0ms 01: 0.5ms (Default:APW7705A/B/C/D) 10: 1ms 11: 2ms							
DLY1CFG[1:0]	Delay 1 Configuration: 00: No delay **01: Delay 1 is the delay before POK rising edge.** (Default:APW7705A/B/C/D) 10: Delay 1 is the delay before starting sequence. 11: Delay 1 is both the delay before starting sequence and before POK rising edge.							
DLY1[2:0]	Delay 1 Time Setting: **000: 10ms** (Default:APW7705A/B/C/D) 001: 12ms 010: 14ms 011: 16ms 100: 18ms 101: 20ms 110: 22ms 111: 24ms							

Register Definition

REG0E REGCTRL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DSM	LDO_PDWN	PSR5DIS	PSR4DIS	PSR2DIS	PSR3DIS	PSR1DIS	LDODIS
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	0	0	0	0	0

Bit Name	Bit Definition
DSM	Deep Sleep Mode Enable: 0: Deep Sleep Mode is disabled. (Default:APW7705A/B/C/D) 1: Deep Sleep Mode is enabled.
LDO_PDWN	LDO Pull Down: 0: Pull down but not in DSM. 1: Always pull down. (Default:APW7705A/B/C/D)
PSR5DIS	Buck 5 Regulator Disable: 0: Buck 5 regulator is turned on. (Default: APW7705A/B/C/D) 1: Buck 5 regulator is turned off.
PSR4DIS	Buck 4 Regulator Disable: 0: Buck 4 regulator is turned on. (Default: APW7705A/B/C/D) 1: Buck 4 regulator is turned off.
PSR2DIS	Buck 2 Regulator Disable: 0: Buck 2 regulator is turned on. (Default: APW7705A/B/C/D) 1: Buck 2 regulator is turned off.
PSR3DIS	Buck 3 Regulator Disable: 0: Buck 3 regulator is turned on. 1: Buck 3 regulator is turned off. (Default: APW7705A/D)
PSR1DIS	Buck 1 Regulator Disable: 0: Buck 1 regulator is turned on. (Default: APW7705A/B/C/D) 1: Buck 1 regulator is turned off.
LDODIS	LDO Regulator Disable: 0: LDO regulator is turned on. (Default:APW7705B/C/D) 1: LDO regulator is turned off. (Default:APW7705A)

Register Definition

REG0F SETCTRL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved				BUSY	Reserved	CMD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
BUSY	OTP Memory Busy: 0: New operation can be commanded. 1: No new operation can be commanded; all registers are locked; writing operation will not have effect.							
CMD[1:0]	Command: 00: no operation. (Default:APW7705A/B/C/D) 01: save data as default on register REG00~REG0E. 10: restore default on register REG00~REG0E. 11: Restore factory default on REG00~REG0E.							

REG10 SETCTRL Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved	TEMPFL	PSR5FL	PSR4FL	PSR2FL	PSR3FL	PSR1FL	LDOFL
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
TEMPFL	Temperature Fault: 0: No fault. 1: Temperature fault detected.							
PSR5FL	Buck 5 Regulator Fault: 0: No fault. 1: Buck 5 regulator fault detected.							
PSR4FL	Buck 4 Regulator Fault: 0: No fault. 1: Buck 4 regulator fault detected.							
PSR2FL	Buck 2 Regulator Fault: 0: No fault. 1: Buck 2 regulator fault detected.							
PSR3FL	Buck 3 Regulator Fault: 0: No fault. 1: Buck 3 regulator fault detected.							
PSR1FL	Buck 1 Regulator Fault: 0: No fault. 1: Buck 1 regulator fault detected.							
LDOFL	LDO Regulator Fault 0: No fault. 1: LDO regulator fault detected.							

Register Definition

REG11 TEMPEN Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved			AL1	AL0	CR[1:0]		SD
Read/Write	R	R	R	R	R	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	0
Bit Name	Bit Definition							
AL1	ALERT1 Status: 0: ALERT1 is not asserted. 1: ALERT1 is asserted.							
AL0	ALERT0 Status: 0: ALERT0 is not asserted. 1: ALERT0 is asserted.							
CR[1:0]	Temperature Conversion Rate: 00: 0.25Hz 01: 1Hz 10: 4Hz (Default:APW7705A/B/C/D) 11: 8Hz							
SD	Temperature Conversion Shutdown: 0: Temperature Conversion is not shutdown. (Default:APW7705A/B/C/D) 1: Temperature Conversion is shutdown							

REG12 TEMPREG Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	TEMPREG[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power On Default								
Bit Name	Bit Definition							
TEMPREG[7:0]	Temperature Readout According To External Temperature Information(via TS pin): 1101 1000: -40℃ . . 1111 1110: -2°C 1111 1111: -1 °C 0000 0000: 0 °C 0000 0001: 1 °C 0000 0010: 2 °C . . . 0111 1101: 125℃							

Register Definition

REG13 THIGH Register

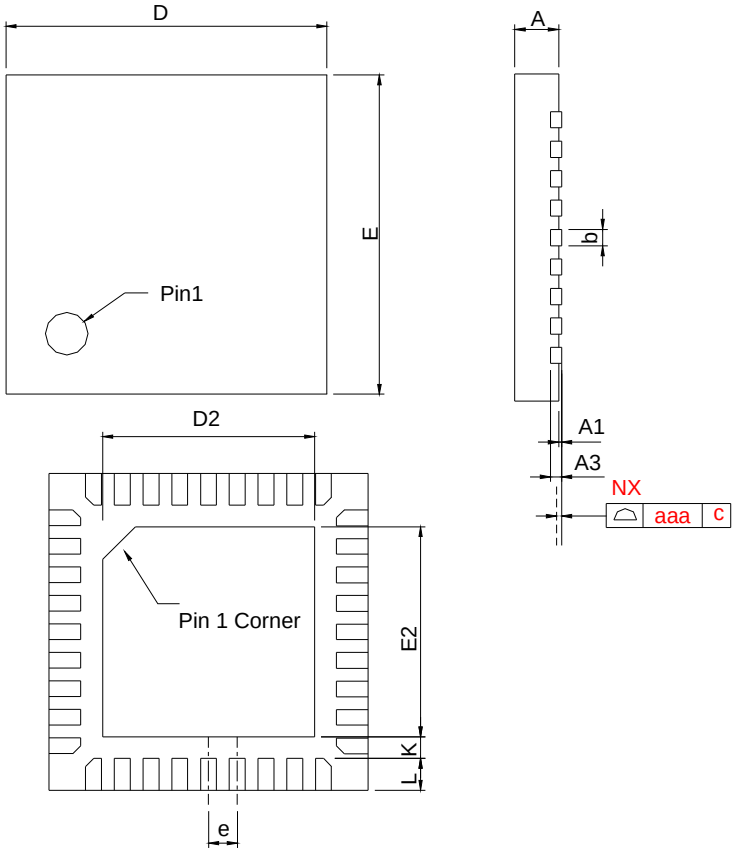
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	THIGH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	0	0	1	0
Bit Name	Bit Definition							
TEMPHIGH[7:0]	Temperature High Limit Threshold: 1101 1000: -40℃ . . 1111 1110: -2℃ 1111 1111: -1℃ 0000 0000: 0℃ (Default:APW7705A/B/C/D) 0000 0001: 1℃ 0000 0010: 2℃ . . . 0111 1101: 125℃							

REG14 TLOW Register

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	TLOW[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	Bit Definition							
TEMPLOW[7:0]	Temperature Low Limit Threshold: 1101 1000: -40℃ . 1111 0110: -10℃ (Default: APW7705A/B/C/D) . 1111 1110: -2℃ 1111 1111: -1℃ 0000 0000: 0℃ 0000 0001: 1℃ 0000 0010: 2℃ . . . 0111 1101: 125℃							

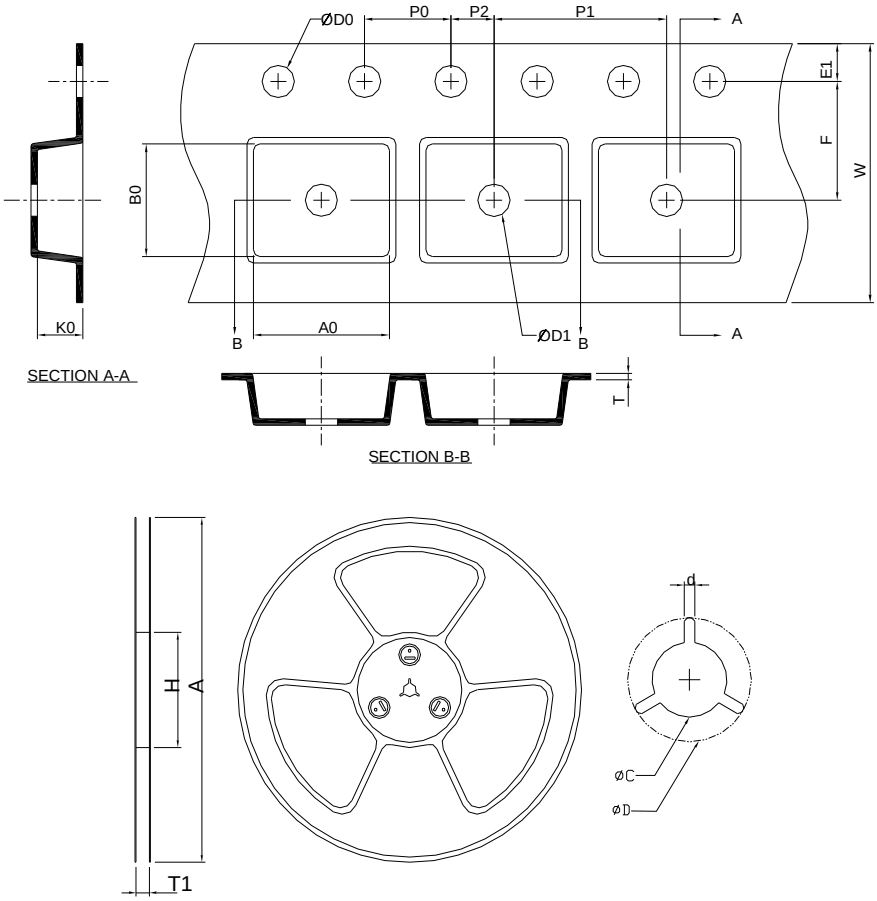
Package Information

TQFN5x5-36



SYMBOL	TQFN5*5-36			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	4.90	5.10	0.193	0.201
D2	3.50	3.80	0.138	0.150
E	4.90	5.10	0.193	0.201
E2	3.50	3.80	0.138	0.150
e	0.45 BSC		0.018 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

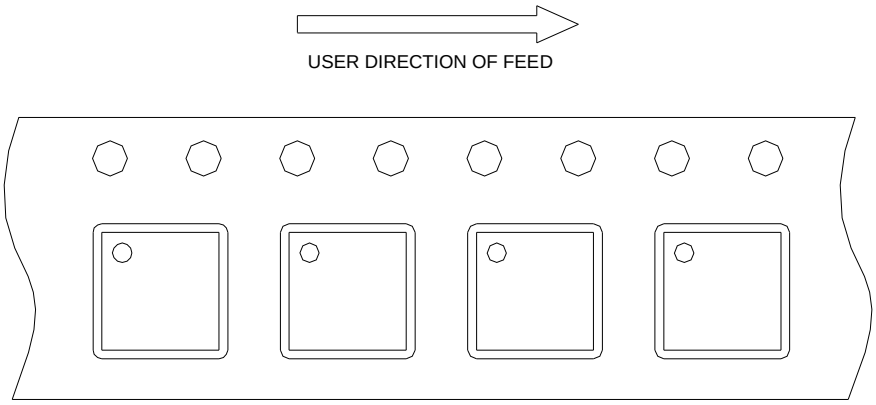
(mm)

Devices Per Unit

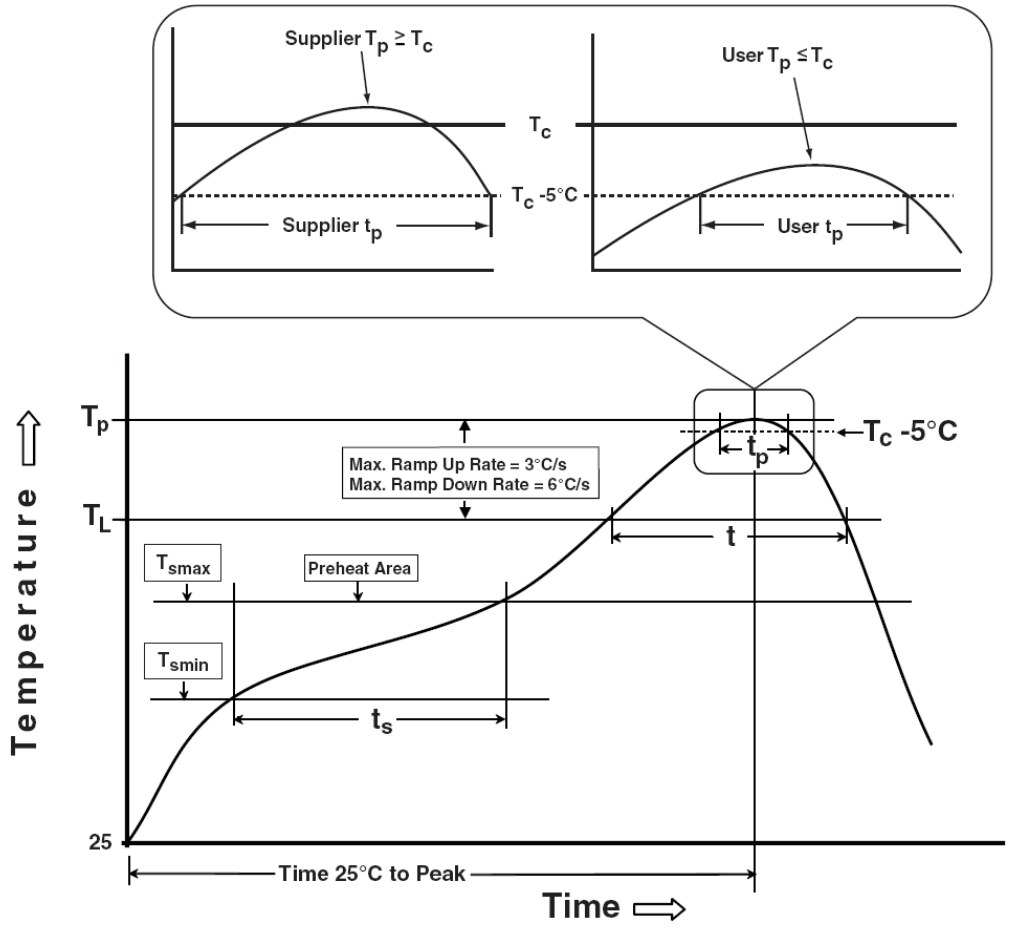
Package Type	Unit	Quantity
TQFN5x5-36	Tape & Reel	2500

Taping Direction Information

TQFN5x5-36



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838