Dual-Phase COT Buck PWM Controller

Features

- **Support Wide Input Voltage Range from 5.4V to 24V**
- **VCC Support Range from 4.5V to 5.5V**
- **Integrated High-side MOSFET Driver with Integrated Bootstrap P-CHMOSFET**
- **Drive N-CH MOSFET with built in Adaptive Dead Time Control Scheme**
- **Support Single-PFM, Two Phase PWM, and Ultra-sonic PFM mode**
- **PWM Switching Frequency 500KHz ~700KHz by FSpin**
- **Built in Constant On Time PWM Control with Current Balance Operation**
- **Support Single and Two Phase PWM Control by LGATE2 & PSI Voltage Setting**
- **Built in Adjustable Over Current Protection by LGATE1 Setting.**
- **Built in Under Voltage Protection with Latch off Mode**
- **Built in Over Voltage Protection with Latch off Mode**
- **Built in Over Temperature Protection**
- **Individual EN & POK indicator**
- **Built in VID for VOUT adjustment**
- **Built in decay down mode.**
- **TQFN 4x4-24 Package**

Applications

- **Notebook**
- **Graphic card**
- **Motherboard**

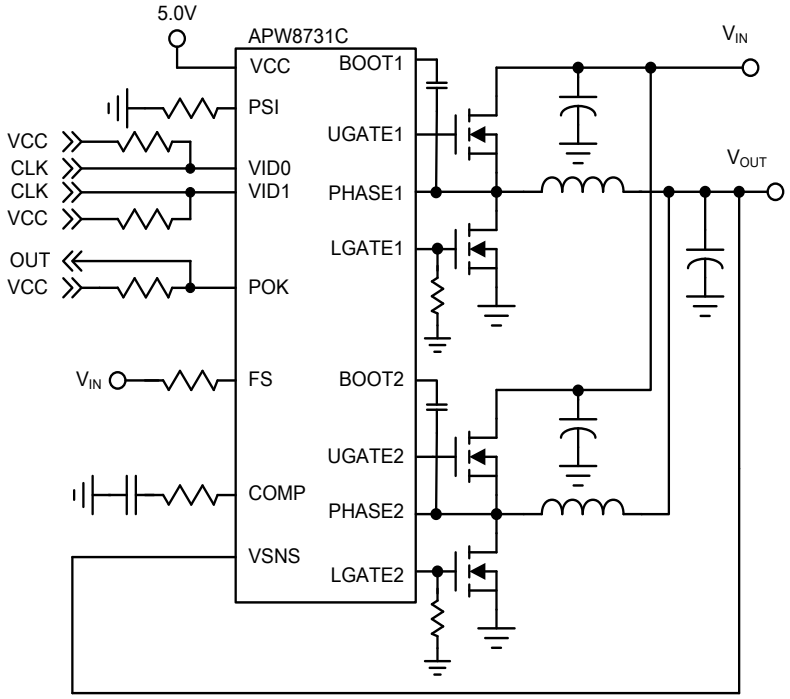
General Description

The APW8731C is a dual-phase PWM control IC which provides a precision voltage regulation system and supports wide input range from 5.4V to 24V. By integrating dual-phase power MOSFET drivers and controller into the one IC, APW8731C can reduce the number of external components for a cost and space saving power management solution.

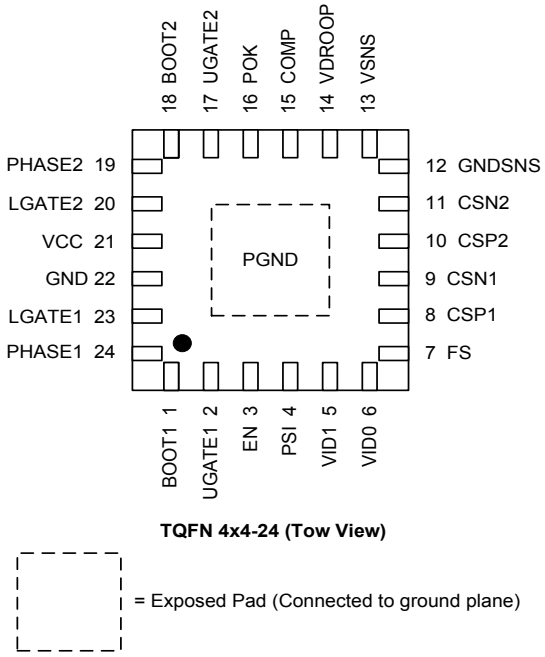
The APW8731C's PWM controller adopts constant on time architecture which has the trait of excellent transient resposnse. The PWM controller features automatic phase reduction that can either operates in dual-phase mode or single-phase mode, depending on resistor settings on PSI and LGATE2 pin. The resistor on LGATE2 pin can also set PWM/PFM/USM operations. The device integrates adjustable load line voltage positioning (droop) and detect voltage on low side $R_{DS(ON)}$ for channel-current balance.

The protection functions include over current protection (OCP), under voltage protection (UVP), over voltage protection (OVP) and over temperature protection (OTP). OCP, UVP or OVP occurrence will lead to latch-off. A thermal shutdown function is implemented to prevent damages due to heat by excessive power dissipation. Typically the thermal shutdown threshold temperature is 150°C.When the thermal shutdown is triggered the device stops switching and output voltage re-start after the junction temperature cools by 30°C. APW8731C is packaged in TQFN 4x4-24.

Simplified Application Circuit



Pin Configuration



TQFN 4x4-24 (Tow View)

= Exposed Pad (Connected to ground plane)

Ordering and Marking Information

APW8731C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB: TQFN4x4-24 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8731C QB: 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
$V_{BOOT1/2}$	BOOT1/ BOOT2 to GND Voltage		-0.3 ~ 35	V
	BOOT1/ BOOT2 to PHASE1/PHASE2 Voltage		-0.3 ~ 7	V
$V_{UGATE1/2}$	UGATE1/UGATE2 to PHASE1/PHASE2	<20ns pulse width	-5 ~ $V_{BOOT1/2}$+0.3	V
		>20ns pulse width	-0.3 ~ $V_{BOOT1/2}$+0.3	
$V_{LAGTE1/2}$	LGATE1/LGATE2 to PGND Voltage	<20ns pulse width	-5 ~ V_{VCC}+0.3	V
		>20ns pulse width	-0.3 ~ V_{VCC}+0.3	
$V_{PHASE1/2}$	PHASE1/PHASE2 to PGND Voltage	<20ns pulse width	-5 ~ 35	V
		>20ns pulse width	-1 ~ 28	
V_{FS}	FS to GND Voltage(V_{EN}=0V)		-0.3 ~ 28	V
V_{CC}	VCC Supply Voltage (VCC pin to GND)		-0.3 ~ 7	V
	EN,PSI,VID0,VID1,POK,FS,COMP,VDROOP,CSP1,CSN1,CSP2,CSP2,VSNS		-0.3 ~ V_{VCC}+0.3	V
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds.		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	40	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air	7	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Range	Unit
V_{IN}	Input Voltage		5.4 ~ 24	V
V_{VCC}	VCC Supply Voltage		4.5 ~ 5.5	V
I_{OUT}	Converter Output Current		0 ~ 32	A
L_{OUT}	Converter Output Inductor		0.15 ~ 0.68	μH
L_{DCR}	Minimum Direct Current Resistance of the Inductor	Two-phase	3	mΩ
		Single-phase	2	
C_1	VCC Input Capacitor		6.8 ~ 10	μF
R_{FS}	Operation Frequency Setting		470 ~ 620	kΩ
T_J	Junction Temperature		-40 ~ 125	°C
T_A	Ambient Temperature		-40 ~ 85	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Refer to Figure 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 7.4V, V_{CC} = 5V, T_A = 25°C, unless otherwise. Typical values are at T_A = 25°C

Symbol	Parameter	Test condition	APW8731C			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current (Single-Phase)	V_{EN} = H, V_{PSI} = 0V, R_{LG2} = 1.8 kΩ	-	180	-	μA
		V_{EN} = H, V_{PSI} = 0V, R_{LG2} = NC	-	245	-	μA
	VCC Shutdown Current	V_{EN} = L, V_{VCC}= 5V	-	-	10	μA
POWER ON RESET						
V_{POR}	VCC POR Threshold Voltage	V_{VCC} Rising	4.1	4.3	4.45	V
	POR Hysteresis Voltage	V_{VCC} Falling	-	0.2	-	V
SOFT-START						
t_{SS}	Soft-Start Time	The time interval is the VOUT voltage from 0% to 100%.	350	500	650	μs
PWM FREQUENCY SETTING						
t_{ON}	On Time	V_{IN}=19V, V_{OUT}=1.8V, By FS resistor =500kΩ	168	187	206	ns
$t_{ON(MIN)}$	Minimum On Time	Over all temperature	-	70	-	ns
$t_{OFF(MIN)}$	Minimum Off Time		-	225	-	ns
I_{FS}	Leakage Current	V_{FS}=24V, V_{EN}=0V	-	0.1	1	μA
BOOTSTRAP SWITCH						
R_{P_RNO}	Bootstrap P-CH MOSFET R_{ON}	I_F=10mA	-	10	20	Ω
I_R	Bootstrap Reverse Leakage Current	$V_{BOOT1/2}$ = 29V, $V_{PHASE1/2}$ = 24V, V_{VCC}=5V	-	0.1	0.5	μA
EN, VID0, VID1						
	Input Logic High Voltage	Input voltage is at rising	1.2	-	-	V
	Input Logic Low Voltage	Input voltage is at falling	-	-	0.6	V
	Input Leakage Current	V_{VCC}=5V, V_{EN} / $V_{VID0/1}$=5V	-	0.1	1	μA
	EN Turn on Delay Time		-	280	-	μs
	Output Enable Time	Timing info here is for initial ramp up for first EN. Not for VID changes.	-	-	2	ms
SR	VID Transition Slew Rate		13	-	60	mV/μs
t_{RAMP_UP}	Ramping Up Time	Time from VID signal to V_{OUT} voltage change complete	-	-	150	μs
t_{RAMP_DOWN}	Ramping Down Time	Time from VID signal to V_{OUT} voltage change complete. (does not apply for decay down mode) (Note 4)	-	-	150	μs
POWER GOOD INDICATOR						
	POK Leakage Current	V_{POK} = 5V	-	0.1	1	μA
	POK Voltage Threshold	When V_{VSNS} from lower value to target value, POK goes high.	85	90	95	%
		When V_{VSNS} from target value to upper value, POK goes low.	2.28	2.4	2.52	V
		When V_{VSNS} from target value to lower value, POK goes low.	80	85	90	%
	POK Output Low Voltage	I_{POK_SINK} = 4mA	-	-	0.4	V

Electrical Characteristics (Cont.)

Refer to Figure 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 7.4V, V_{CC} = 5V, T_A = 25°C, unless otherwise. Typical values are at T_A = 25°C

Symbol	Parameter	Test condition	APW8731C			Unit
			Min.	Typ.	Max.	
POWER GOOD INDICATOR (Cont.)						
	POK Enable Delay Time	The time between 0% of the target value and the rising edge of the POK.	450	650	850	μs
OUTPUT VOLTAGE						
V_{REF}	Reference Voltage	V_{VID0}=H;V_{VID1}=H,	-	1.8	-	V
		V_{VID0}=L;V_{VID1}=H	-	1.65	-	V
		V_{VID0}=H;V_{VID1}=L	-	1.1	-	V
		V_{VID0}=L;V_{VID1}=L	-	0	-	V
	Output Voltage Accuracy	V_{OUT}=1.8V, V_{IN}=5.4V ~ 24V	-18	-	18	mV
		V_{OUT}=1.65V, V_{IN}=5.4V ~ 24V	-16.5	-	16.5	mV
		V_{OUT}=1.1V, V_{IN}=5.4V ~ 24V	-11	-	11	mV
POWER SAVING MODE						
I_{PSI}	Leakage Current	V_{PSI}=5V, V_{EN}=0V	-	0.1	1	μA
V_{PSI_H}	PSI High Threshold Voltage	V_{PSI} Rising	1.4	1.5	1.6	V
V_{PSI_L}	PSI Low Threshold Voltage	V_{PSI} Falling	0.5	0.6	0.7	V
	Two Phase with PWM to Single Phase with PFM Delay Time	(Note 4)	-	300	-	μs
	Two Phase with PWM to Single Phase with PWM Delay Time	(Note 4)	-	300	-	μs
	Two Phase with PWM to Single Phase with Ultra -sonic PFM Delay Time	(Note 4)	-	300	-	μs
F_{USM}	Switching Frequency of Ultra-sonic PFM	R_{LG2}=3.3kΩ	25	35	45	kHz
I_{LGATE2}	Mode Setting Current	Source from LGATE2 pin	216	240	264	μA
V_{LGATE2_1}	Operation Mode Logic	Case1: R_{LG2}=N.C	2	-	-	V
V_{LGATE2_2}		Case2: R_{LG2}=6.2kΩ ±1%	1.2	-	1.7	V
V_{LGATE2_3}		Case3: R_{LG2}=3.3kΩ ±1%	0.68	-	0.95	V
V_{LGATE2_4}		Case4: R_{LG2}=1.8kΩ ±1%	-	-	0.5	V
	CSN1/2 Leakage Current	V_{EN}=0V, $V_{CSN1/2}$=5V	-	0.1	1	μA
	CSP1/2 Leakage Current	V_{EN}=0V, $V_{CSP1/2}$=5V	-	0.1	1	μA
	RDROOP Leakage Current	V_{DROOP}=5V	-	0.1	1	μA

Electrical Characteristics (Cont.)

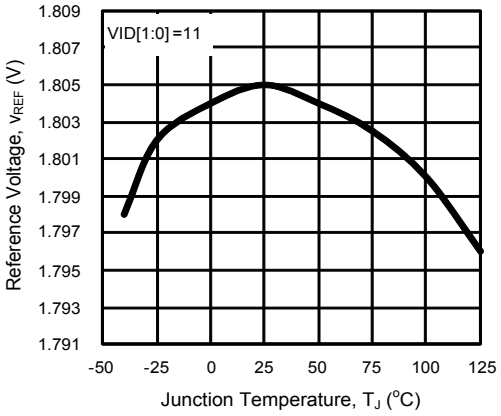
Refer to Figure 1 in the "Typical Application Circuits". These specifications apply over V_{IN} = 7.4V, V_{CC} = 5V, T_A = 25°C, unless otherwise. Typical values are at T_A = 25°C

Symbol	Parameter	Test condition	APW8731C			Unit
			Min.	Typ.	Max.	
ZERO CROSS DETECTION						
V_{ZC}	Zero Cross Detection Voltage	$V_{PHASE1/2}$-V_{PGND}	-5	-	5	mV
GATE DRIVERS						
$I_{UGATE1/2}$	UGATE1/2 Leakage Current	UGATE1/2 no switching	-	0.1	1	µA
$I_{LGATE1/2}$	LGATE1/2 Leakage Current	LGATE1/2 no switching	-	0.1	1	µA
$I_{PHASE1/2}$	PHASE1/2 Leakage Current	$V_{PHASE1/2}$ =24V, V_{CC}=5.5V	-	0.1	1	µA
$I_{CSN1/2}$	CSN1/2 Leakage Current	$V_{CSN1/2}$=5V	-	0.1	1	µA
R_{UG-SRC}	Upper Side Gate Source	I_{UGATE}=100mA Sourcing (Note 4)	-	2	4	Ω
R_{UG-SNK}	Upper Side Gate Sink	I_{UGATE}=100mA Sinking	-	1	2	Ω
R_{LG-SRC}	Low Side Gate Source	I_{LGATE}=100mA Sourcing	-	1.5	3	Ω
R_{LG-SNK}	Low Side Gate Sink	I_{LGATE}=100mA Sinking	-	1	2	Ω
t_{DT}	Dead Time	(Note 4)	-	20	-	ns
I_{VSNS}		V_{VSNS} = 2V	-	20	30	µA
R_{VSNS_DIS}	Soft-Stop Discharge Resistance	When the protection circuit is triggered or the EN logic level is low.	-	6	10	Ω
I_{GNDSNS}	GNDSNS Input Current	V_{EN}=0V, V_{GNDSNS} =5V	-	0.1	1	µA
PROTECTIONS						
	Over Voltage Protection (OVP)	Sensed at V_{VSNS}	2.28	2.4	2.52	V
	OVP De-bounce Time	(Note 4)	-	10	-	µs
	Under Voltage Protection (UVP)	(V_{VSNS}-V_{GNDSNS})/V_{REF}	45	50	55	%
	UVP De-bounce Time	(Note 4)	-	10	-	µs
I_{OCSET}	OCP Setting Current	Over all temperature condition	110	120	130	µA
	Maximum OCP Setting Voltage	When R_{OCSET}=open	0.9	1	-	V
	Thermal Shutdown Threshold	(Note 4)	-	150	-	°C
	Thermal Shutdown Hysteresis	(Note 4)	-	30	-	°C

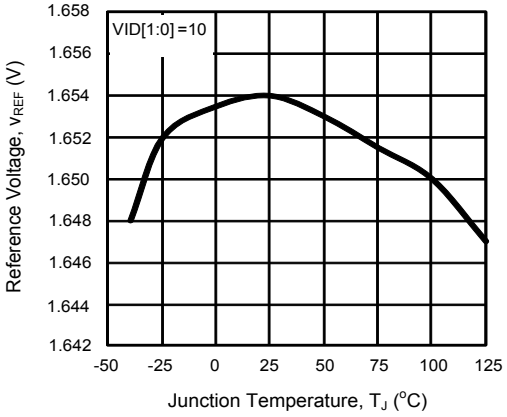
Note 4: Guarantee by design, not production test.

Typical Operating Characteristics

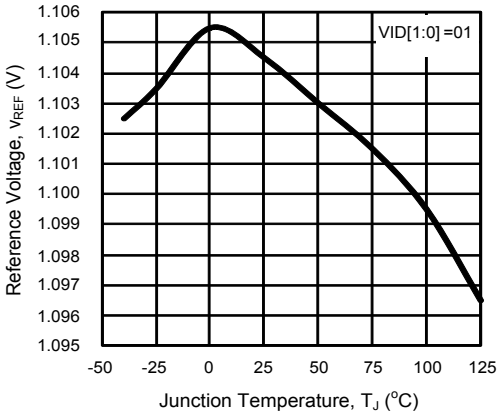
Reference Voltage vs. Junction Temperature



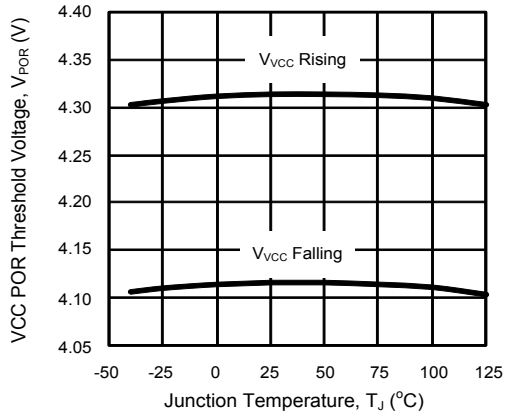
Reference Voltage vs. Junction Temperature



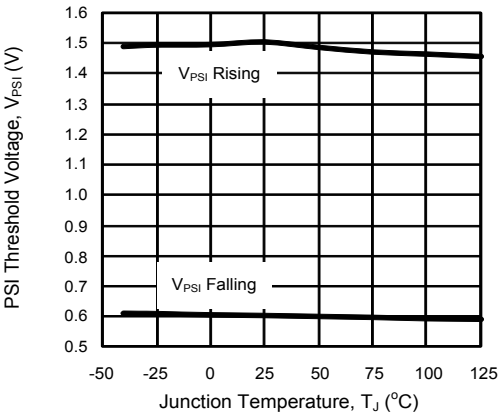
Reference Voltage vs. Junction Temperature



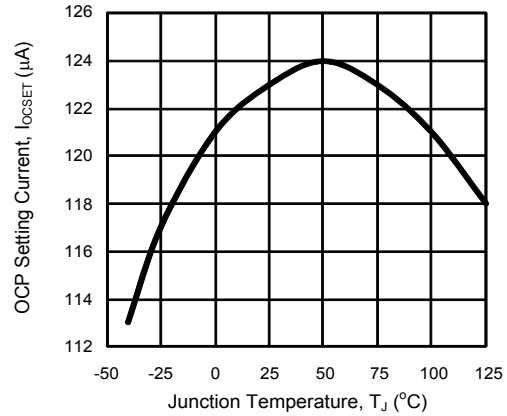
VCC POR Threshold Voltage vs. Junction Temperature



PSI Threshold Voltage vs. Junction Temperature

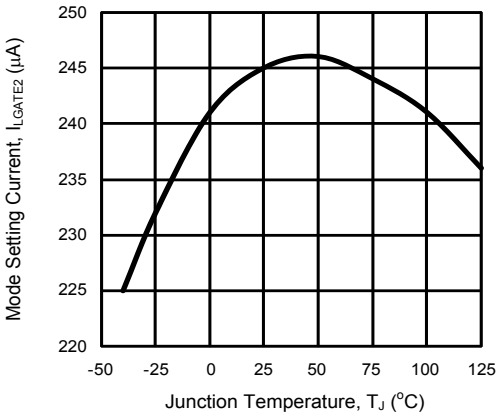


OCP Setting Current vs. Junction Temperature

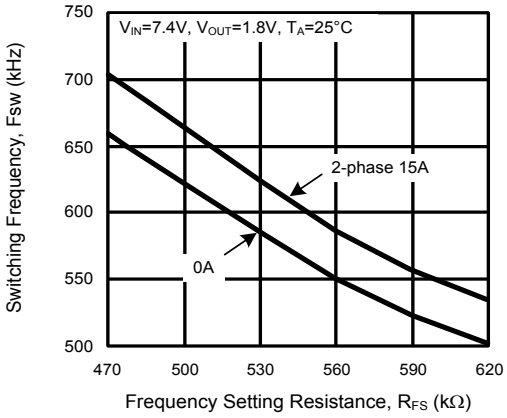


Typical Operating Characteristics

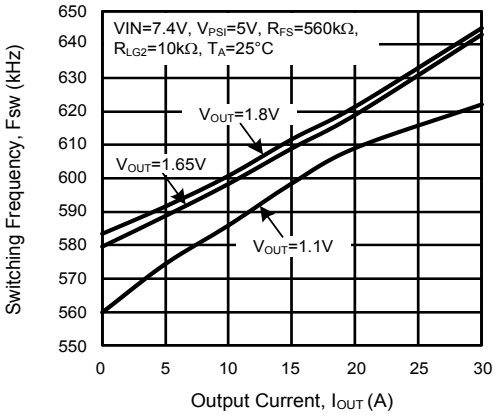
Mode Setting Current vs. Junction Temperature



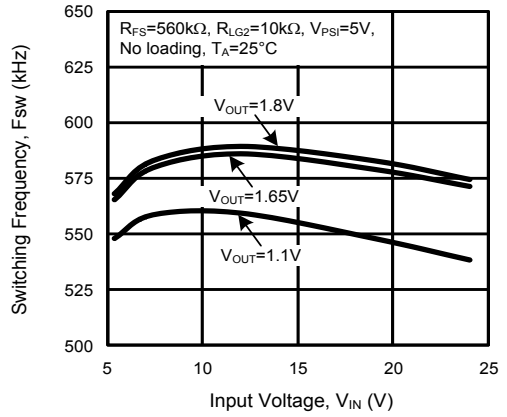
Switching Frequency vs. Frequency Setting Resistance



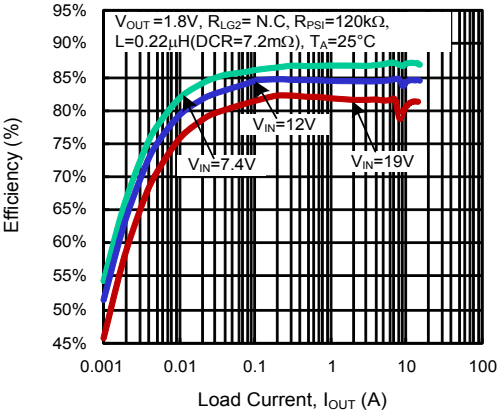
Switching Frequency vs. Output Current



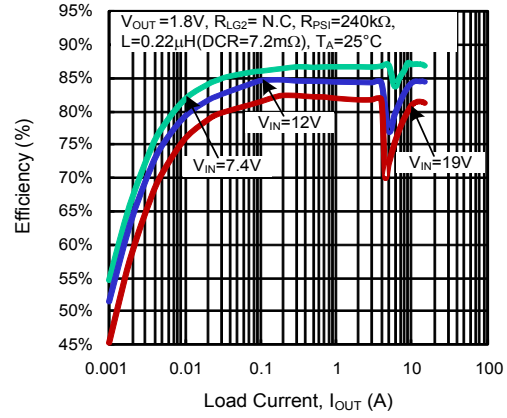
Switching Frequency vs. Input Voltage



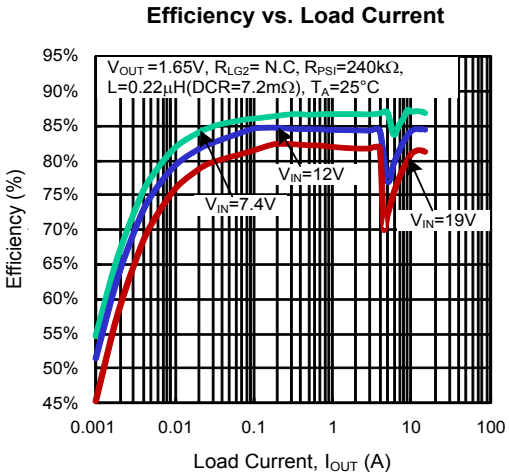
Efficiency vs. Load Current



Efficiency vs. Load Current



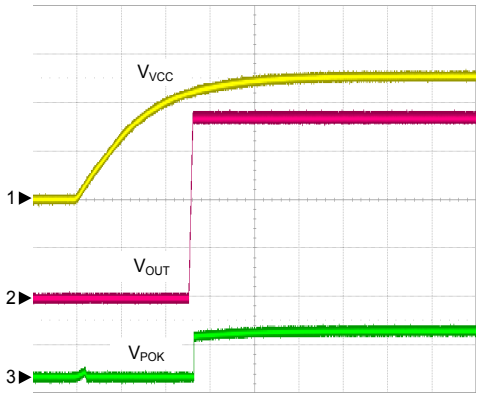
Typical Operating Characteristics



Operating Waveforms

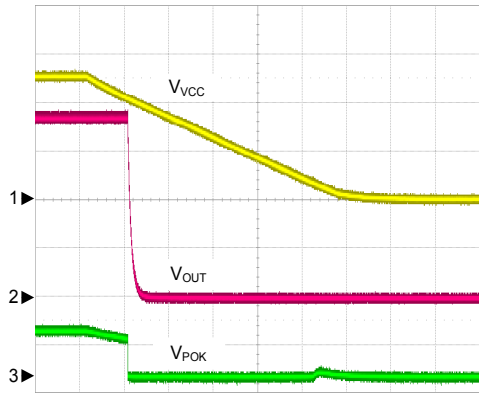
Refer to the typical application circuit. The test condition is V_{IN}=7.4V, V_{OUT}=1.8V,T_A= 25°C unless otherwise specified.

Power On



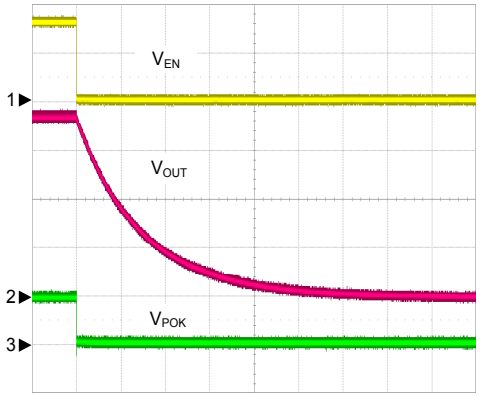
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VCC}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 5ms/Div

Power Off



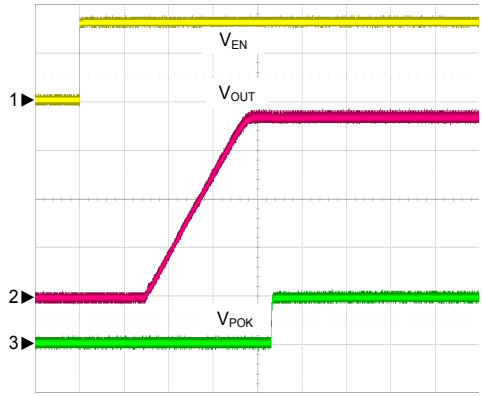
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VCC}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 10ms/Div

Shutdown



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 500µs/Div

Enable

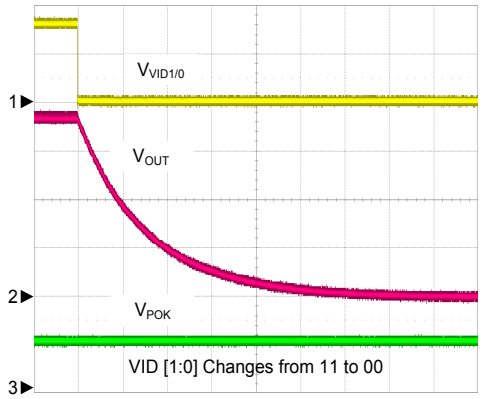


R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{EN}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 200µs/Div

Operating Waveforms

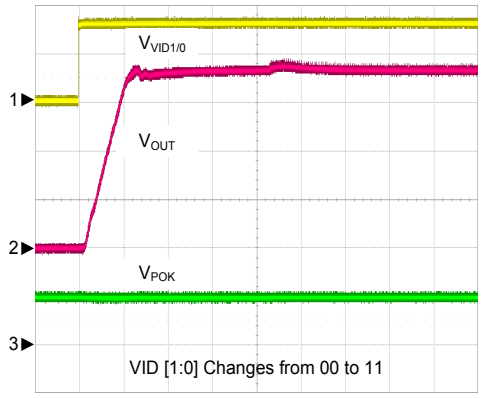
Refer to the typical application circuit. The test condition is V_{IN}=7.4V, V_{OUT}=1.8V,T_A= 25°C unless otherwise specified.

Dynamic Output Voltage Control



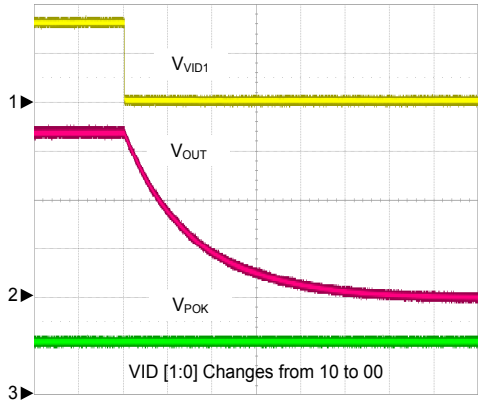
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 500µs/Div

Dynamic Output Voltage Control



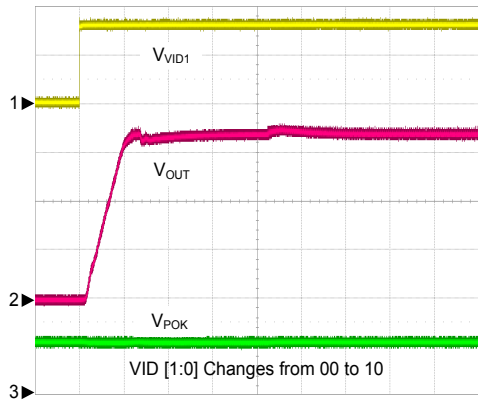
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID}, 2V/Div, DC
CH2: V_{OUT}, 0.5V/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

Dynamic Output Voltage Control



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID1}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 500µs/Div

Dynamic Output Voltage Control

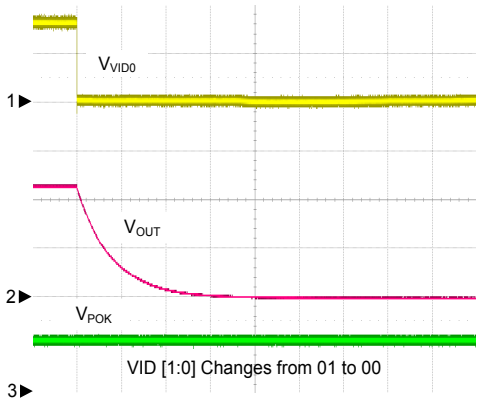


R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID1}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

Operating Waveforms

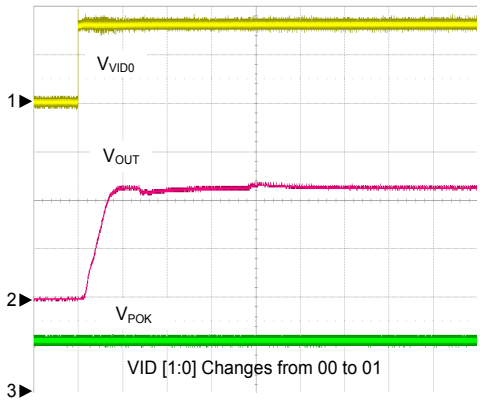
Refer to the typical application circuit. The test condition is V_{IN}=7.4V, V_{OUT}=1.8V,T_A= 25°C unless otherwise specified.

Dynamic Output Voltage Control



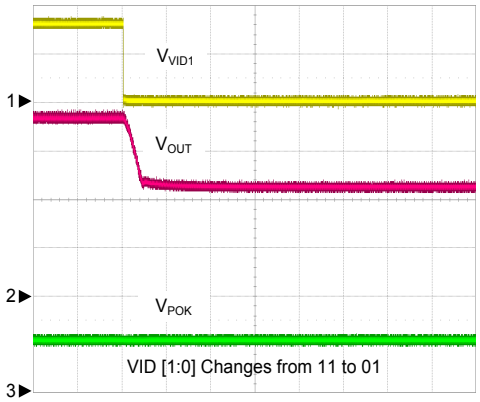
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID0}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 1ms/Div

Dynamic Output Voltage Control



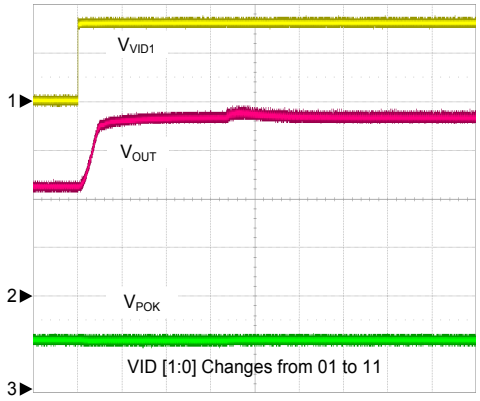
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID0}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

Dynamic Output Voltage Control



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID1}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

Dynamic Output Voltage Control

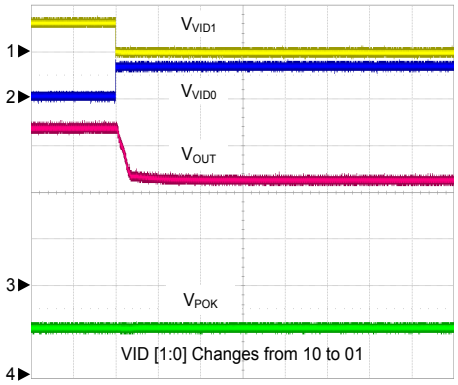


R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω
CH1: V_{VID1}, 2V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=7.4V, V_{OUT}=1.8V,T_A= 25°C unless otherwise specified.

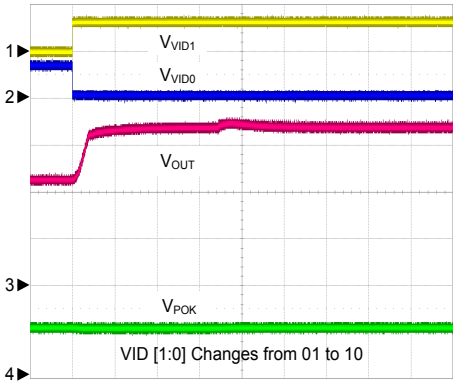
Dynamic Output Voltage Control



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω

CH1: V_{VID1}, 5V/Div, DC
CH2: V_{VID0}, 5V/Div, DC
CH3: V_{OUT}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

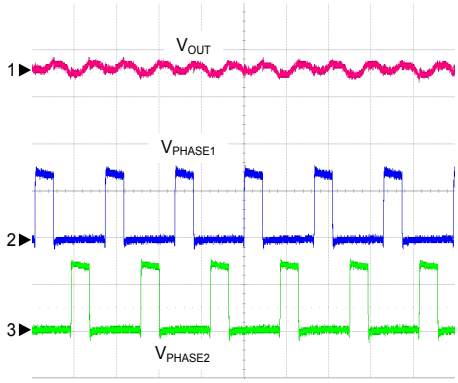
Dynamic Output Voltage Control



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω

CH1: V_{VID1}, 5V/Div, DC
CH2: V_{VID0}, 5V/Div, DC
CH3: V_{OUT}, 500mV/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 100µs/Div

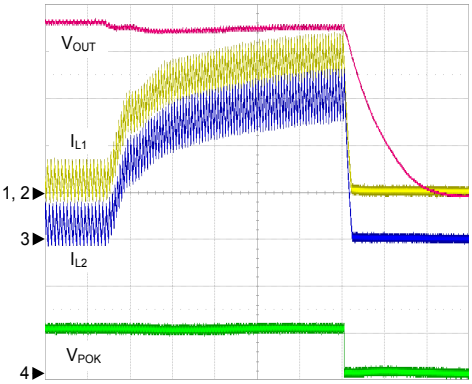
Normal Operation



R_{PSI}=240kΩ, R_{LG2}=10kΩ, I_{OUT}=14A

CH1: V_{VCC}, 50mV/Div, DC offset 1.8V
CH2: V_{PHASE1}, 5V/Div, DC
CH3: V_{PHASE2}, 5V/Div, DC
TIME: 1µs/Div

OCP



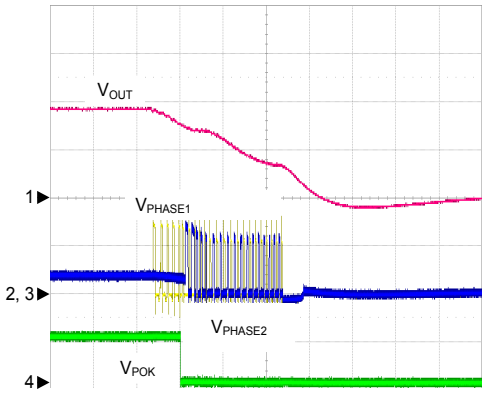
R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{OCSET}=4.7kΩ, I_{LOAD}=5A to OCP

CH1: V_{OUT}, 500mV/Div, DC
CH2: I_{L1}, 10A/Div, DC
CH3: I_{L2}, 10A/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 20µs/Div

Operating Waveforms

Refer to the typical application circuit. The test condition is V_{IN}=7.4V, V_{OUT}=1.8V,T_A= 25°C unless otherwise specified.

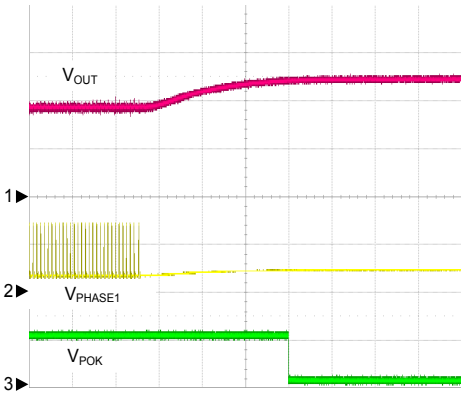
UVP



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{OCSET}=4.7kΩ

CH1: V_{OUT}, 1V/Div, DC
CH2: V_{PHASE1}, 5V/Div, DC
CH3: V_{PHASE2}, 5V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 10µs/Div

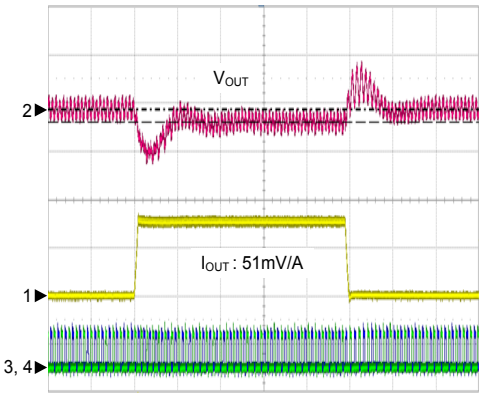
OVP



R_{PSI}=240kΩ, R_{LG2}=10kΩ, R_{LOAD}=1Ω

CH1: V_{OUT}, 1V/Div, DC
CH2: V_{PHASE1}, 5V/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 50µs/Div

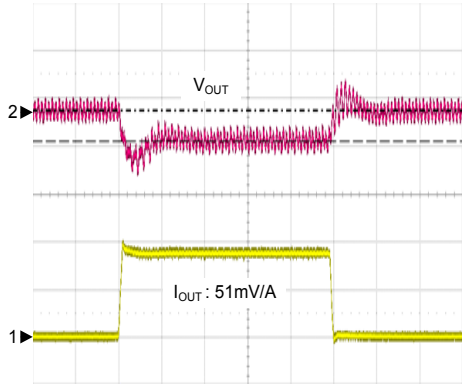
Load Transient Response



I_{OUT} =6.6A to 22A to 6.6A (slew rate=15.4A/µs)

CH1: I_{OUT}, 500mV/Div, DC offset 336mV
CH2: V_{OUT}, 50mV/Div, DC offset 1.65V
CH3: V_{PHASE1}, 5V/Div, DC
CH4: V_{PHASE2}, 5V/Div, DC
TIME: 10µs/Div

Load Transient Response

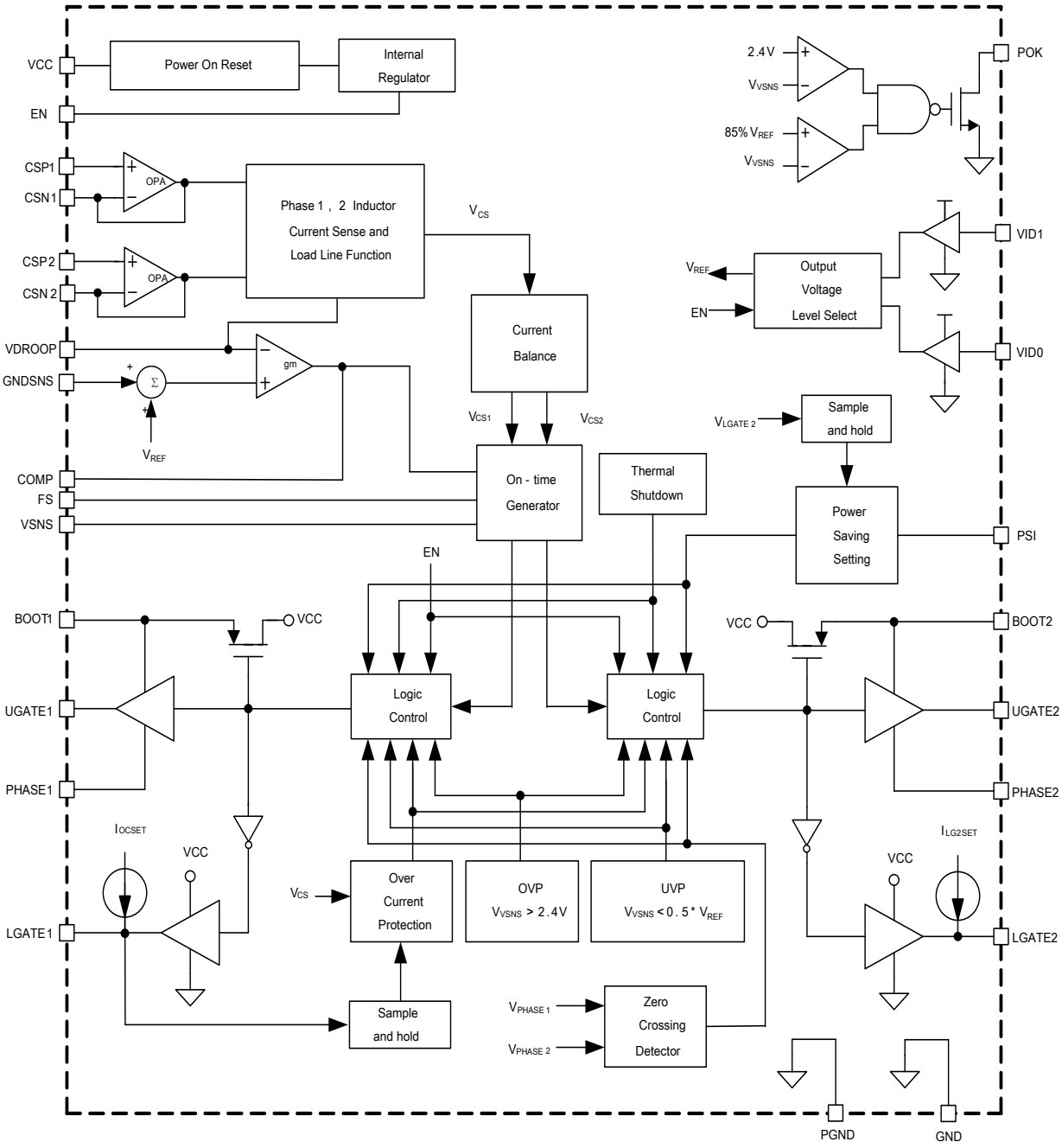


I_{OUT} =12.4A to 31A to 12.4A (slew rate=18.6A/µs)
R_{DROOP}=1kΩ, C_{DROOP}=330pF
CH1: I_{OUT}, 500mV/Div, DC offset 632mV
CH2: V_{OUT}, 50mV/Div, DC offset 1.8V
TIME: 10µs/Div

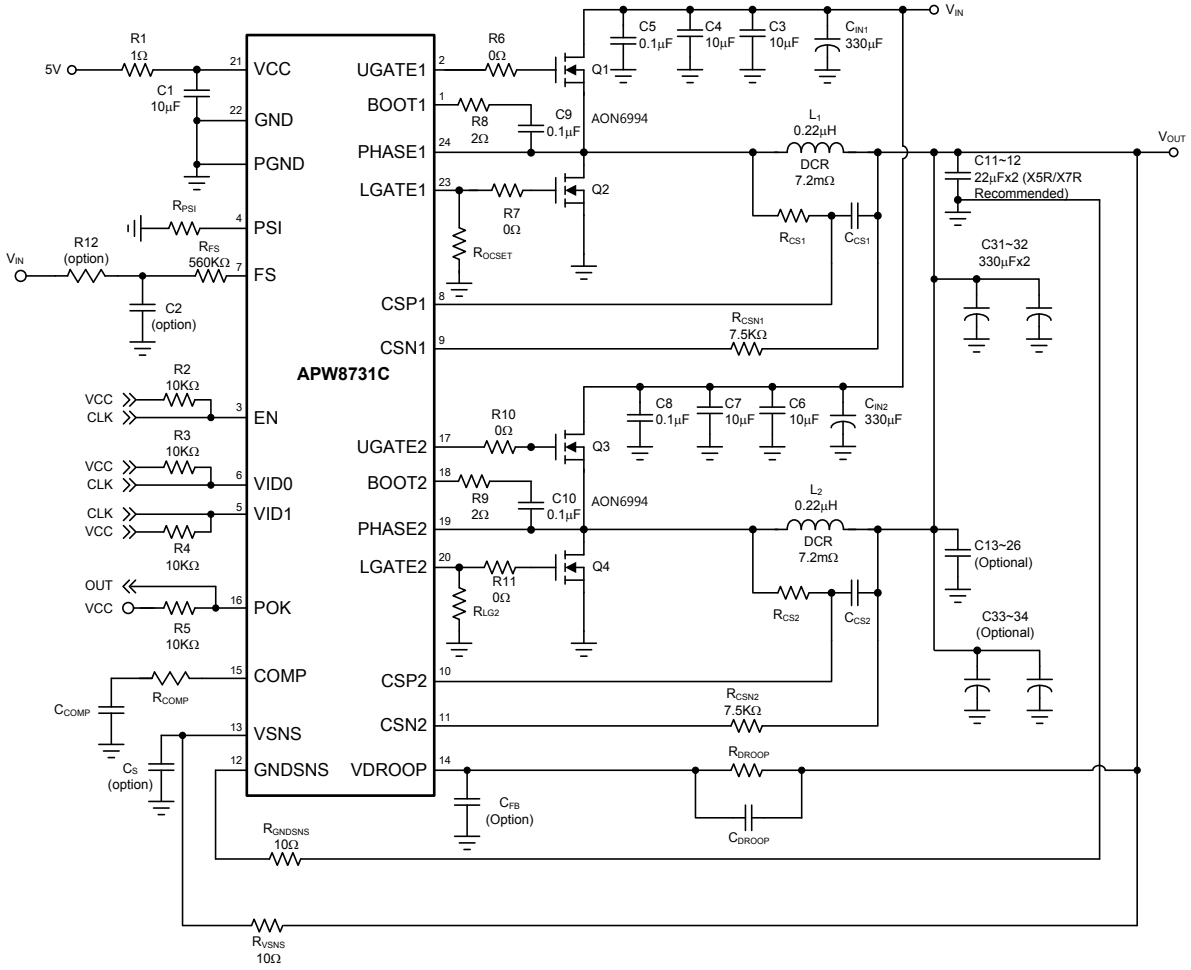
Pin Descriptions

PIN	NAME	FUNCTION
1	BOOT1	External Power N-CH MOSFET Gate Drive Boost Input for channel 1. A 0.1μF to 1μF capacitor should be connected from PHASE1 to BOOT1 for power N-CH MOSFET gate driving purposes. Ensure that C_{BOOT1} is placed near the IC.
2	UGATE1	Upper Gate Driver Output for channel 1. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
3	EN	Enable Input pin. This pin is set high to turn on the regulator and low to turn it off.
4	PSI	Power Saving Mode. Connect a resistor from PSI to GND and detect voltage on R_{LG2} to select two phases or single-phase operating. Short this pin to ground for single-phase operation.
5	VID1	VID1 Input. This pin is used to adjust reference voltage.
6	VID0	VID0 Input. This pin is used to adjust reference voltage.
7	FS	Frequency selection Input. This pin is used to adjust switching frequency level.
8	CSP1	Positive Input of current sensing Amplifier for channel 1. This pin combined with CSN1 senses the inductor current of channel 1 through an RC network.
9	CSN1	Negative Input of current sensing Amplifier for channel 1. This pin combined with CSP1 senses the inductor current of channel 1 through an RC network.
10	CSP2	Positive Input of current sensing Amplifier for channel 2. This pin combined with CSN2 senses the inductor current of channel 2 through an RC network.
11	CSN2	Negative Input of current sensing Amplifier for channel 2. This pin combined with CSP2 senses the inductor current of channel 2 through an RC network.
12	GNDSNS	GND Sense. Negative node of the remote voltage sense.
13	VSNS	Output Voltage Sense for COT Regulator. The POK, UVP, and OVP circuits detect this signal on VSNS to report output voltage status.
14	VDROOP	Output Voltage Feedback Pin and Load Line Voltage Droop Setting Pin.
15	COMP	Compensation Pin for Stability.
16	POK	Power good indicator. Connect a resistor from POK to a pull-high voltage.
17	UGATE2	Upper Gate Driver Output for channel 2. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
18	BOOT2	External Power N-CH MOSFET Gate Drive Boost Input for channel 2. A 0.1μF to 1μF capacitor should be connected from PHASE2 to BOOT2 for power NMOSFET gate driving purposes. Ensure that C_{BOOT2} is placed near the IC.
19	PHASE2	Switch Node for Channel 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
20	LGATE2	Low-side Gate Driver Output for Channel 2. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
21	VCC	Power supply input. VCC needs to be connected to an external supply voltage between 4.5V to 5.5V.
22	GND	Ground. Device ground voltage reference.
23	LGATE1	Low-side Gate Driver Output for Channel 1. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
24	PHASE1	Switch Node for Channel 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE1 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
Exposed Pad	PGND	Ground. Tie this pin to the ground island/plane through the lowest impedance connection available.

Block Diagram



Typical Application Circuit



Note 5: The C_{FB} capacitor should be placed close to the VDROOP and GND.
Note 6: The C_S capacitor should be placed close to the VSNS and GND.
Note 7: R_{DROOP} =0Ω means disable Load Line (LL) function

Figure.1 Dual Phase Configuration

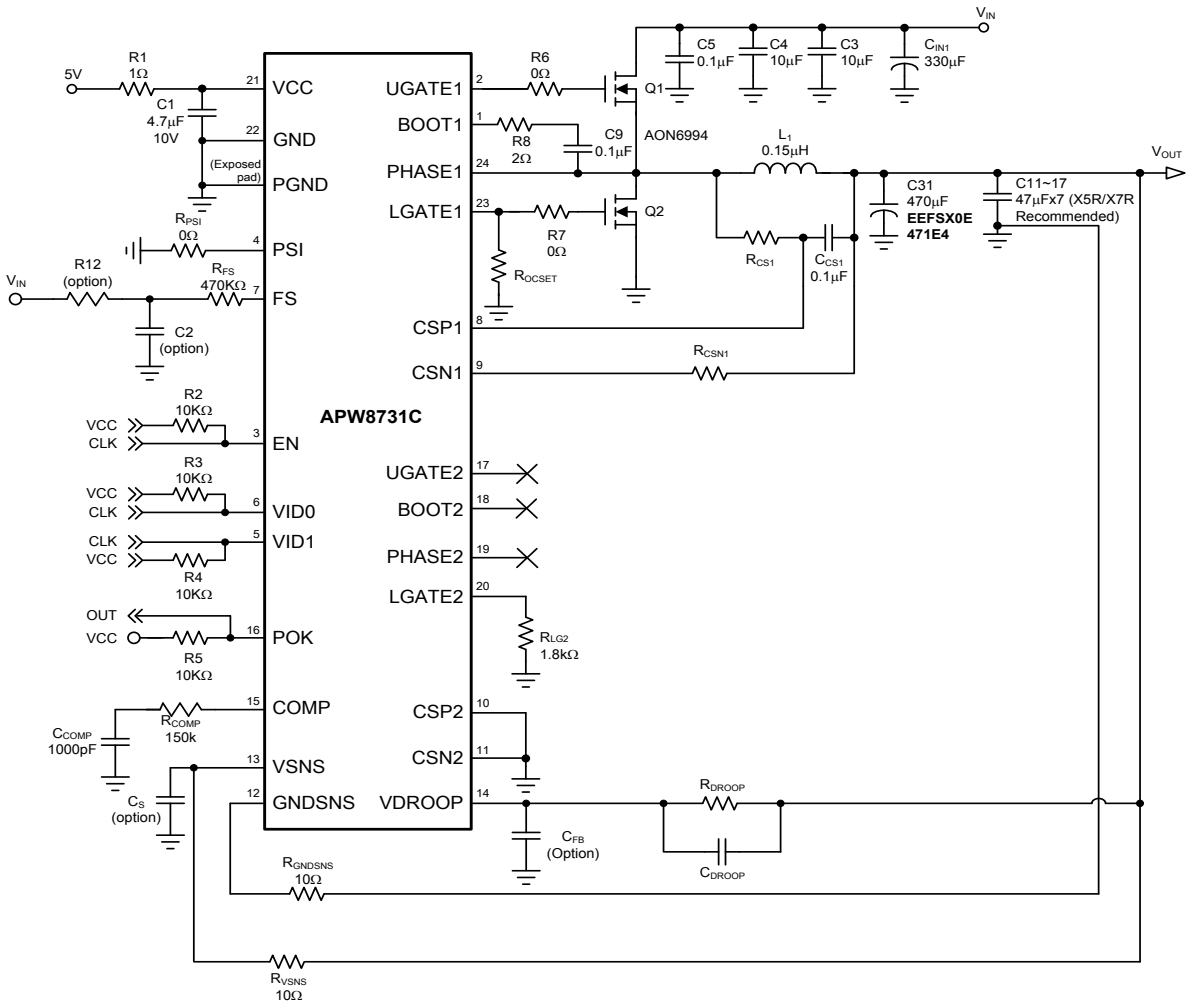
Table 1.

V_{OUT}	LL function	C_{DROOP}	R_{FS}	Rcomp	Ccomp	C_{OUT} (MLCC)	C_{OUT} (SP-Cap)
1.8V	enable	330pF	560KΩ	39KΩ	470pF	2x22µF	2x330µF
1.65V	disable	N.C	560KΩ	62KΩ	470pF	2x22µF	2x330µF
1.8V	enable	330pF	560KΩ	82KΩ	470pF	16x22µF	N.C
1.65V	disable	N.C	560KΩ	150KΩ	470pF	16x22µF	N.C

Table 2.

Designation	Description
C_{OUT} (SP-Cap)	330µF, 2.5V, ESR 4.5mΩ, Panasonic EEFSX0E331E4
L_1	0.22µH, DCR 7.2mΩ, Cyntec CMME041B-R22MS
L_2	0.22µH, DCR 7.2mΩ, Cyntec CMME041B-R22MS

Typical Application Circuit



Note 5: The C_{FB} capacitor should be placed close to the VDROOP and GND.
Note 6: The C_S capacitor should be placed close to the VSNS and GND.
Note 7: R_{DROOP} =0Ω means disable Load Line (LL) function

Figure.2 Single Phase Configuration

Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo fixed frequency with input voltage feed-forward. The device will turn on the high-side MOSFET for a fixed time. When the feedback voltage is lower than the reference voltage, controller will adjust the off time to stabilize output voltage ripple. COT regulators are widely used in the industry due to their ability to provide fast transient response without complex loop compensation. A major limitation of COT regulators is that the required output capacitance ESR. This architecture relies on the output filter capacitors effective series resistance (ESR) to act as a current sense resistor so the output ripple voltage provides the PWM ramp signal. In PFM operation, the on time generator controls high-side switches on-time. On time pulse width is inversely proportional to the input voltage and directly proportional to the output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The APW8731C does not use PWM controller to produce clock signal. The device uses the constant on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage and inversely proportional to input voltage. In PWM, the on-time calculation is written as below:

$$t_{ON} = 3\times10^{-12}\times R_{FS}\times\frac{V_{OUT}}{V_{IN}-0.5V}$$

Where:
R_{FS} is the resistor connected from FS pin to VIN.
Therefore, the PWM switching frequency is written as:

$$t_{ON} = \frac{D}{F_{SW}} \rightarrow F_{SW} = \frac{V_{OUT}/V_{IN}}{t_{ON}}$$

Where:
F_{SW} is the PWM switching frequency. APW8731C monitors FS voltage as input voltage to calculate on-time.

Setting the Output Voltage

The APW8731C is a dual-phase COT buck PWM controller. The phase1/2 pin of device is connected to a standard converter LC filter circuit for buck conversion. By comparing this sense voltage with an internally generated voltage reference, suitable regulation can be implemented to achieve the required output voltage. By selecting VID1/ VID0, the desired output voltage can be adjusted to the required level. The output voltage selection can refer to the below table:

EN	VID1	VID0	V_{OUT}(V)	POK
L	X	X	Discharge	L
H	L	L	0V (decay down mode)	H
H	L	H	1.1V	H
H	H	L	1.65V	H
H	H	H	1.8V	H

When the VID1 and VID0 simultaneously change to a lower set value (VID[1:0] is 00), the regulator output stops switching and becomes high impedance. The output naturally decays into the load; the regulator does not discharge the residual charge on the output capacitors. When the VID changes to a higher value (VID[1:0] is 01 or 10 or 11), the output voltage rises with a ramp-up slope of 20mV/μs (typical) depending on the ramp up time requirement and must ramp without discharging any residual charge on the output capacitors. The implementation of decay down is shown in timing chart.
The decay down function helps to save power when there are frequent transitions from high to low voltage. It prevents power loss due to the frequent charge and discharge cycles of large output capacitors.

VCC POWER ON RESET (POR)

The Power-On-Reset (POR) circuit compares the input voltage at VCC with the POR rising threshold (4.3V, typical) to ensure the input voltage is high enough for reliable operation. The 0.2V (typ.) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the POR rising threshold, startup begins. When the input voltage falls below the POR falling threshold, the controller turns off the converter.

Pulse-Frequency Modulation (PFM)

In PFM mode, an automatic switchover to pulse frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$t_{ON-PFM} = \frac{1}{F_{SW}}\times\frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is PWM mode's the nominal switching frequency.

Function Description (Cont.)

Pulse-Frequency Modulation (PWM)

In Forced-PWM mode, the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing, is disabled. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of V_{OUT}/V_{IN}. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced PWM mode is MOSFET useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Ultra-sonic Modulation (USM)

At light load condition and set up R_{LG2}=3.3kΩ (V_{PSI}<0.6V), the controller will enter the USM mode. Audible noise and EMI can be reduced in USM mode. The switching frequency in USM mode is lower than the one in PFM/PWM mode. In USM mode, the output current capacity can't support heavy load, so controller acquires output current information to judge when to enter the PFM mode to stabilize the output voltage.

Soft-start and Soft-stop

The soft-start sequence is when the VCC voltage exceeds the POR voltage threshold and the EN threshold exceeds 1.2V (delay 280 μs), after delay, the device initials a startup process and then ramps up the output voltage to the setting of output voltage. In the events of under-voltage, over-voltage, over-current, or shutdown, the chip will enable soft-stop function. The soft-stop function discharges the output voltages to the GND through an internal 6Ω switch.

Over Current Protection (OCP)

A resistor (R_{OCSET}) connected from the LG1 to GND programs the over-current trip level. The OCP threshold is determined when the voltage V_{OCP} on R_{OCSET} is developed by I_{OCSET} (120μA typical) during power on process. If the R_{OCSET} x I_{OCSET} exceeds 1V or the R_{OCSET} is floating, than the V_{OCP} will be the internal default value 1V.

The threshold of the OCP is therefore given by:

$$I_{OCPSET} \times R_{OCSET} = I_{L1} \times 8.7 \times 10^3 \times \frac{R_{DCR1}}{R_{CSN1}} + I_{L2} \times 8.7 \times 10^3 \times \frac{R_{DCR2}}{R_{CSN2}}$$

Assume, R_{DCR1} = R_{DCR2} , R_{CSN1} = R_{CSN2}

$$I_{OCP} = \frac{120 \times 10^{-6} \times R_{OCSET}}{8.7 \times 10^3} \times \frac{R_{CSN}}{R_{DCR}}$$

When the inductor current exceeds the OCP threshold, the device turns off both high-side and low-side MOSFET.

Over Voltage Protection (OVP)

The device provides an over-voltage protection function. When the VSNS pin exceeds 2.4V(typical), the over-voltage protection circuit turns off high-side and low-side MOSEFET and shuts down the device. The device remains in shutdown mode until the power is re-cycled or restart EN signal.

Over Temperature Protection (OTP)

A thermal shutdown function is implemented to prevent damages due to excessive heat. Typically the thermal shutdown threshold temperature is 150°C.When the thermal shutdown is triggered the device stops switching and output voltage re-start after the junction temperature cools by 30°C.

Under Voltage Protection (UVP)

This device provides under-voltage protection function. When V_{VSNS} is below the UVP threshold (50% of the reference voltage), the under-voltage protection circuit turns off high-side and low-side MOSEFET and shuts down the device. The device remains in shutdown mode until the power is re-cycled or restart EN signal. In addition, the UVP function does not work during soft start.

Automatic Phase Reduction (PSI)

The APW8731C features automatic phase reduction that turns off phase2 driver signal at light load condition and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range. The output current is sensed and mirrored to PSI pin as:

$$V_{PSI} = \frac{I_{OUT} \times R_{DCR}}{R_{CSN}} \times R_{PSI}$$

The APW8731C runs the LGATE2 sample-and-hold process during a 120 μs time frame before initialing startup. The device will setup the V_{LG2SET} voltage on the resistor connected from the LGATE2 to GND by internal current source I_{LG2SET} (240μA typical). When the sample and hold process on LGATE2 pin is end, the device memorizes V_{LG2SET} level and shuts down the current source, I_{LG2SET}, during normal operation.
The V_{LG2SET} is therefore given by:

$$V_{LG2SET} = I_{LG2SET} \times R_{LG2}$$

Function Description (Cont.)

When the R_{LG2} is not connected, meaning that the R_{LG2} is virtually near an infinite value, the sampling V_{LS2SET} voltage will outrun a preset upper threshold, the IC then determines this case as case 1. In case 1, the IC will either operates in single-phase mode with PFM at light load condition (eq. V_{PSI}<0.6V) or in dual-phase mode with PWM at heavy load condition (eq. V_{PSI}>1V). Several cases can be selected by a proper resistor on LGATE2 pin. The rest cases referred to case 2, 3, 4 are listed in below table, for your reference.

Table3. Operation mode selection

Case	R_{LG2}	V_{PSI}>1V	V_{PSI}<0.6V	De-bounce Time (μs)	
1	NC	A	B	A→B	B→A
				300	0
2	6.2KΩ		C	A→C	C→A
				300	0
3	3.3KΩ		D	A→D	D→A
				300	0
4	1.8KΩ	E	F	E→F	F→E
				0	0

A: Two Phases with PWM
B: Single Phase with PFM
C: Single Phase with PWM
D: Single Phase with Ultra-sonic PFM
E: Single Phase with PWM
F: Single Phase with PFM

Load Line Function

APW8731C features a load line function to virtually mimic a load line. The load line function decreases V_{OUT} voltage accordingly when load current increases. In order to control load line function, the APW8731C uses an RC network to sense inductor's current. The RC value should meet the following equation.

$L_X/R_{DCRX}=R_{CSX}*C_{CSX}$

The virtual load line resistance, R_{LL}, can be calculated by below equation:

$R_{LL}=\Delta V_{OUT}/\Delta I_{OUT} = K*(R_{DCR1}* R_{DROOP}/R_{CSN1})$

Where, K is an internal gain which is 1.

With the implementation of load line function, the V_{OUT} voltage drops according to load current , as shown as figure 3. The V_{OUT} voltage with load line activation can be calculated by below equation:

$V_{OUT}=V_{OUT\_nominal}-I_{OUT}*R_{LL}$

Load Line Function (Cont.)

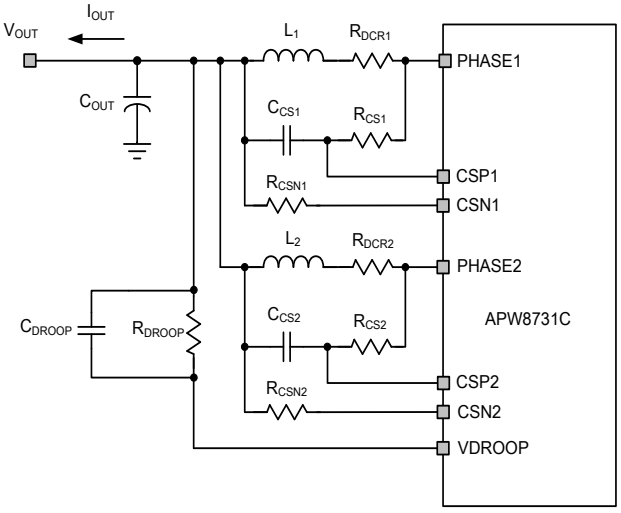


Figure 2. Load Line RC network.

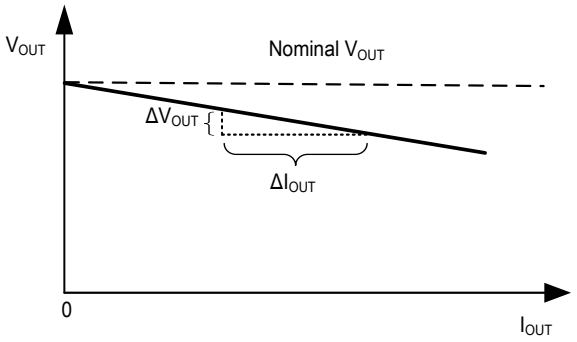


Figure 3. V_{OUT} Curve with Load Line Function

Power-OK Output

POK is an open-drain output, needing an external pullhigh resistor to VCC to provide the POK signal for system. The POK function is continuously monitoring the output voltage.When output voltage is greater than 85% of reference voltage and VCC voltage exceeds the POR voltage threshold and the EN threshold exceeds 1.2V, POK will get high.When the output voltage VOUT exceeds 2.4V or falls below 85% (typ.) of the target output voltage, POK signal will be pulled low and latched immediately.

Enable/Disable

An Enable POR function is designed to prevent wrong logic controls when the V_{EN} voltage is low. Pulling the V_{EN} above 1.2V will enable the driver output, and pulling V_{EN} below 0.6V will disable the driver output. If enable function is not used, connect EN to VCC for normal operation. When the IC is disabled, the supply current is reduced to less than 10μA.The EN pin cannot be left floating.

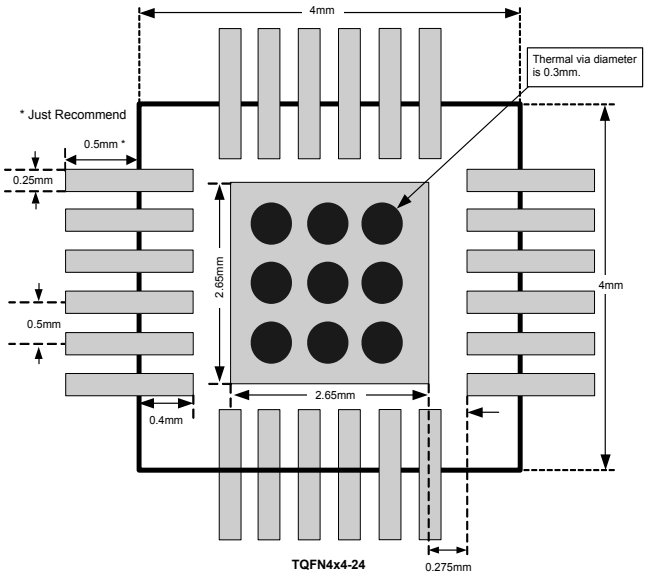
Application Information

Layout Consideration

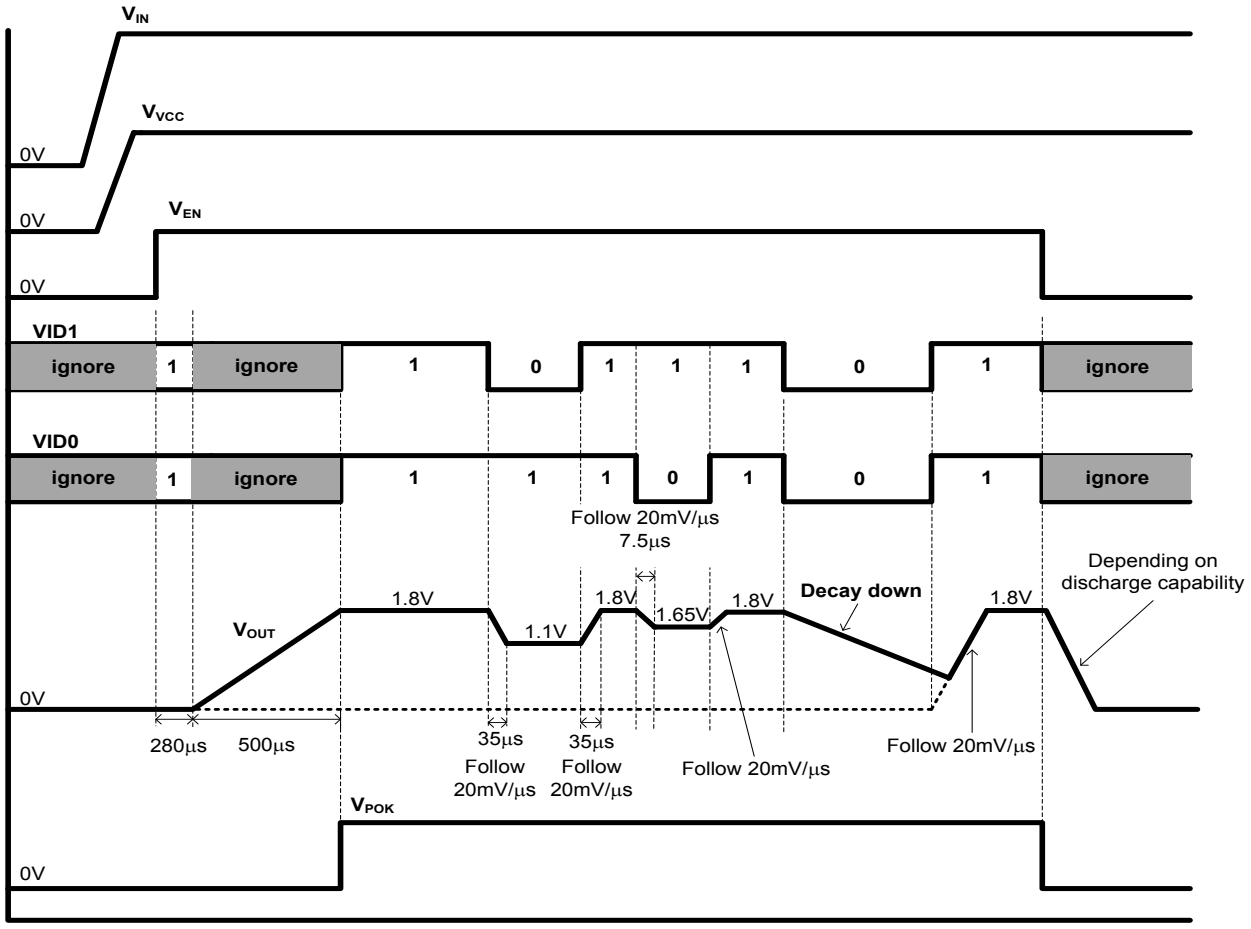
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN/VCC and GND. Connecting the capacitor and VIN/VCC/GND with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/VCC and GND to capacitor less than 2mm respectively is recommended.
2. Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance. The high-side power MOSFET and low-side power MOSFET and inductor should be placed as close as possible to minimize the noise coupling into other circuits and minimize losses.
3. All sensitive analog PCB traces and components (as PSI, VID0/1, FS, CSP1/2, CSN1/2, GNDSNS, VSNS, VDROOP, COMP) should be placed away from high voltage switching nodes (as PHASE1/2, LGATE1/2, UGATE1/2, or BOOT1/2 nodes) to avoid coupling. All sensitive PCB traces and components should be shielded with a ground planes. For other component limitations, refer to the notes in the Typical Application Circuit section.
4. The output capacitor should be placed close to circuit layout board load side.
5. PCB traces should be as wide as possible. (Not include signal line)
6. The PCB trace distance and width between PHASE1 and the positive pin of the output capacitor must be the same as the PCB trace between PHASE2 and the positive pin of the output capacitor.
7. Connect the negative pin of the output capacitor to the GNDSNS pin by using a dedicated PCB trace.
8. Connect the positive pin of the output capacitor to the VDROOP and VSNS pins individually by using a dedicated PCB trace.

Recommended Minimum Footprint

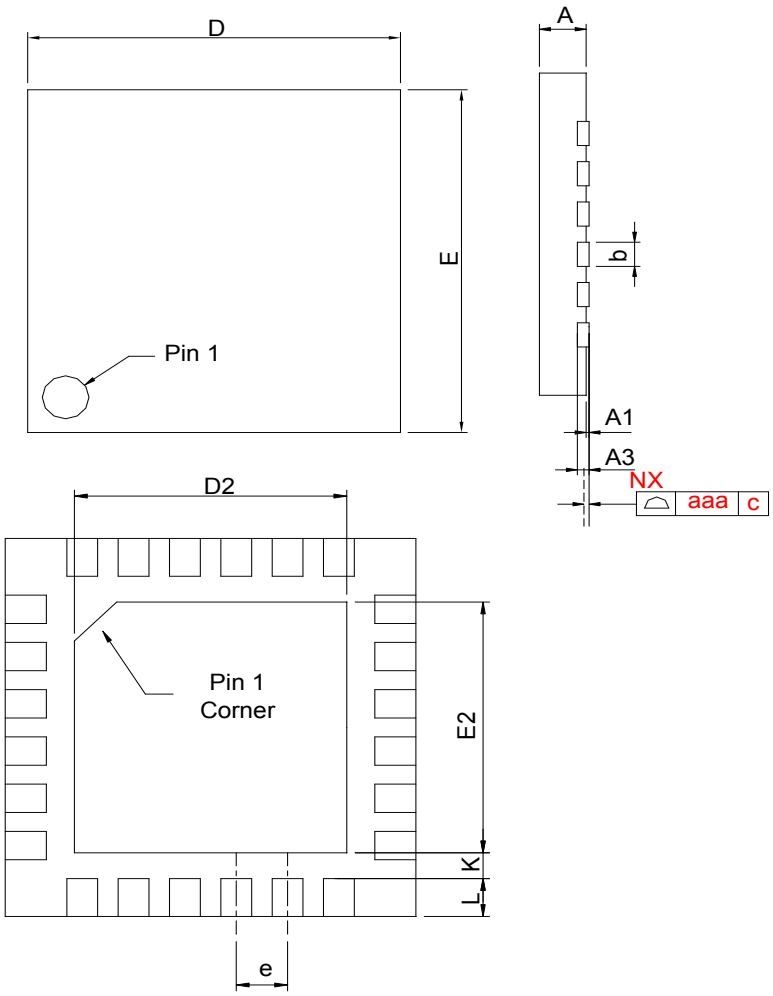


Timing Chart



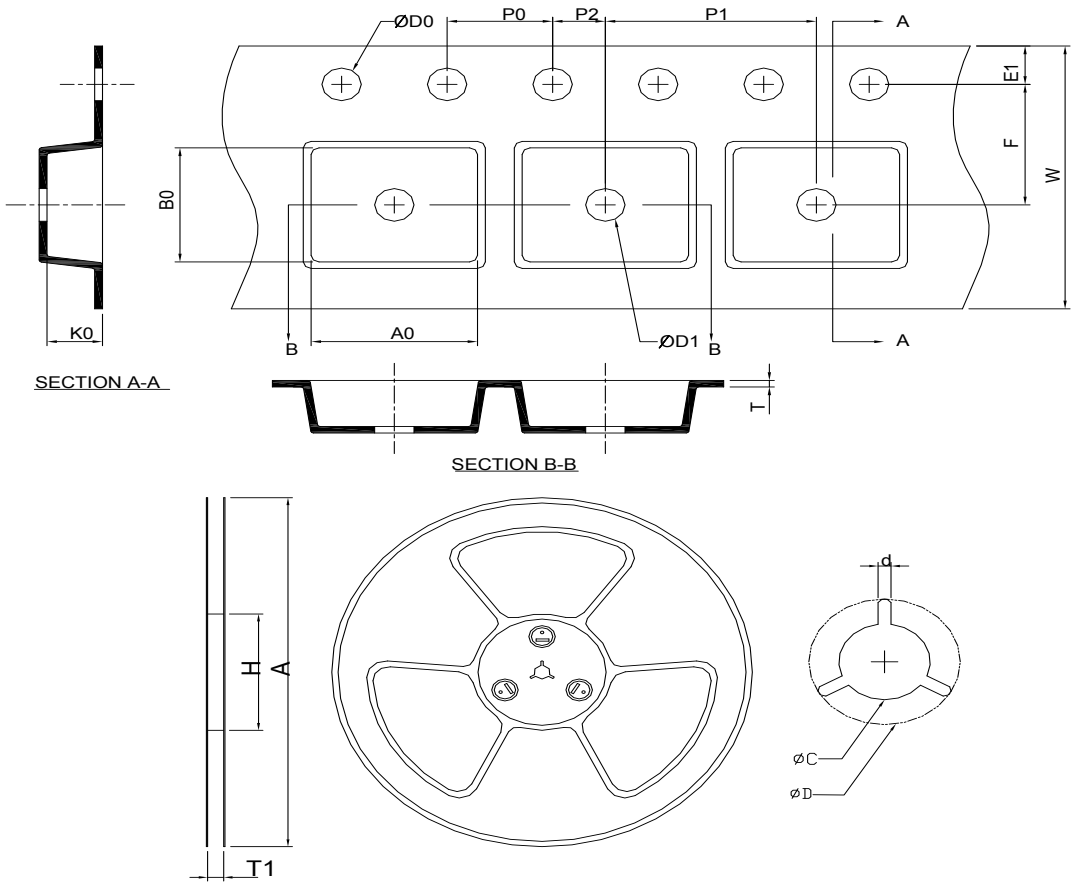
Package Information

TQFN4x4-24



SYMBOL	TQFN4*4-24					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.035	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.008	0.010	0.012
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.50	2.65	2.80	0.098	0.104	0.110
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.50	2.65	2.80	0.098	0.104	0.110
e	0.50 BSC			0.020BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20			0.008		
aaa	0.08			0.003		

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-24	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

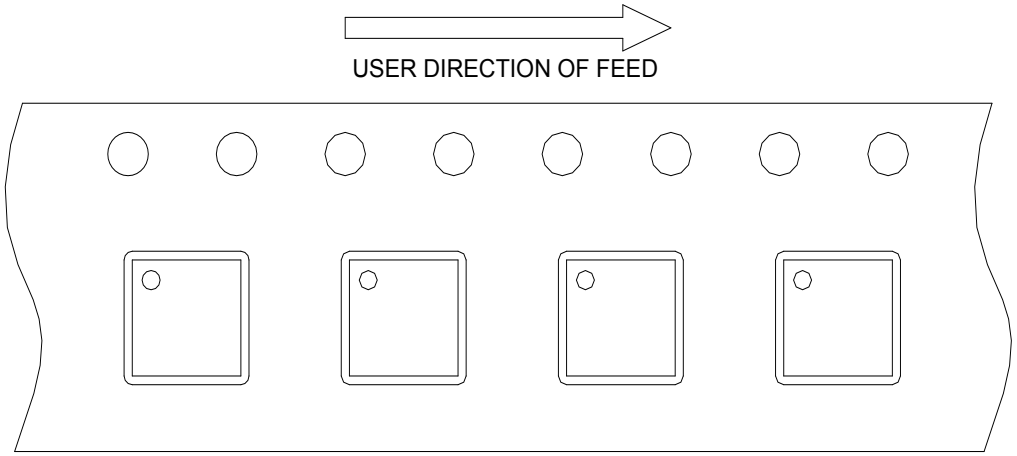
(mm)

Devices Per Unit

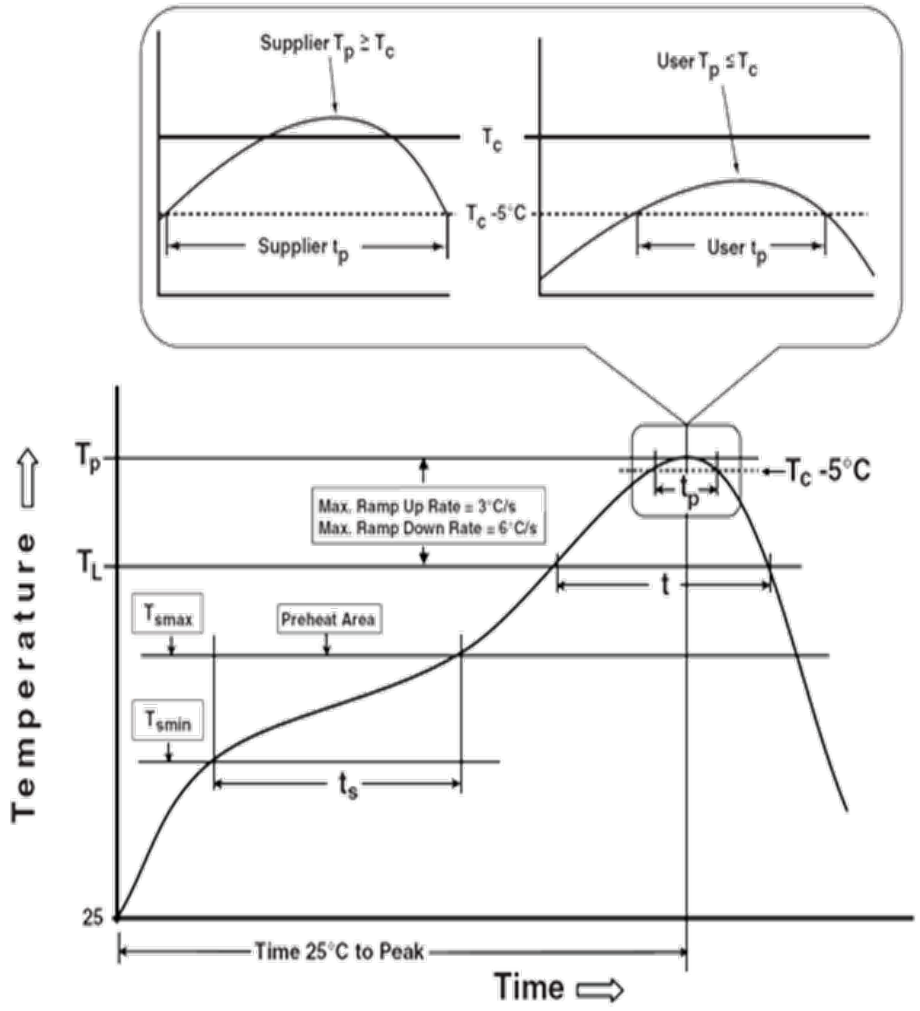
Package Type	Unit	Quantity
TQFN4x4-24	Tape & Reel	3000

Taping Direction Information

TQFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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