

## Features

- Wide Operating Range from +5.5V to +23V Input Voltages
- Power-On-Reset Monitoring on VIN at 4.2V ~ 4.4V range
- Built-in 100uA low quiescent current
- Support IOUT = 6A Application
- Built in PWM & PFM Control Schemes with COT architecture
- Built in Integrated Bootstrap Forward P-CH MOSFET
- APW8765B Fixed Switching Frequency from 500KHz
- APW8765C Fixed Switching Frequency from 750KHz
- APW8765B Fixed 3.3V VOUT REF voltage with  $\pm 0.6\%$  accuracy
- APW8765C Fixed 5.1V VOUT REF voltage with  $\pm 0.6\%$  accuracy
- Support Ultrasonic Mode selection on EN Pin
- Support built-in fixed Soft Start time 1.65mS
- Integrated 30m $\Omega$  N-Channel MOSFET For High Side MOS
- Integrated 15m $\Omega$  N-Channel MOSFET For Low Side MOS
- Built in Open-Drain Type POK function and EN control
- Built in 3.3V & 5.0 V / 100mA LDO and Switch-over MOSFET with PWM output
- UVP setting at 70% of VREF & OVP setting at 125% of VREF & Thermal Shutdown
- Built in Over Current Protection and Current Limit Protection using high-side MOSFET Rds(on) and low-side MOSFET Rds(on) sensing
- Flip-Chip VTQFN 3x3-12P with Lead Free & RoHS compliant

## General Description

The APW8765B/C is a 6A, synchronous buck converter with integrated 30m $\Omega$  High-Side MOSFET and 15m $\Omega$  Low-Side MOSFET. The APW8765B/C designed with a constant on-time control architecture can step down high voltage to accommodate low-voltage chipset for IMPV8 applications.

The APW8765B/C is equipped with an automatic PFM/PWM mode operation. At light load, the converter operates in the PFM mode to reduce the switching losses and provide high efficiency. At heavy load, the converter works in PWM mode and operates nearly at constant frequency for low-noise requirements.

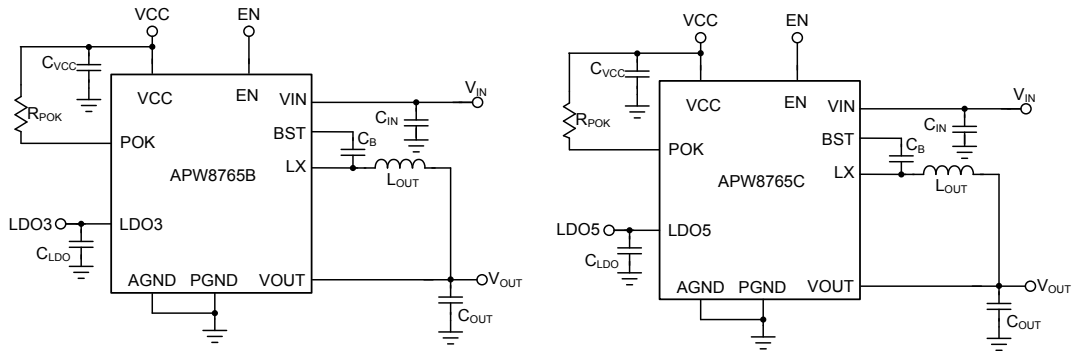
The APW8765B/C is also equipped with Power-on-reset, soft-start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature, over-current and current-limit) into a single package.

This device, available in VTQFN 3x3-12 package, provides a very compact system solution to minimize external components and PCB area.

## Applications

- Notebook
- Graphic card
- Motherboard

## Simplified Application Circuit

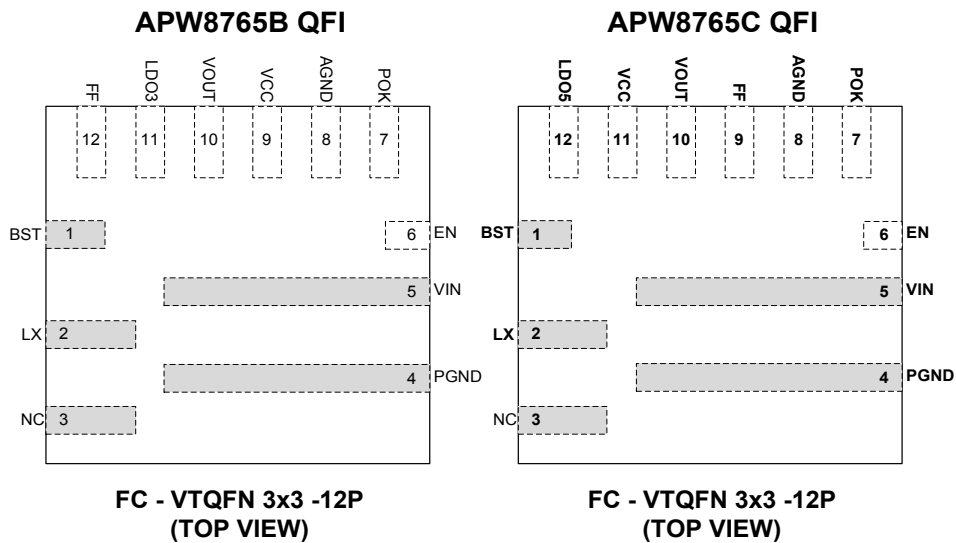


## Ordering and Marking Information<sup>(Note1)</sup>

<p>APW8765B/C</p>	<p>Package Code                  QF: VTQFN3x3-12                  Operating Ambient Temperature Range                  I: -40 to 85 °C                  Handling Code                  TR: Tape &amp; Reel                  Lead Free Code                  L: Lead Free Device      G: Halogen and Lead Free Device</p>		
<p>APW8765B/C QF :</p> <table border="1" style="display: inline-table; margin-right: 20px;"> <tr> <td>APW 8765B XXXXX</td> </tr> </table> <table border="1" style="display: inline-table;"> <tr> <td>APW 8765C XXXXX</td> </tr> </table>	APW 8765B XXXXX	APW 8765C XXXXX	<p>XXXXX - Date Code</p>
APW 8765B XXXXX			
APW 8765C XXXXX			

Note1: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration



## Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Rating	Unit	
$V_{IN}$	VIN Supply Voltage (VIN to AGND)	-0.3 ~ 27	V	
$V_{BOOT1}$	BOOT Supply Voltage (BOOT to LX)	$V_{LX}-0.3 \sim V_{LX}+7$	V	
$V_{GND}$	AGND to PGND	-0.3 ~ +0.3	V	
	All Other Pins (PGOOD , EN , VOUT , FF , LDO3 , LDO5 , VCC)	-0.3 ~ 7	V	
$V_{LX}$	LX Voltage (LX to GND)	>30ns pulse width <30ns pulse width	V	
$P_D$	Power Dissipation	Internally Limited	W	
$T_J$	Junction Temperature	150	°C	
$T_{STG}$	Storage Temperature	-65 ~ 150	°C	
$T_{SDR}$	Maximum Lead Soldering Temperature(10 Seconds)	260	°C	
$V_{ESD}$	Minimum ESD Rating(Note 3)	Human Body Mode	±2	kV
		MM Mode	0.2	kV

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3: The device is ESD sensitive. Handling precautions are recommended.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Junction-to-Ambient Resistance in free air (Note 4) – VTQFN2x3-12	45	°C/W

Note 4:  $\theta_{JA}$  is measured with the component mounted on a four-layer Anpec evaluation board in free air

## Recommended Operating Conditions (Note 5)

Symbol	Parameter	Range	Unit
$V_{IN}$	Converter Input Voltage	5.5 ~ 23	V
$I_{OUT}$	Converter Output Current	0 ~ 6	A
$L_{OUT}$	Converter Output Inductor	1.0 ~ 2.2	μH
$C_{IN}$	Converter Input Capacitor (MLCC)	20 ~ 30	μF
$C_{OUT}$	Converter Output Capacitor (MLCC)	44 ~ 66	μF
$T_A$	Ambient Temperature	-40 ~ 85	°C
$T_J$	Junction Temperature	-40 ~ 125	°C

Note 5: Refer to the typical application circuit

## Electrical Characteristics

Unless otherwise specified, these specifications apply over  $V_{IN}=19V$ ,  $V_{EN}=5V$  and  $T_A=-40$  to  $85$  °C. Typical values are at  $T_A=25$ °C.

Symbol	Parameter	Test Conditions	APW8765B/C			Unit
			Min	Typ	Max	
<b>INPUT VOLTAGE</b>						
$V_{IN}$	VIN POR Voltage Threshold	$V_{IN}$ Rising	4.2	4.3	4.4	V
	VIN POR Hysteresis		-	0.2	-	V
<b>REFERENCE VOLTAGE &amp; SOFT START</b>						
$V_{OUT}$	Reference Output Voltage	APW8765B	-	3.3	-	V
		APW8765C	-	5.1	-	V
	Reference Voltage Accuracy	$T_A = 25$ degree	-0.6	-	+0.6	%
$T_{SS}$	Soft Start Time	From EN high to PG high	-	1.65	-	ms
<b>VCC POR THRESHOLD</b>						
$V_{CC}$	VCC POR Voltage Threshold	$V_{IN}$ Rising	-	4.3	-	V
	VCC POR Hysteresis		-	0.2	-	V
<b>SUPPLY CURRENT</b>						
$I_{VIN}$	VIN Supply Current	At no switching	-	80	100	uA
$I_{VIN\_SD}$	VIN Shutdown Current	VIN = 19V , EN= L	-	60	80	uA
<b>SWITCHING FREQUENCY</b>						
$F_{OSC}$	Switching Frequency	APW8765B	-	0.5	-	MHz
		APW8765C	-	0.75	-	MHz
$T_{ON(min)}$	Minimum On Time		-	50	-	ns
$T_{OFF(min)}$	Minimum Off Time		-	200	-	ns
<b>ENABLE CONTROL</b>						
$V_H$	High Level Input Threshold Voltage	For EN	1.2	-	-	V
$V_L$	Low Level Input Threshold Voltage	For EN	-	-	0.4	V
	EN High Level at Ultrasonic Mode	For EN	-	-	1.7	V
	EN Low Level at Normal	For EN	2.3	-	-	V
$T_{USM}$	Ultrasonic Mode operation period		-	32	-	us
$I_{LKG}$	Input Leakage Current at EN	$V_{EN} = 5.0V$	-	1.0	-	uA
<b>INTERNAL POWER SWITCH</b>						
$R_{DS(ON)H}$	VNN NMOS_HI ON Resistance	$V_{CC}=5V$	-	30	-	mΩ
$R_{DS(ON)L}$	VNN NMOS_LO ON Resistance	$V_{CC}=5V$	-	15	-	mΩ

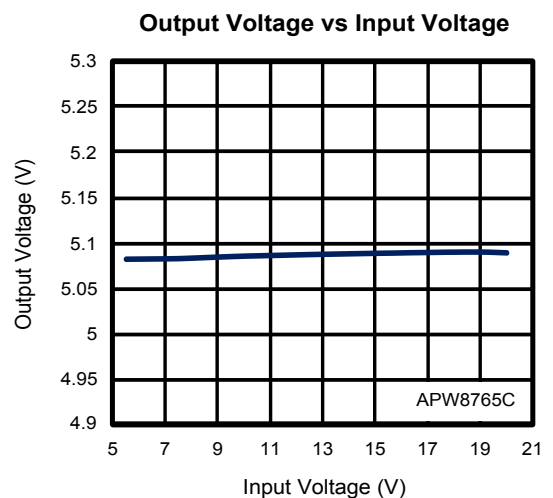
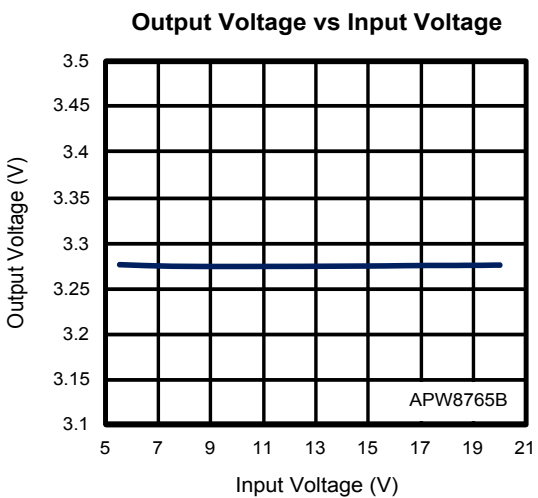
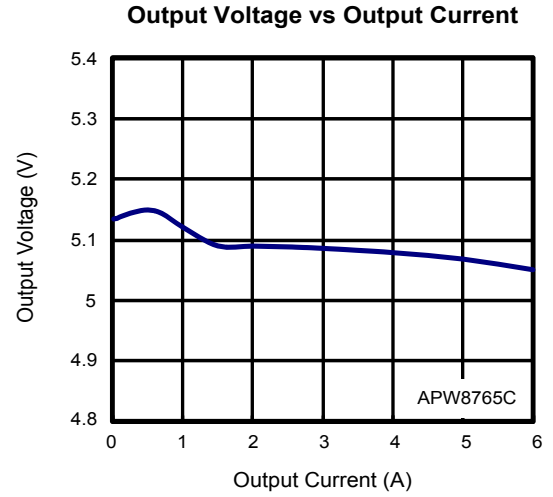
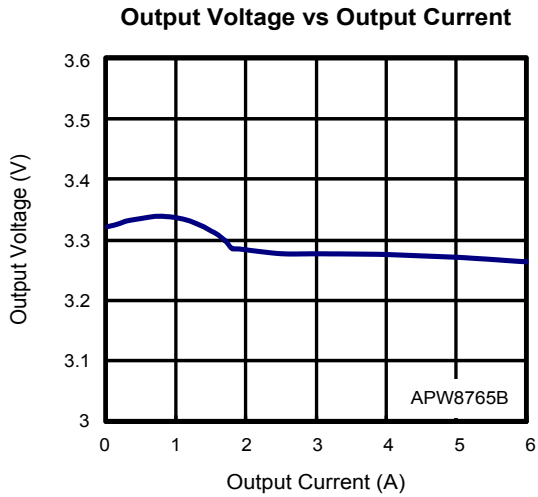
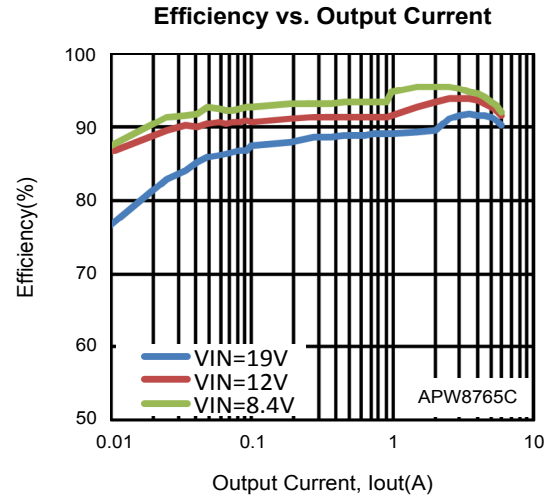
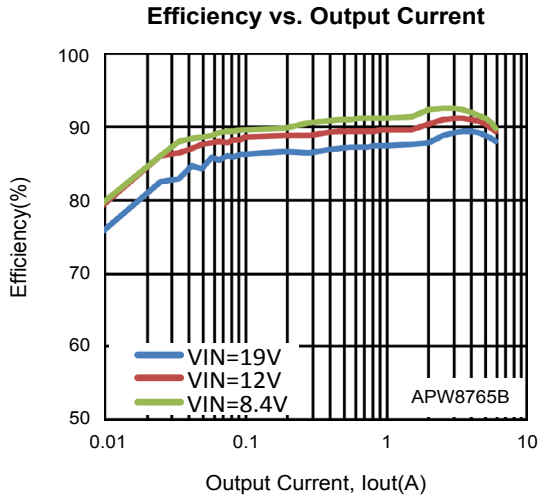
## Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over  $V_{IN}=19V$ ,  $V_{EN}=5V$  and  $T_A=-40$  to  $85$  °C. Typical values are at  $T_A=25$ °C.

Symbol	Parameter	Test Conditions	APW8765B/C			Unit
			Min	Typ	Max	
<b>LDO REGULATOR</b>						
$V_{LDO3}$	LDO Regulator	APW8765B	3.23	3.3	3.36	V
$V_{LDO5}$		APW8765C	4.9	5	5.1	V
	LDO Load Regulation	$V_{IN} = 19V, I_{OUT} = 10m\sim 100mA$	-	2	-	%
$I_{LDO\_limit}$	LDO Current Limit		150	200	300	mA
	LDO Switch bypass R	ILDO =50mA	-	0.8	-	Ω
<b>POWER-OK INDICATOR</b>						
$V_{POK}$	POK Threshold (OTP occur, POK always go low)	$V_{OUT} / V_{REF}$ , POK go high from Lower	85	90	95	%
		Hysteresis	-	5	-	%
		$V_{OUT} / V_{REF}$ , POK go low from Normal	120	125	130	%
	POK Leakage Current		-	0.1	1	uA
	POK High to Low Debounce Time		-	15	-	us
	EN Low to PG Low Delay		-	1	-	us
<b>CURRENT LIMIT &amp; OVER CURRENT PROTECTION</b>						
$I_{LIM\_P}$	High side Current Limit		-	14	-	A
$I_{LIM\_N}$	Low side Current Limit		-	9	-	A
	High Side Over Current Protection		-	20	-	A
<b>PROTECTION</b>						
$V_{OVP}$	Over Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	120	125	130	%
	Over Voltage Protection delay time		-	5	-	us
$V_{UVP}$	Under Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	65	70	75	%
	Under Voltage Protection delay time		-	10	-	us
$T_{OTP}$	OTP Rising Threshold		-	150	-	°C
	OTP Hysteresis		-	30	-	°C

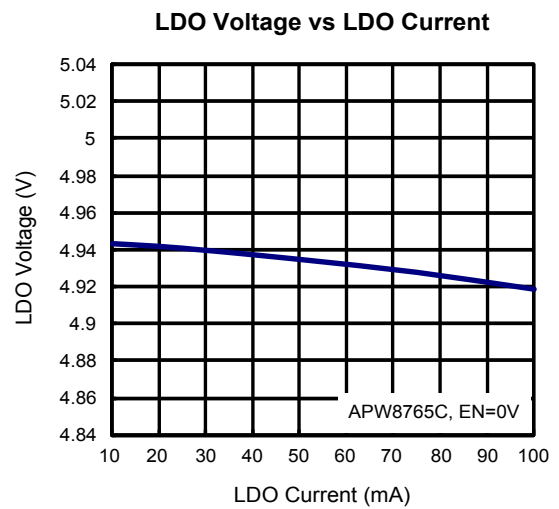
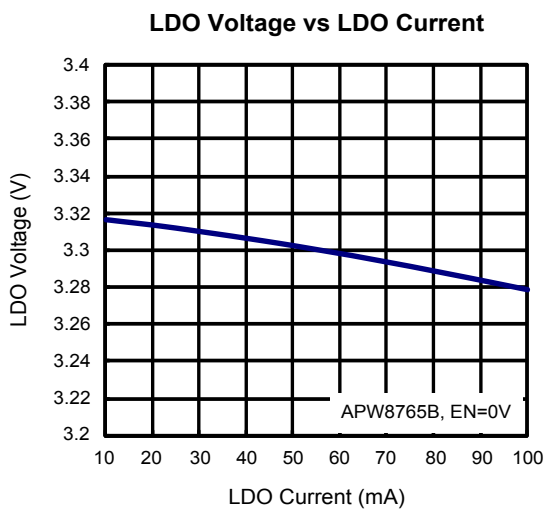
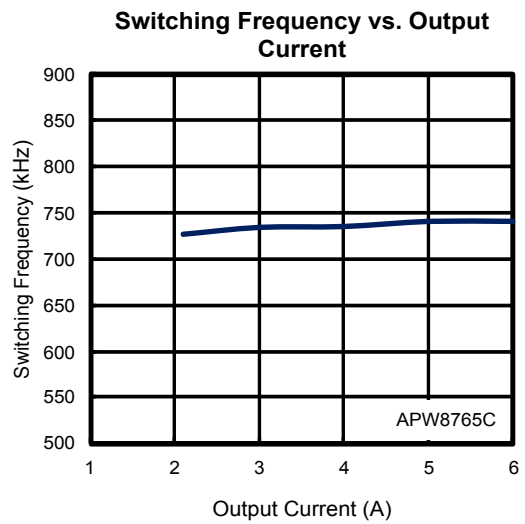
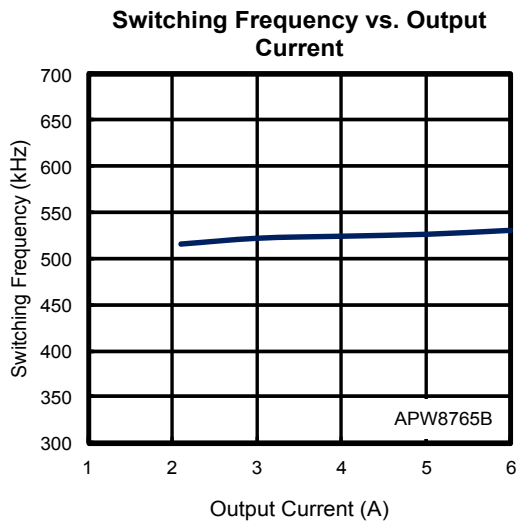
## Typical Operating Characteristics

Refer to the typical application circuit. The test condition is  $V_{IN}=19V$ ,  $T_A=25^\circ C$  unless otherwise specified.



## Typical Operating Characteristics (Cont.)

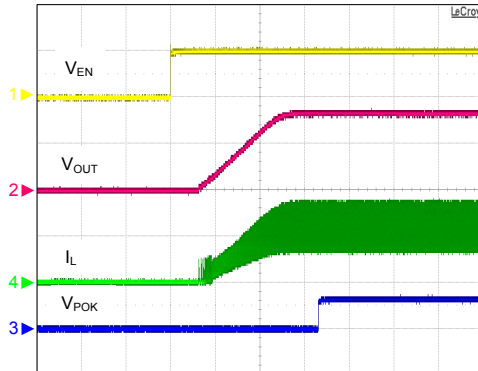
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## Operating Waveforms

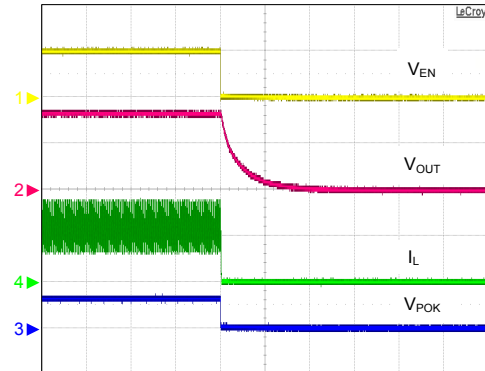
Refer to the typical application circuit. The test condition is  $V_{IN}=19V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

### Enable



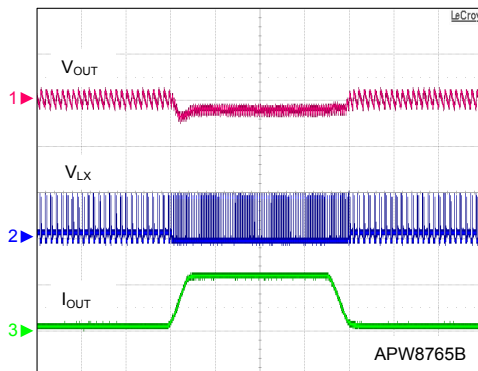
CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 2V/Div, DC  
 CH3:  $V_{POK}$ , 5V/Div, DC  
 CH4:  $I_L$ , 5A/Div, DC  
 TIME: 500 $\mu$ s/Div

### Shutdown



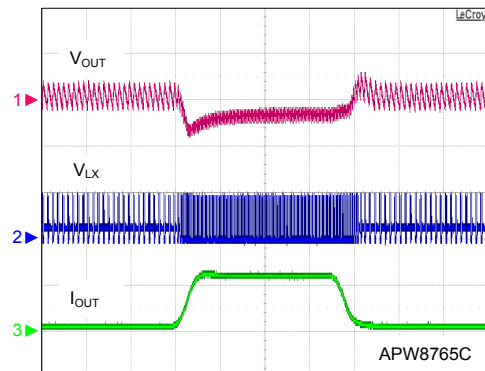
CH1:  $V_{EN}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 2V/Div, DC  
 CH3:  $V_{POK}$ , 5V/Div, DC  
 CH4:  $I_L$ , 5A/Div, DC  
 TIME: 100 $\mu$ s/Div

### Load Transient



CH1:  $V_{OUT}$ , 200mV/Div, AC  
 CH2:  $V_{LX}$ , 20V/Div, DC  
 CH3:  $I_{OUT}$ , 5A/Div, DC  
 TIME: 50 $\mu$ s/Div

### Load Transient



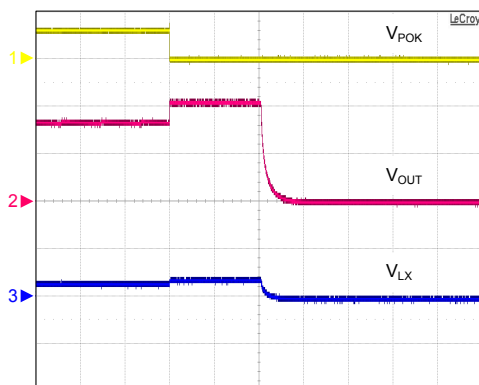
CH1:  $V_{OUT}$ , 200mV/Div, AC  
 CH2:  $V_{LX}$ , 20V/Div, DC  
 CH3:  $I_{OUT}$ , 5A/Div, DC  
 TIME: 50 $\mu$ s/Div



## Operating Waveforms (Cont.)

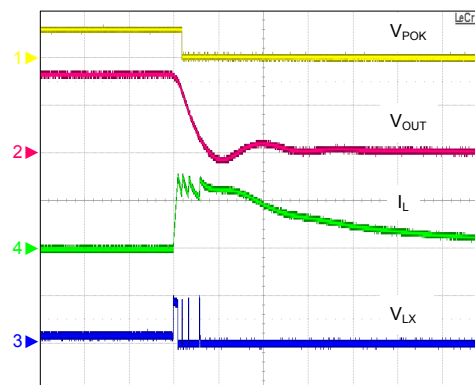
Refer to the typical application circuit. The test condition is  $V_{IN}=19V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

### Over Voltage Protection



CH1:  $V_{POK}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 2V/Div, DC  
 CH3:  $V_{LX}$ , 10V/Div, DC  
 TIME: 50ms/Div

### Under Voltage Protection



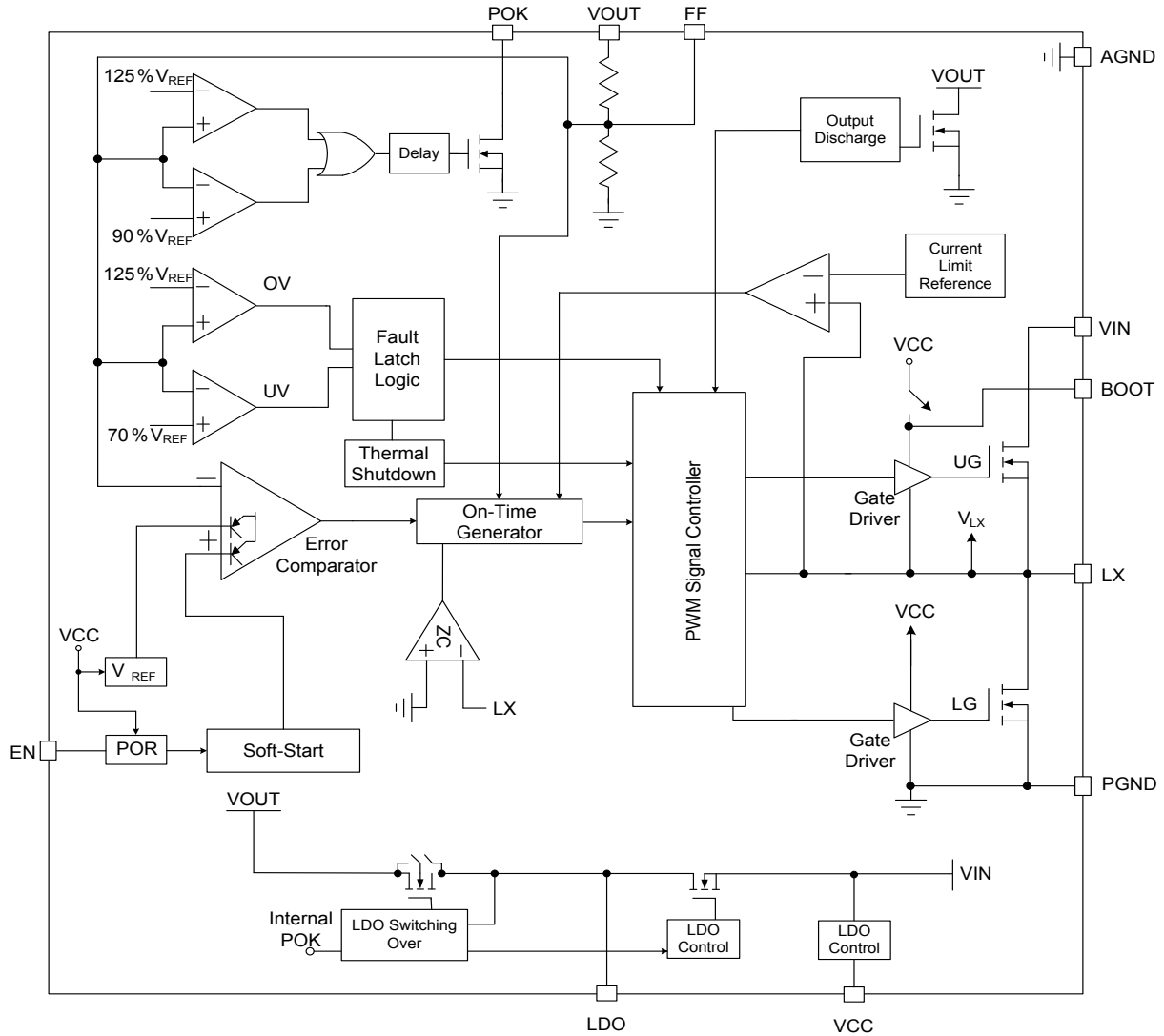
CH1:  $V_{POK}$ , 5V/Div, DC  
 CH2:  $V_{OUT}$ , 2V/Div, DC  
 CH3:  $V_{LX}$ , 20V/Div, DC  
 CH4:  $I_L$ , 10A/Div, DC  
 TIME: 10 $\mu$ s/Div

## Pin Descriptions

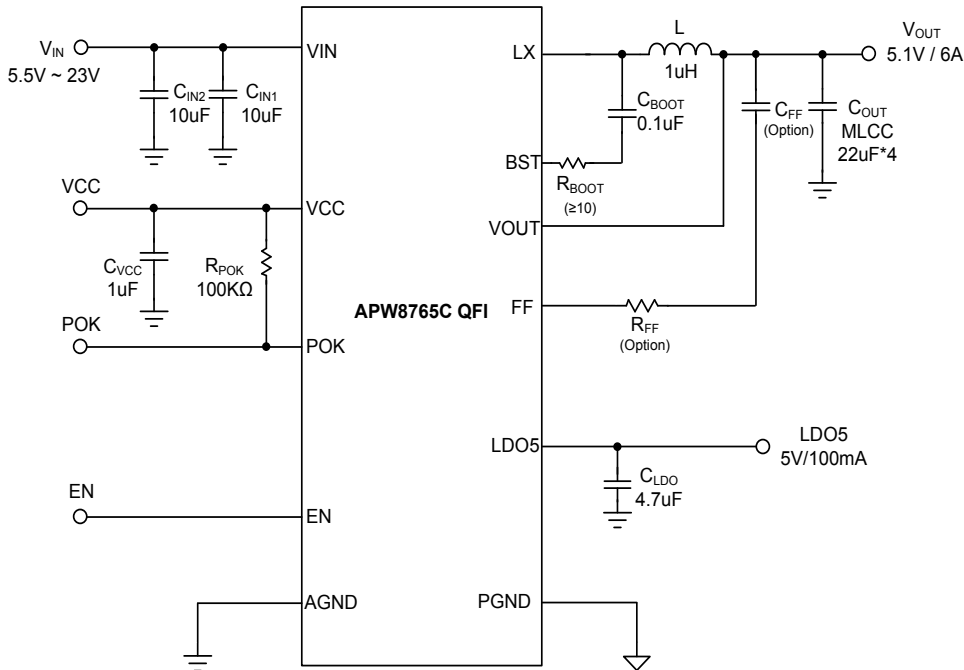
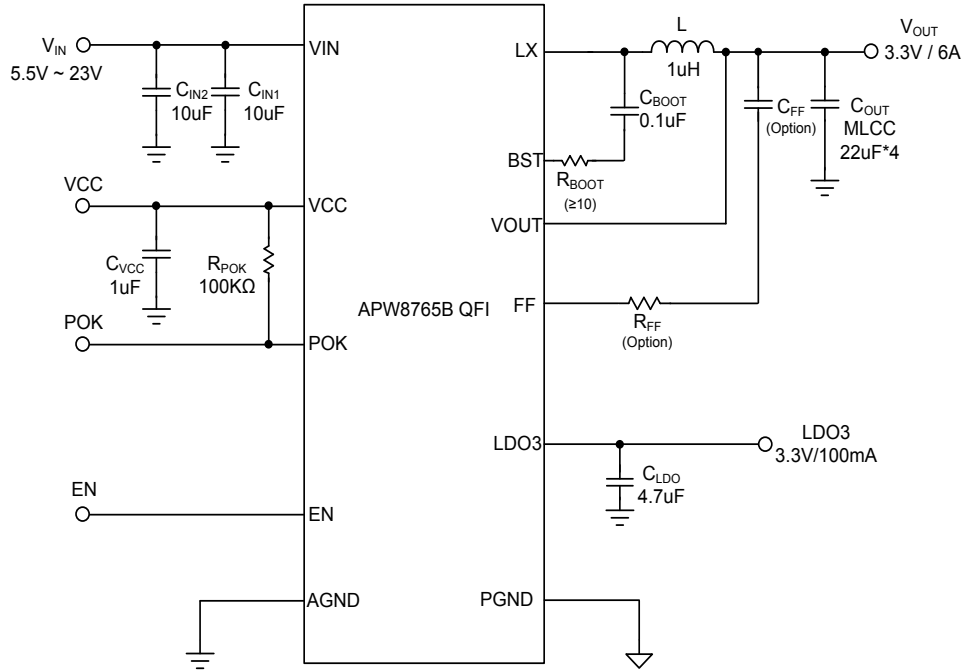
PIN			FUNCTION
APW 8765B	APW 8765C	NAME	
1	1	BST	High-side Gate Driver Supply Voltage Input. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
2	2	LX	Power Switching Output. The SW is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
3	3	NC	No connection.
4	4	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers.
5	5	VIN	Battery Voltage Input. The APW8765B/C operates from a +5.5V to +23V input rail. Must be closely decoupled to GND with two 10 $\mu$ F or greater ceramic capacitor.
6	6	EN	PWM enable pin. Logic high enables the PWM output. Logic low disables the PWM output. EN pin also be used to set Ultrasonic mode. When EN is between 1.2V and 1.7V, it will enter the Ultrasonic mode. If EN is higher than 2.3V, then it enters the normal mode. Do not float this pin.
7	7	POK	Power good indicator. POK is an open-drain output used to indicate the status of the PWM output voltage. Connect a resistor from POK to a pull-high voltage.
8	8	AGND	Signal ground for this IC .
9	-	VCC	5V Linear Regulator Output for internal control circuit. And VCC to GND with a 1.0 $\mu$ F ceramic capacitor for stability.
-	9	FF	Output Feedforward pin. Connect RC network from the output to this pin.
10	-	VOUT	Output Voltage Feedback Pin. This pin is connected to the output voltage. The pin also provide the bypass input for internal LDO3.
-	10	VOUT	Output Voltage Feedback Pin. This pin is connected to the output voltage. The pin also provide the bypass input for internal LDO5.
11	-	LDO3	3.3V Linear Regulator Output. LDO can provide 100mA current for external load. Bypass to GND with a minimum of 4.7 $\mu$ F ceramic capacitor for stability.
-	11	VCC	5V Linear Regulator Output for internal control circuit. And VCC to GND with a 1.0 $\mu$ F ceramic capacitor for stability.
12	-	FF	Output Feedforward pin. Connect RC network from the output to this pin.
-	12	LDO5	5V Linear Regulator Output. LDO can provide 100mA current for external load. Bypass to GND with a minimum of 4.7 $\mu$ F ceramic capacitor for stability.

## Block Diagram

APW8765B/C



## Typical Application Circuit



## Function Descriptions

### Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 200ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

### Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where  $F_{SW}$  is the nominal switching frequency of the converter in PWM mode. Similarly, the on-time of ultrasonic mode is the same with PFM mode. The description of ultrasonic mode will be illustrated later.

The load current at handoff from PFM to PWM mode is given by:

$$\begin{aligned} I_{LOAD(PFM \text{ to } PWM)} &= \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM} \\ &= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}} \end{aligned}$$

### Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if the enable pin is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.3V, typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 4.1V (typical), the POR disables the chip.

### EN Pin Control

When  $V_{EN}$  is above the EN high threshold (1.2V, minimum), the converter is enabled. When  $V_{EN}$  is below the EN low threshold (0.4V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC. When EN is between 1.2V and 1.7V, the IC will enter the Ultrasonic mode. The unique ultrasonic mode maintains the switching frequency above 32kHz, which eliminates noise in audio application.

### Power-Up Control Logics

Part.	EN	VCC	VOUT	LDO 5V	LDO 3V3
APW8765B	ON	ON	ON	X	ON
	OFF	ON	OFF	X	ON
APW8765C	ON	ON	ON	ON	X
	OFF	ON	OFF	ON	X

### Soft-Start

The APW8765B/C integrates soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage.

During soft-start stage before the POK pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the soft start voltage equal the VOUT voltage. This will ensure the output voltage starts from its existing voltage level.

In the event of under-voltage, over-voltage, over-temperature or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages by low side turns MOSFET on linearly.

### Power OK Indicator

POK is actively held low in shutdown and standby. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 90% to 125% of the converter reference voltage. When the output voltage has to stay within this window, POK signal will become high. When the output voltage outruns 90% or 125% of the target voltage, POK signal is pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

### Under-Voltage Protection (UVP)

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the VOUT voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under voltage threshold, the under voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 3 $\mu$ s de-bounce time, the device turns off both high side and low-side MOSEFET with latched. Toggling EN pin to low or recycling VIN will clear the latch and bring the chip back to operation.

## Function Descriptions (Cont.)

### Over-Voltage Protection (OVP)

The over voltage function monitors the output voltage by VOUT pin. Should the VOUT voltage increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over voltage protection comparator will turn off the power MOSFET and shut down the IC. Once an over-voltage fault condition is set, it can only be reset by toggling EN or VIN power-on-reset signal.

### Current Limit and Over-Current Protection (OCP)

The APW8765B/C uses the high-side MOSFET's  $R_{DS(ON)}$  and the low-side MOSFET's  $R_{DS(ON)}$  of the synchronous rectifier as a current-sensing element. The high side current limit circuit employs a "peak" current-sensing algorithm, and the Low side current limit circuit employs a "valley" current-sensing algorithm(See Figure 1).

If the magnitude of the current-sense signal at LX pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.

The PWM controller uses the low-side MOSFETs on-resistance  $R_{DS(ON)}$  to monitor the current for protection against shorted outputs. The MOSFET's  $R_{DS(ON)}$  is varied by temperature and gate to source voltage, the user should determine the maximum  $R_{DS(ON)}$  in manufacture's datasheet. The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at LX. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

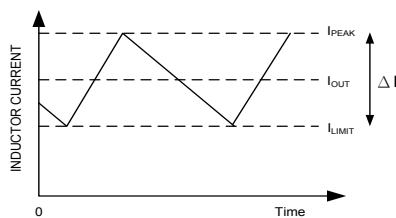


Figure 1. Current Limit algorithm

An over-current condition will shut down the device, the VOUT voltage is also discharged to the GND by an internal resistor, requiring a VIN POK or EN re-enable again to restart IC.

### Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature  $T_{OTP}$ , the IC will enter the over temperature protection state that suspends the PWM, which forces the UG and LG gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP designed with a 30°C hysteresis lowers the average  $T_J$  during continuous thermal overload conditions, which increases lifetime of the APW8765B/C.

### Linear Regulator

The LDO regulators can supply up to 100mA for external loads. Bypass to GND with a minimum of 4.7uF ceramic capacitor for stability. In APW8765B/C, the VLDO is fixed 3.3V / 5V in standby mode. When PWM output voltage is over its bypass threshold (PWM is 3V / 4.7V), the internal LDO to VOUT switchover is active. These actions change the current path to power the loads from the PWM regulator voltage, rather than from the internal linear regulator. This LDO is not control by EN.

## Application Information

### Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, IRIPPLE, and affects the load transient response.

Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the switching frequency of the regulator.

Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current.

Increasing the switching frequency (FSW) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage.

A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

### Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff, the output voltage ripple includes the capacitance voltage drop  $\Delta V_{C_{OUT}}$  and ESR voltage drop  $\Delta V_{ESR}$  caused by the AC peak-to-peak inductor's current. These two voltages can be represented by.

$$\Delta C_{OUT} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1 $\mu$ F) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

### Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately  $I_{OUT}/2$ , where  $I_{OUT}$  is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

### Thermal Consideration

Because the APW8765B/C build-in high-side and low-side MOSFET, the heat dissipated may exceed the maximum junction temperature of the part in applications. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance. To avoid the APW8765B/C from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The main power dissipated by the part is approximated:

$$P_{UPPER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})D + 0.5 (I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{LOWER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})(1 - D)$$

$I_{OUT}$  is the load current

TC is the temperature dependency of  $R_{DS(ON)}$

$F_{SW}$  is the switching frequency

$t_{SW}$  is the switching interval

D is the duty cycle

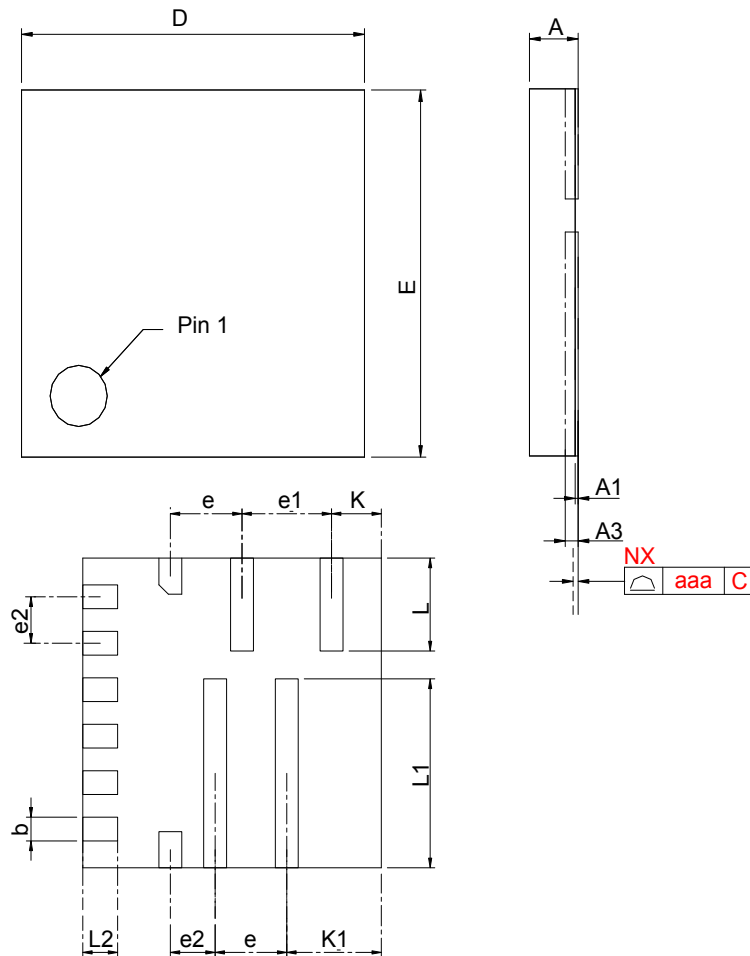
Note that both internal MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching interval,  $t_{SW}$ , is the function of the reverse transfer capacitance  $C_{RSS}$ . The (1+TC) term factors in the temperature dependency of the  $R_{DS(ON)}$ , and can be extracted from the " $R_{DS(ON)}$  vs. Temperature" curve of the power MOSFET. In APW8765B/C case, the  $R_{DS(ON)}$  is about 30m $\Omega$  from specification table.





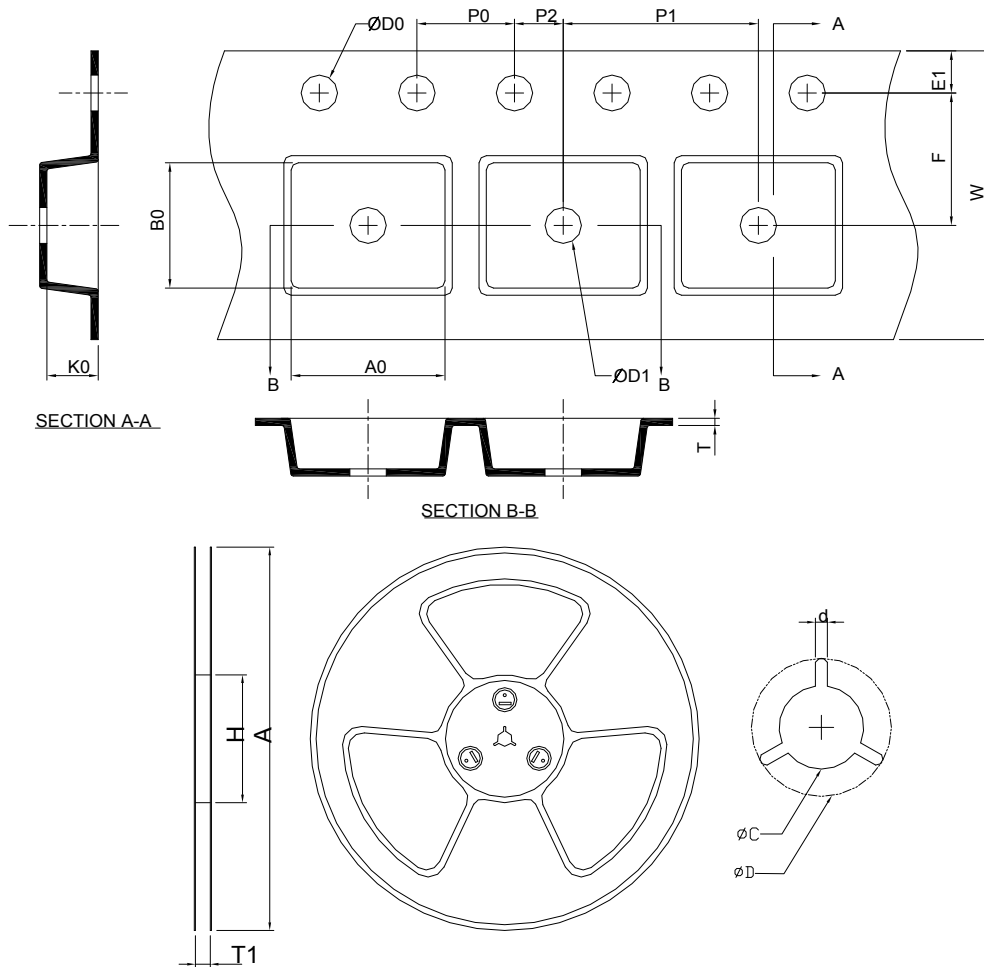
## Package Information

VTQFN3x3-12P



SYMBOL	VTQFN3*3-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.10	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.72 BSC		0.028BSC	
e1	0.90 BSC		0.035BSC	
e2	0.45 BSC		0.018 BSC	
L	0.80	1.00	0.031	0.039
L1	1.73	1.93	0.068	0.076
L2	0.25	0.45	0.010	0.018
K	0.50 BSC		0.020 BSC	
K1	0.95 BSC		0.037 BSC	
aaa	0.08		0.003	

## Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN 3*3	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	0.70±0.10

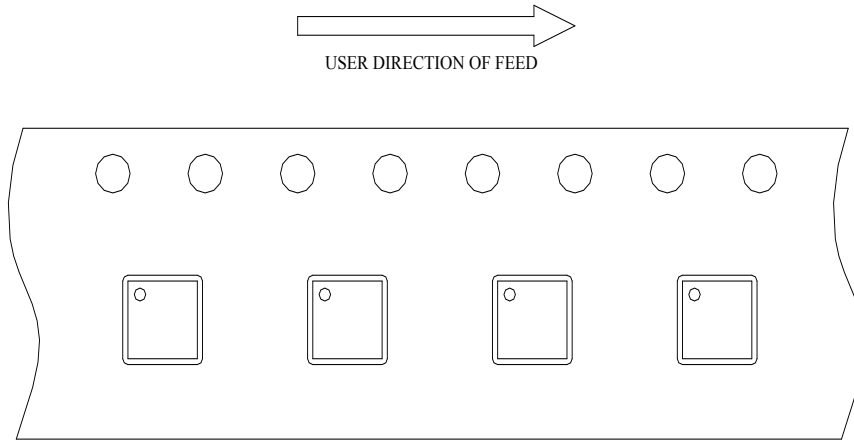
(mm)

## Devices Per Unit

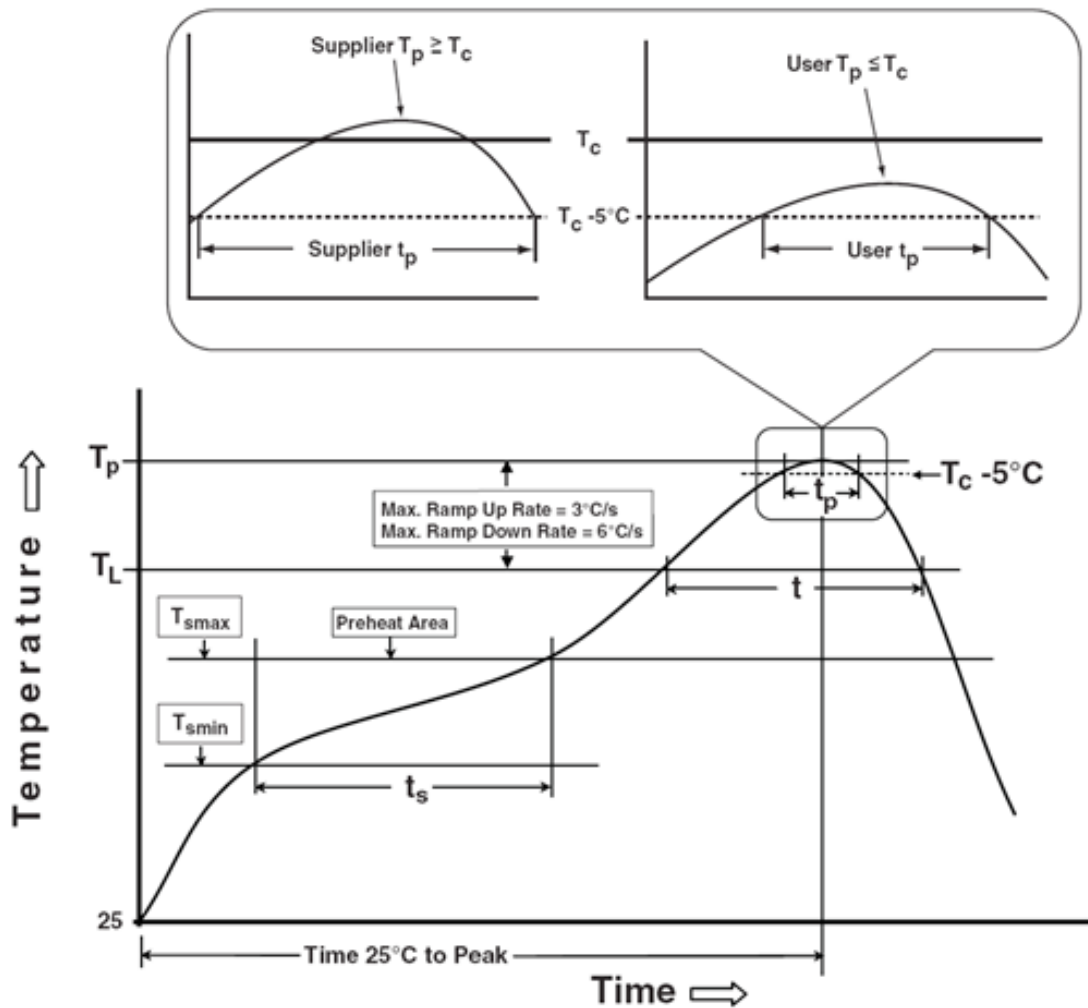
Package type	Packing	Quantity
VTQFN3x3	Tape & Reel	3000

## Taping Direction Information

VTQFN3x3-12P



## Classification Profile



## Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup>	
	<350	>350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup>		
	<350	350-2000	>2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

## Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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## Customer Service

### **Anpec Electronics Corp.**

Head Office :

No.6, Dusing 1st Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,

Sindian City, Taipei County 23146, Taiwan

Tel : 886-2-2910-3838

Fax : 886-2-2917-3838