APW8827

3A 5V 1MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
  - Automatic Skip/PWM Mode Operation
- **Integrated 75mΩ High side 65mΩ Low Side MOSFET**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VIN**
- **Integrate Soft Start and Output Discharge**
- **Over-Temperature Protection**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **Small SOT-23-6 ,TDFN2x2-8 and VTDFN2x2-8 packages**
- **Lead Free and Green Devices Available (RoHS compliant)**

General Description

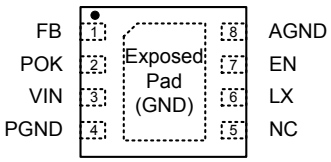
APW8827 is a 3A synchronous buck converter with integrated 75mΩ high side and 65mΩ low side power MOSFETs. The APW8827 design with a current-mode control scheme, can convert wide input voltage of 2.9V to 5.5V to provide excellent output voltage regulation.
The APW8827 is equipped with an automatic Skip/PWM mode operation. At light load, the IC operates in the Skip mode to reduce the switching losses. At heavy load, the IC works in PWM mode.
The APW8827 is also equipped with Power-on-reset, soft start, Output Discharge, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.
This device, available TDFN2x2-8, VTDFN2x2-8 and SOT-23-6 provide a very compact system solution external components and PCB area.

Applications

- **Notebook Computer & UMPC**
- **LCDMonitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Portable Instrument**

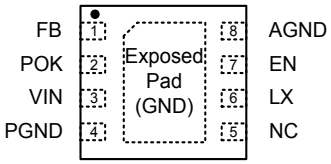
Pin Configuration

APW8827



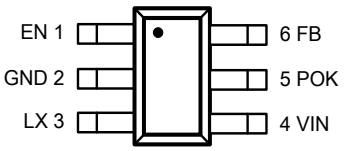
TDFN2x2-8
(TOP VIEW)

APW8827



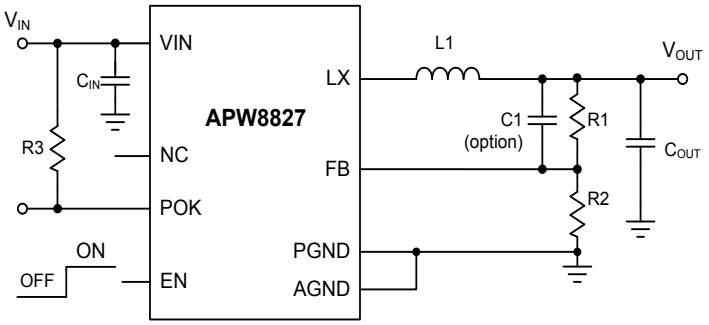
VTDFN2x2-8
(TOP VIEW)

APW8827

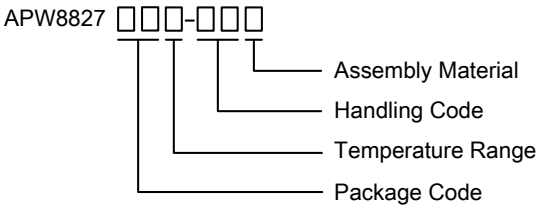


SOT23-6
(Top View)

Simplified Application Circuit



Ordering and Marking Information



Package Code
QB : TDFN-2x2-8 C: SOT23-6 QF : VTDFN2x2-8

Operating Ambient Temperature Range
I : -40 to 85°C

Handling Code
TR : Tape & Reel

Assembly Material
G: Halogen and Lead Free Device

APW8827 QB :	W27 X	X - Date Code	
APW8827 C :	W27X	X - Date Code	
APW8827 QF :	W27 X	X - Date Code	

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	Input Supply Voltage to PGND		-0.3 ~ 6.5	V
V_{LX}	LX to GND Voltage	< 30ns pulse width	-3 ~ 8	V
		> 30ns pulse width	-1 ~V_{IN}+0.3	V
	POK, FB, EN to PGND Voltage		-0.3 ~ 6.5	V
	AGND to PGND Voltage		-0.3 ~ 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	VTDFN2x2-8	75	°C/W
		TDFN2x2-8	75	
		SOT23-6	250	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Control and Driver Supply Voltage	2.9 ~ 5.5	V
I_{OUT}	Converter Output Current	0 ~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

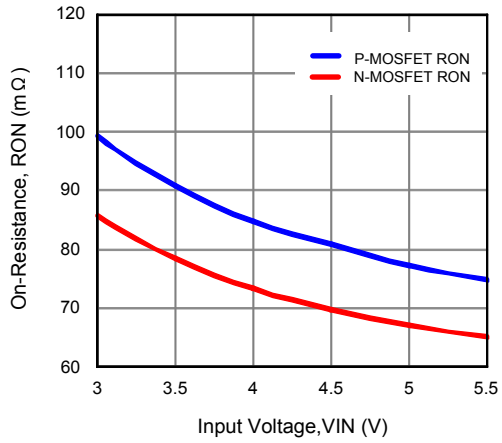
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.7V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

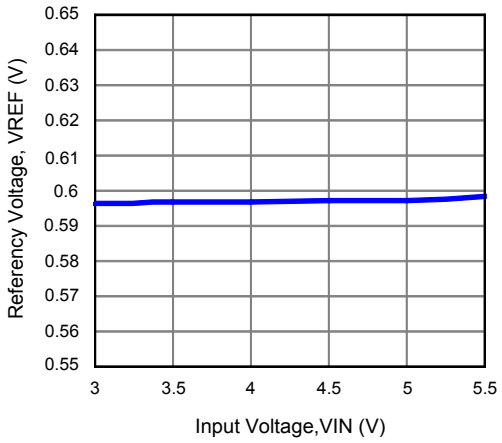
Symbol	Parameter	Test Conditions	APW8827			Unit
			Min	Typ	Max	
Supply Current						
I_{DD}	VIN Supply Current	V_{FB}=0.66V	-	65	-	μA
I_{SHDN}	VIN Shutdown Supply Current	EN=GND	-	-	1	μA
Power-On-Reset (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	2.3	2.4	2.5	V
	VIN POR Hysteresis		0.1	0.2	0.3	V
Reference Voltage						
V_{REF}	Reference Voltage		-	0.6	-	V
		T_A=25°C	-1	-	+1	%
	Output Accuracy	I_{OUT}=10mA~3A, V_{IN}=2.9~5.5V	-1.5	-	+1.5	%
Oscillator						
F_{OSC}	Oscillator Frequency		0.85	1	1.15	MHz
	Minimum on Time		-	70	-	ns
Power MOSFET						
	High Side P-MOSFET Resistance	V_{IN}=5V, I_{LX}=0.5A, T_A=25°C	-	75	-	mΩ
	Low Side N-MOSFET Resistance	V_{IN}=5V, I_{LX}=0.5A, T_A=25°C	-	65	-	mΩ
	High/Low Side MOSFET Leakage Current		-	-	10	μA
Protections						
I_{LIM}	High Side MOSFET current-limit	Peak Current, V_{IN}=2.9~5.5V T_A= -40 ~125 °C	4	5	6	A
T_{OTP}	Over-temperature Trip Point (Resoft start after OTP)		-	160	-	°C
	Over-temperature Hysteresis		-	50	-	°C
	Over- Voltage Protection threshold	V_{OUT} Rising	120	125	130	%V_{REF}
	Under-Voltage Protection threshold		-	50	-	%V_{REF}
	Over-Voltage Protection debounce time		20	25	30	μs
	Low Side Switch Current-Limit	From Drain to Source	-	-1	-	A
Soft-Start, Enable and POK						
	Soft Start time		-	0.8	-	ms
	EN Enable threshold		1.4	-	-	V
	EN shutdown threshold		-	-	0.5	V
	EN Pull Low Current		-	0.5	1	μA
	POK threshold	POK in from Lower (POK Goes High)	82.5	87.5	92.5	%V_{OUT}
		POK Low Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
		POK in from Higher (POK Goes High)	120	125	130	%V_{OUT}
	Power Good pull low resistance		-	-	30	Ω
	Power Good Debounce	High to low	-	20	-	us

Typical Operating Characteristics

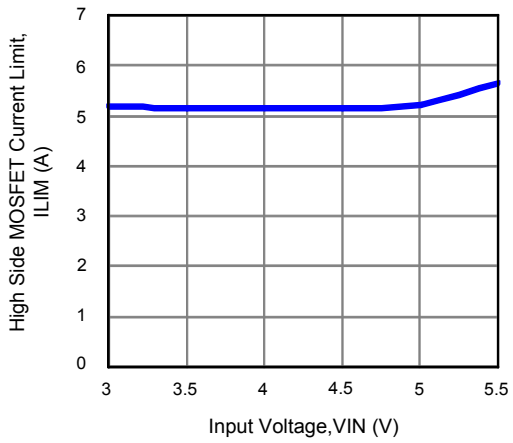
On-Resistance vs. Input Voltage



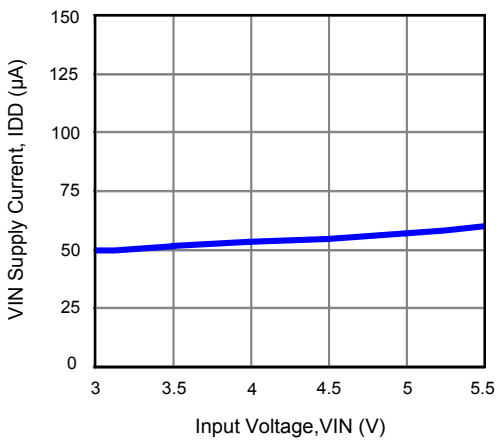
Referency Voltage vs. Input Voltage



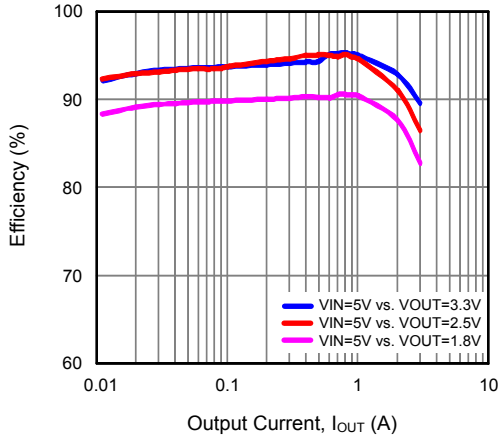
High Side MOSFET Current Limit vs. Input Voltage



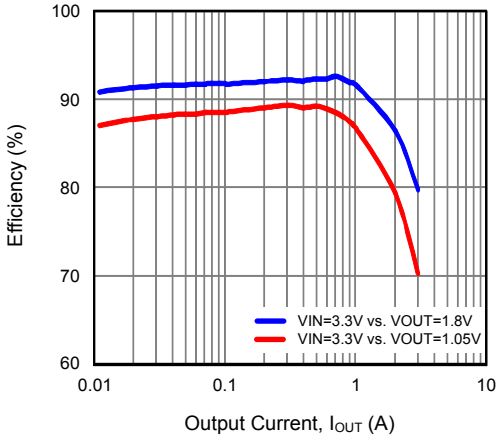
VIN Supply Current vs. Input Voltage



Efficiency vs. Load Current



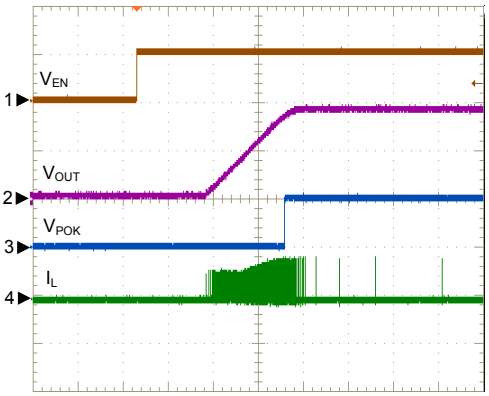
Efficiency vs. Load Current



Operating Waveforms

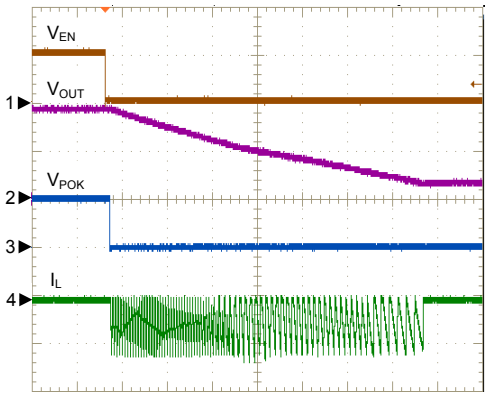
Refer to the typical application circuit. The test condition is V_{IN}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Enable without Loading



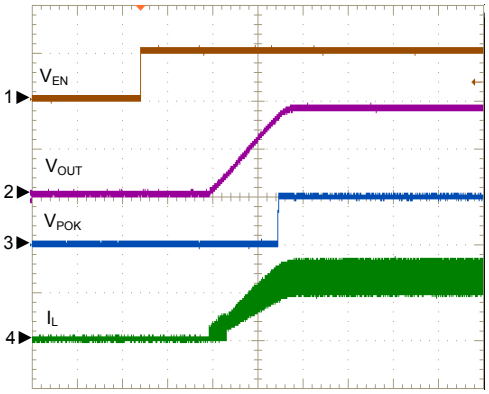
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 400us/Div

Shutdown without Loading



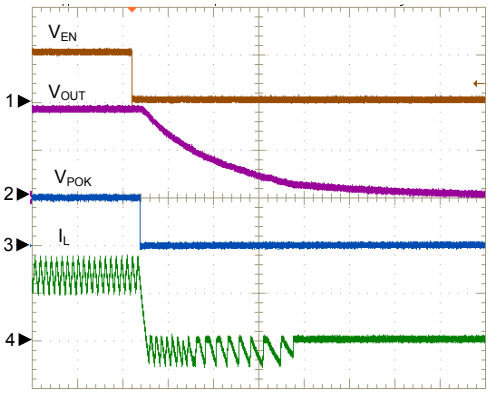
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 20us/Div

Enable with 3A Loading



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 400us/Div

Shutdown with 3A Loading

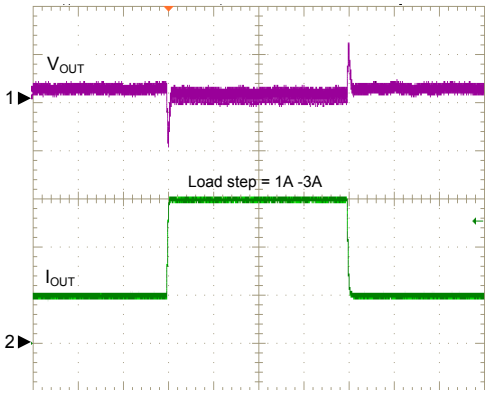


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 10us/Div

Operating Waveforms (Cont.)

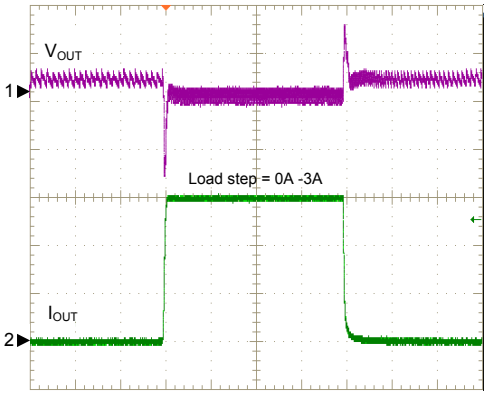
Refer to the typical application circuit. The test condition is V_{IN}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Load Transient



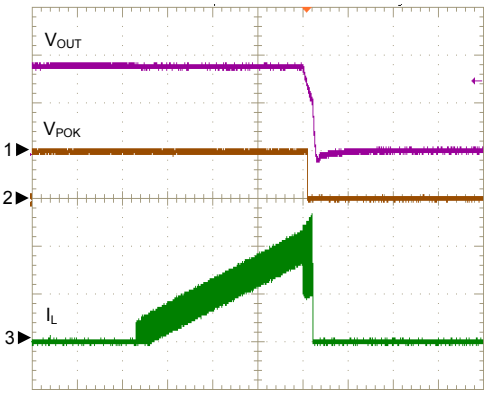
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: I_{OUT}, 1A/Div, DC
TIME: 200us/Div

Load Transient



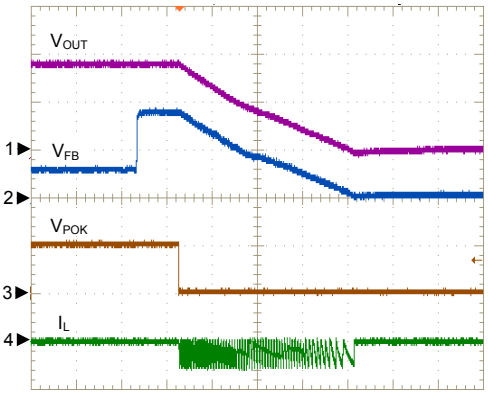
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: I_{OUT}, 1A/Div, DC
TIME: 200us/Div

Current Limit



CH1: V_{OUT}, 1V/Div, DC
CH2: V_{POK}, 5V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 200us/Div

Over Voltage Protection

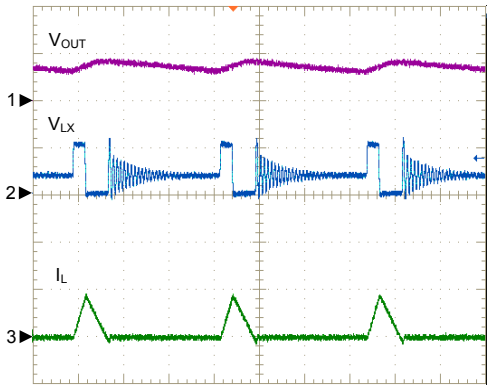


CH1: V_{OUT}, 1V/Div, DC
CH2: V_{FB}, 1V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 2A/Div, DC
TIME: 40us/Div

Operating Waveforms (Cont.)

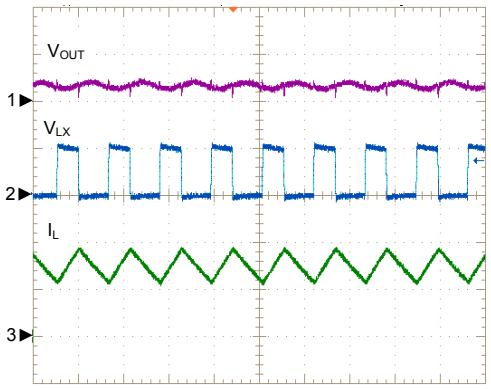
Refer to the typical application circuit. The test condition is V_{IN}=5V, V_{OUT}=1.8V, T_A= 25°C unless otherwise specified.

Normal Operation in Light Load



I_{OUT} =100mA
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 1us/Div

Normal Operation in Heavy Load

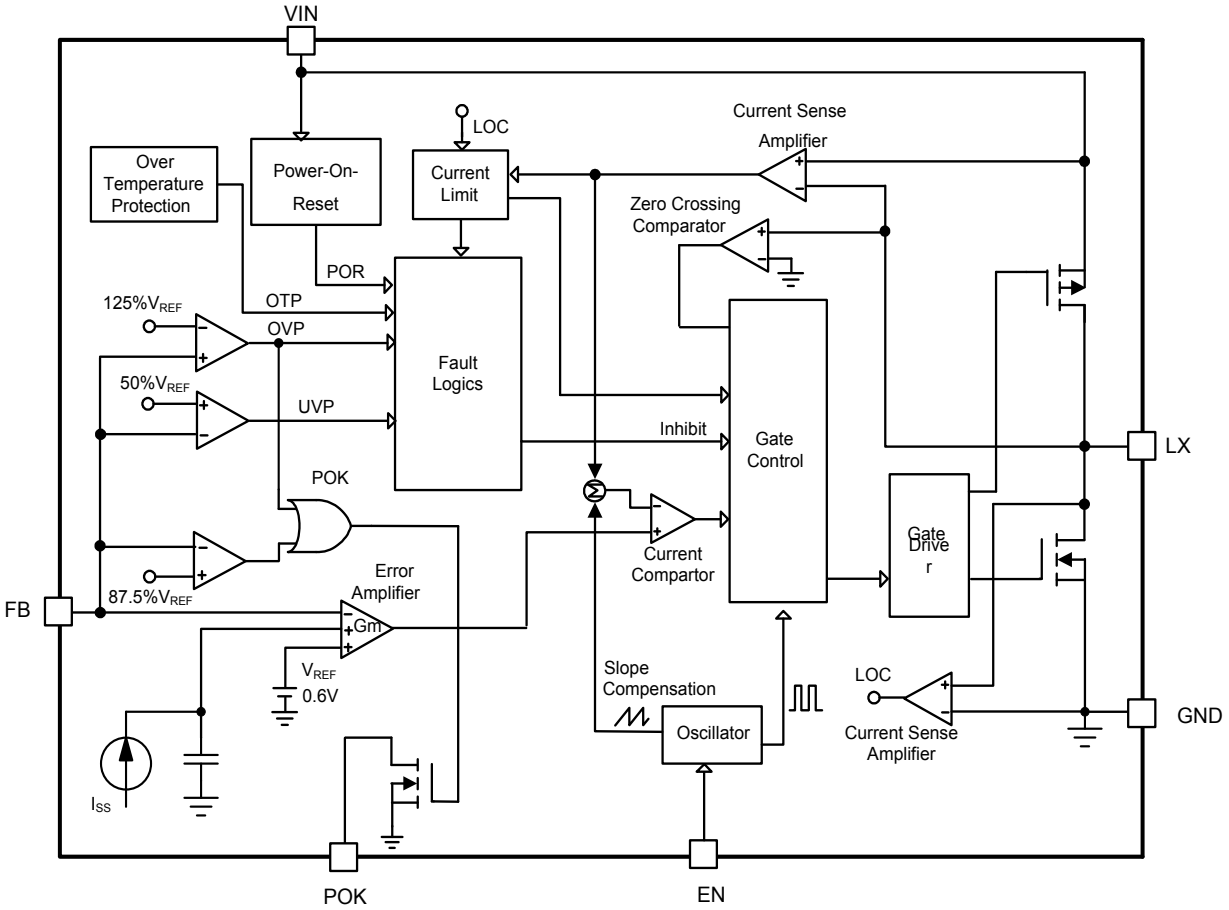


I_{OUT} = 3A
CH1: V_{OUT}, 50mV/Div, DC, Offset=1.8V
CH2: V_{LX}, 5V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 1us/Div

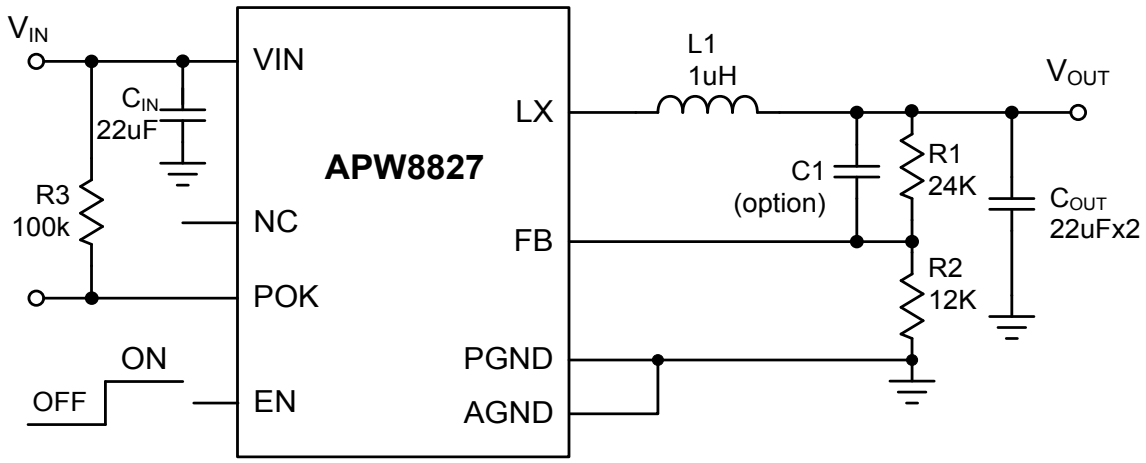
Pin Descriptions

PIN			Function
TDFN2x2-8 VTDFN2x2-8	TSOP23-6	Name	
1	6	FB	Output Feedback Pin. FB Pin senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.
2	5	POK	Output Power Good Indicator Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage for the POK function.
3	4	VIN	Power Input Pin. VIN supplies the power to the buck converter and the the internal control circuitry.
4, Exposed pad	-	PGND	Power Ground. This pin must be connected directly to the ground plane of the PCB.
5	-	NC	No internal connection.
6	3	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
7	1	EN	Enable Input Pin. Drive EN high to turn the converter on and drive it low to turn it off. The EN pin cannot be left floating.
8	-	AGND	Analog Ground. This pin must be connected directly to the ground plane of the PCB.
-	2	GND	IC Ground Pin. This pin must be connected directly to the ground plane of the PCB.

Block Diagram



Typical Application Circuit



Function Descriptions

VIN Power-On-Reset (POR)

The IC continuously monitors the voltage on the VIN pin. The soft start is activated when the VIN voltage and the EN voltage are above their respective POR thresholds.
VIN POR is used to protect the IC from erroneous operation with insufficient VIN voltage. VIN POR also has hysteresis to resist ripple on the VIN voltage.

Output Under-Voltage Protection (UVP)

After the soft start is completed, the IC continuously monitors the output voltage through the FB pin. When the FB voltage drops below the UVP threshold due to an output short circuit, UVP is triggered.
UVP will turn off the converter to prevent the IC from being damaged in the event of a short circuit for a long time. In order to initiate a restart, remove and restore VIN power to the IC or toggle the EN pin.

Over-Voltage Protection (OVP)

The IC continuously monitors the output voltage through the FB pin. OVP is triggered when the FB voltage exceeds the OVP threshold.
OVP will enable the output discharge function to prevent the output voltage from rising continuously. In order to initiate a restart, remove and restore VIN power to the IC or toggle the EN pin.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Current-Limit Protection

The IC monitors the current through the high-side power MOSFET and limits the peak inductor current to prevent the IC from being damaged in the event of an overload or short circuit.
When the IC is operating in current-limit protection mode, the output voltage will drop due to limited output current capability. When the output voltage drops below the UVP threshold, UVP is triggered and the converter is turned off.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot.
The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP.

Output Discharge

When the EN signal is used to turn off the converter or an over-voltage event occurs, the APW8827 initiates a discharge process to cause the output voltage to drop rapidly. During output discharge, the high-side MOSFET will be turned off and the low-side MOSFET will be turned on to allow the output capacitor to discharge through the low-side MOSFET until the discharge current reaches the low-side MOSFET current limit, at which point the low-side MOSFET will be turned off. When the discharge current returns to zero, the low-side MOSFET will be turned on again. Until the FB voltage drops below 0.1V, the discharge process will end and the IC will be turned off.

Enable and Shutdown

The IC provides the EN pin, which is a digital input that turns the converter on or off. Drive EN high to turn the converter on and drive it low to turn it off.

Power Good Indicator

The IC has an open-drain POK pin that indicates the output regulation state.
During soft start, POK goes high when the output reach 87.5% of their target value. During normal operation, when the output is not within the range of 87.5% to 125% of the target voltage, the POK signal will be pulled low immediately. When the output returns between 82.5% and 120% of the target value, the POK will remain high again.
Since POK is an open-drain pull-down device, it usually requires an external pull-up resistor; however, if the pin is not used, no resistor is necessary.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

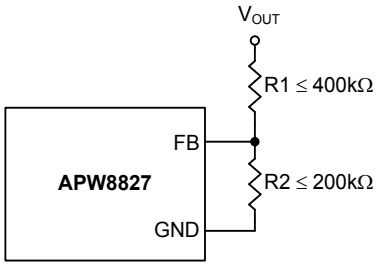
$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to “Typical Application Circuit”. The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 0.6 \cdot \left(1 + \frac{R1}{R2}\right)$$



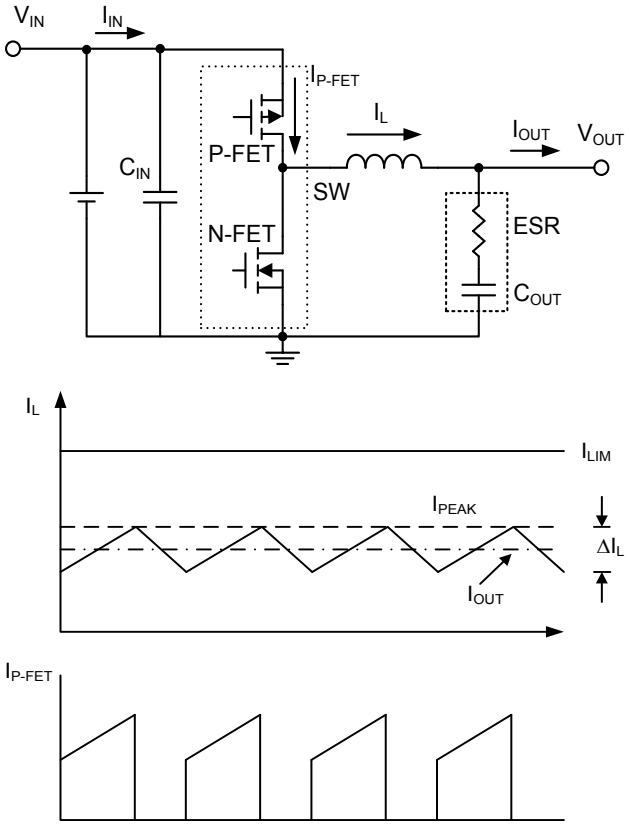
Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple now. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} \cong \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{F_{SW} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Application Information (Cont.)



Power-on Sequencing

The VIN voltage and EN signal should have the correct power-up sequence to avoid triggering UVP or incorrect soft start at startup. It is recommended to provide the EN signal after the VIN voltage is ready.

The recommended power-on sequence is shown in Figure 1.

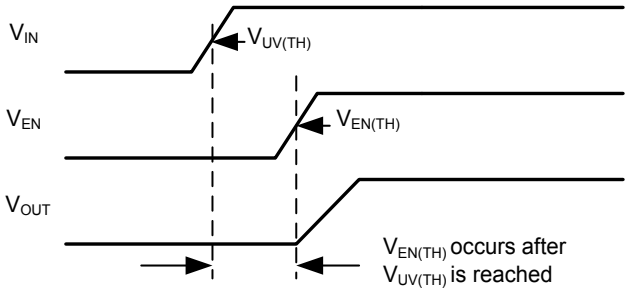


Figure 1. APW8827 power on sequence.

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/PGND to capacitor less than 2mm respectively is recommended.

Layout Consideration(Cont.)

2. Place the VCC capacitor to VCC pin and GND pin as close as possible.
3. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
4. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
5. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
6. For better heat dissipation, it is strongly recommended to enlarge the thermal pad area as much as possible and place a large ground plane on each PCB layer below the thermal pad position, and place as many vias as possible from the top layer to the bottom layer on the thermal pad and around the ground plane.
7. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

Layout Recommendation

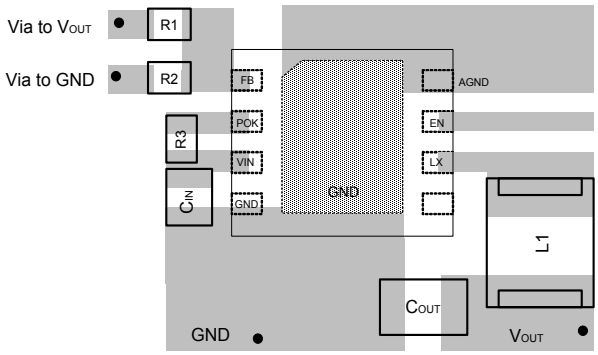


Figure 1: APW8827 TDFN2x2-8 layout recommendation

Recommended Minimum Footprint

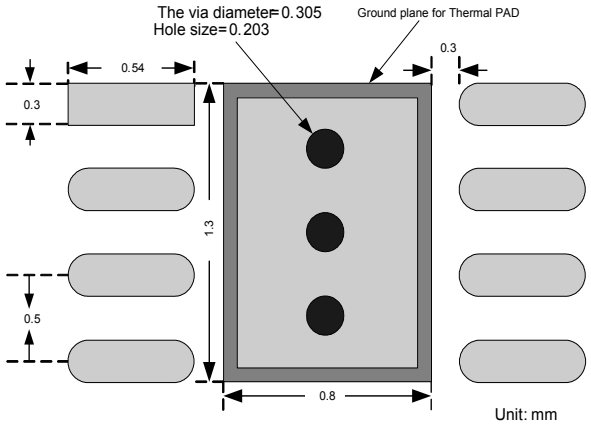


Figure 1: APW8827 TDFN2x2-8 minimum footprint

Application Information (Cont.)

Recommended Minimum Footprint (Cont.)

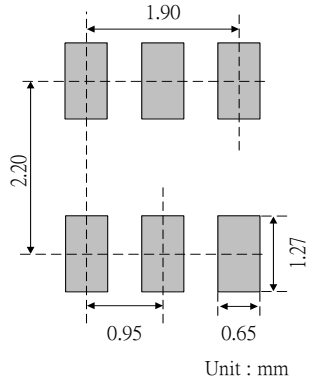
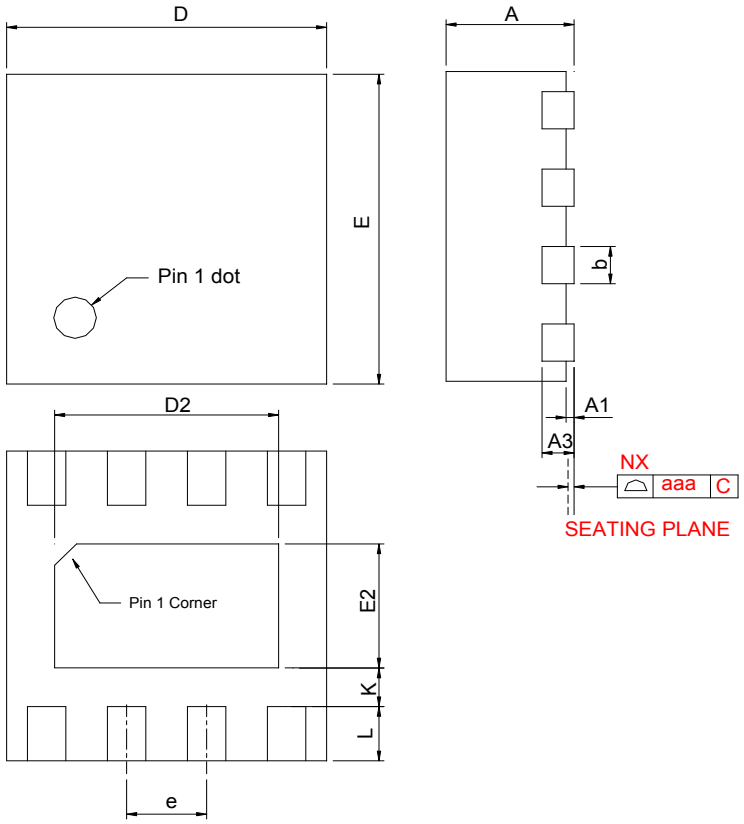


Figure 2: APW8827 SOT-23-6 minimum footprint

Package Information

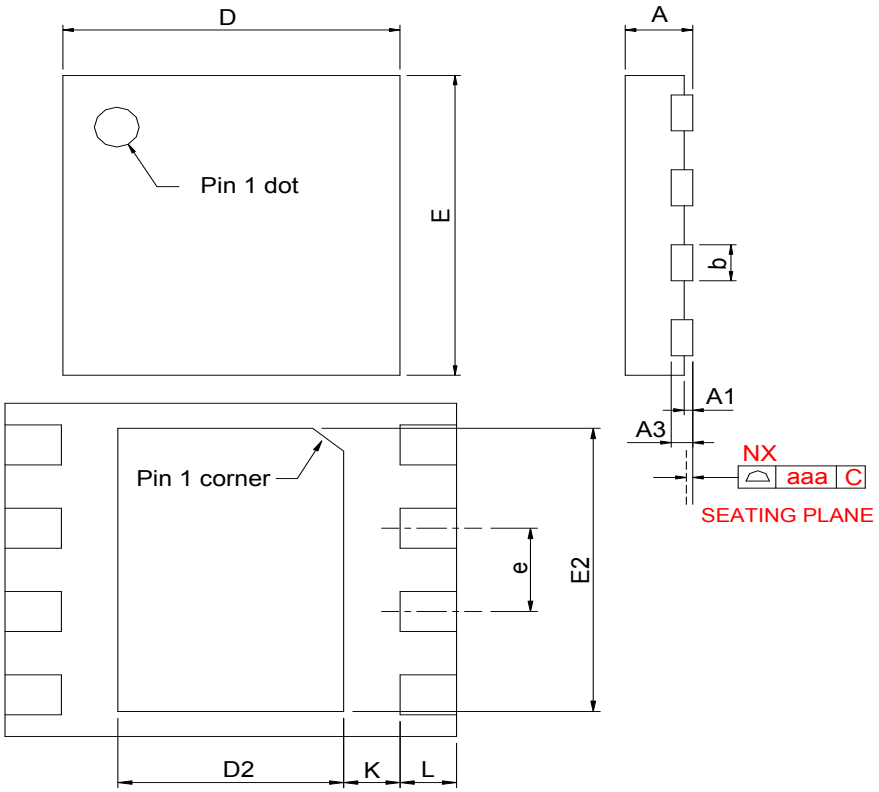
TDFN2x2-8



SYMBOL	TDFN2*2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Package Information

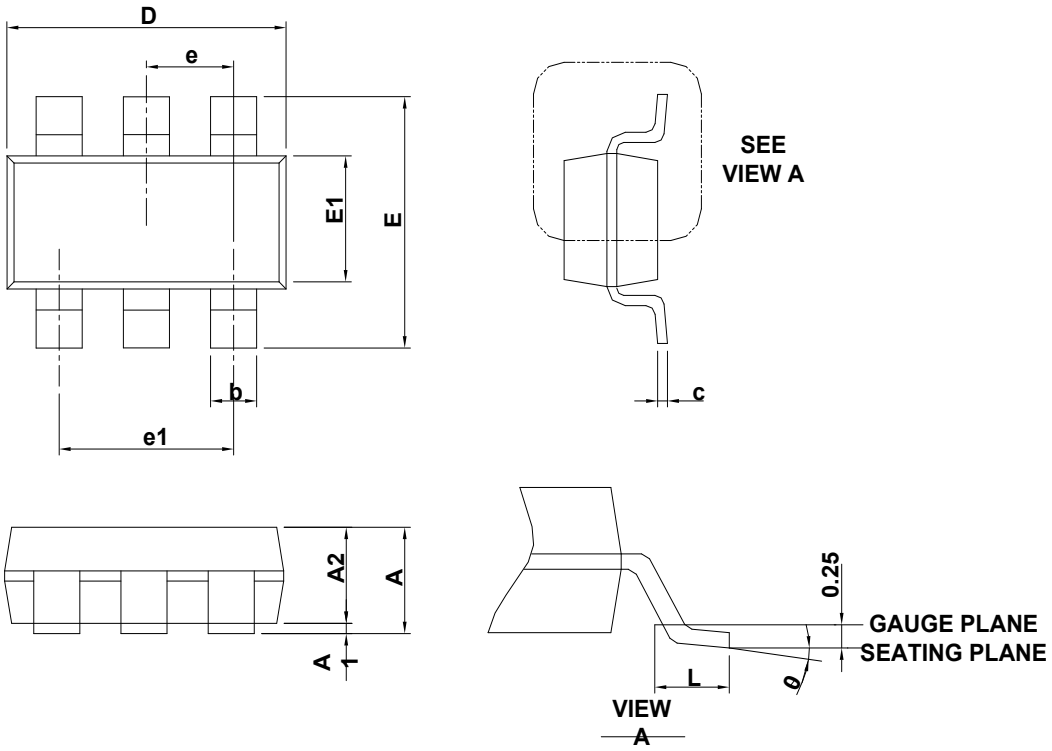
VTDFN2x2-8



SYMBOL	VTDFN2*2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.152 REF		0.006 REF	
b	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
D2	0.90	1.10	0.035	0.043
E	1.90	2.10	0.075	0.083
E2	1.60	1.80	0.063	0.071
e	0.50 BSC		0.020 BSC	
L	0.20	0.30	0.008	0.012
K	0.20		0.008	
aaa	0.08		0.003	

Package Information

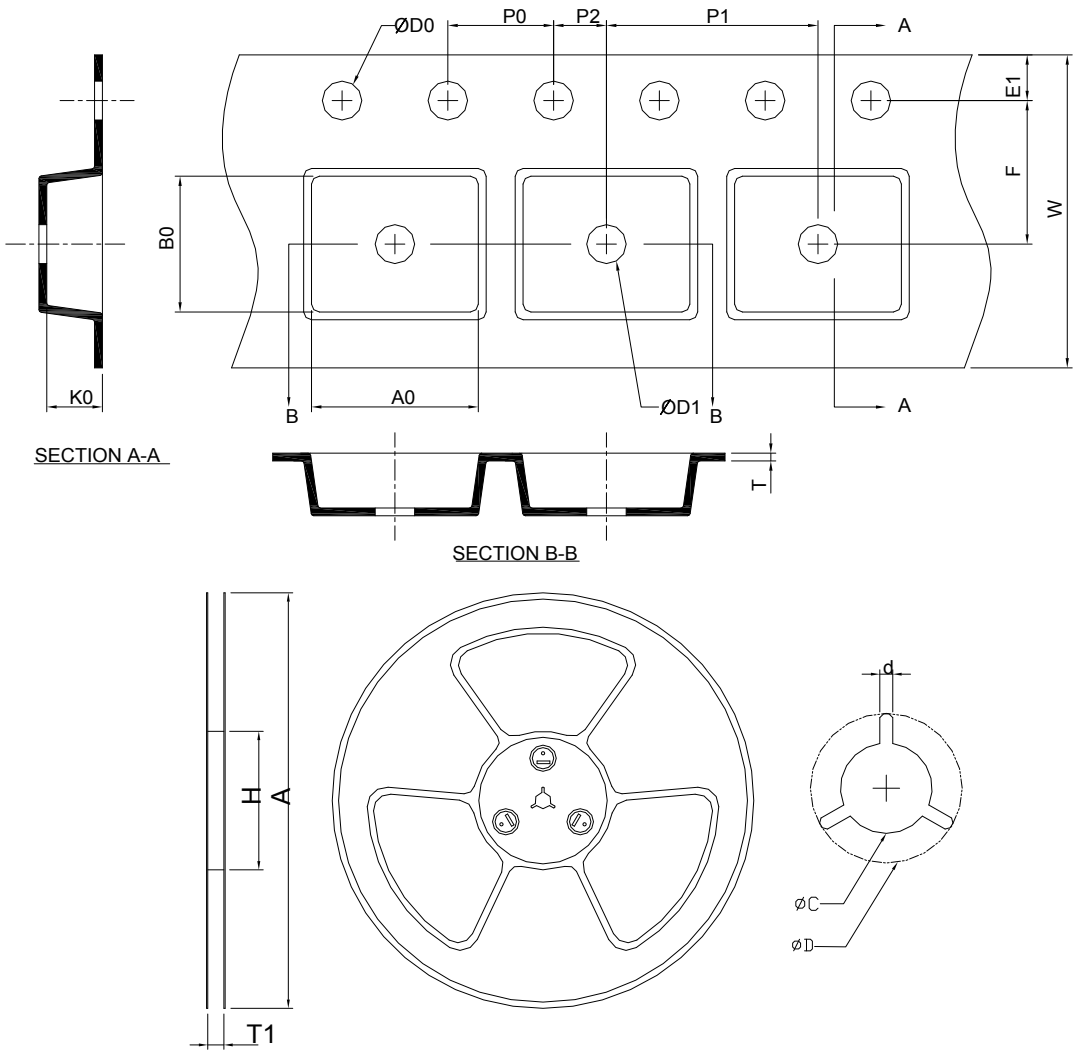
SOT-23-6



SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20
Application	A	H	T1	C	d	D	W	E1	F
VTDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20±0.15	2.20±0.15	0.75±0.05
Application	A	H	T1	C	d	D	W	E1	F
SOT-23-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

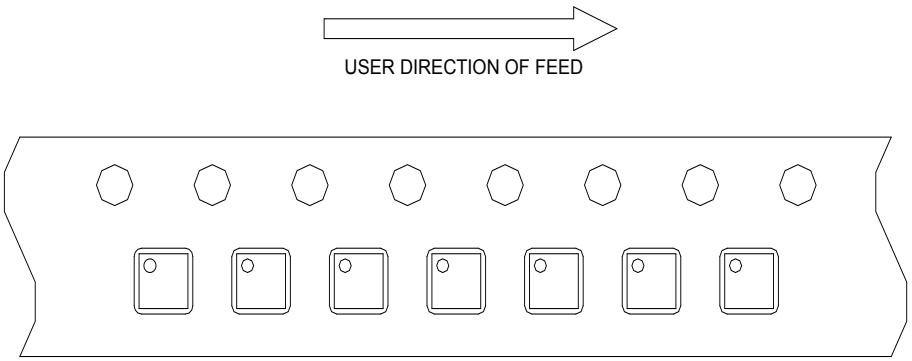
(mm)

Devices Per Unit

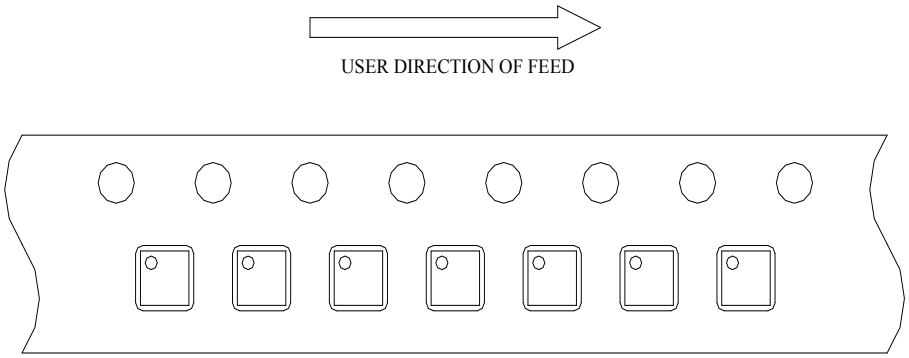
Package Type	Unit	Quantity
SOT-23-6	Tape & Reel	3000
TDFN2x2-8	Tape & Reel	3000
VTDFN2x2-8	Tape & Reel	3000

Taping Direction Information

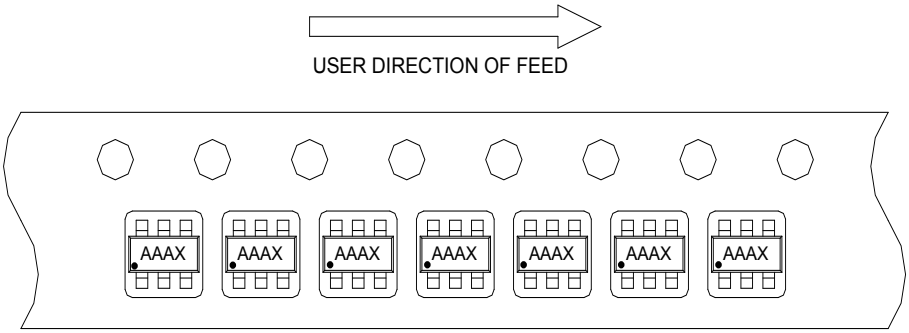
TDFN2x2-8



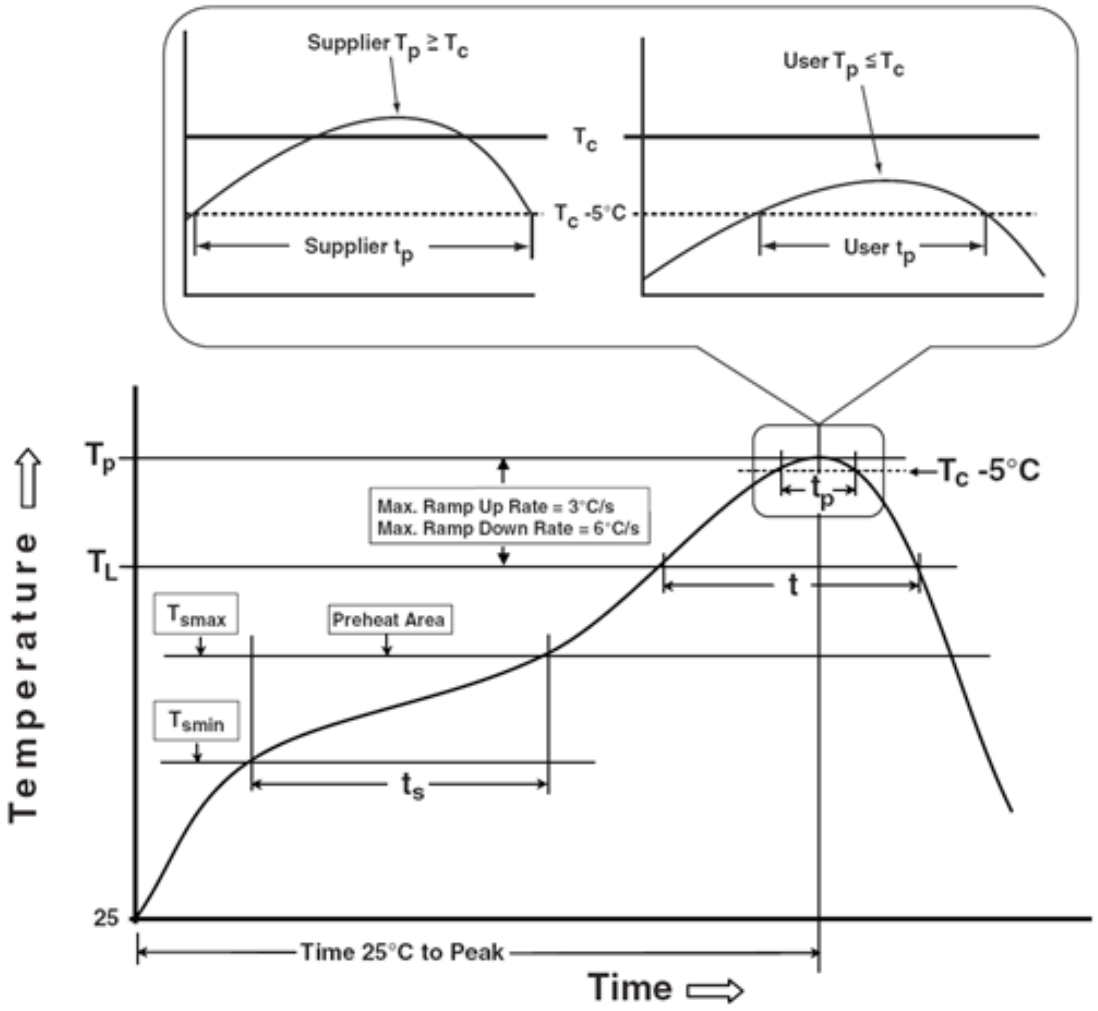
VTDFN2x2-8



SOT-23-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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