High Input Voltage 3.36V / 8A Synchronous Buck Converter with 100mA LDO

Features

- **Wide Operating Range from +5.5V to +24V Input Voltages**
- **Power-On-Reset Monitoring on VIN at 4.5V ~ 4.9V range**
- **Built-in 100uA low quiescent current**
- **Support IOUT = 8A Application**
- **Built in PWM & PFM Control Schemes with COT achitecture**
- **Built in Integrated Bootstrap Forward P-CH MOSFET**
- **Fixed Switching Frequency from700KHz**
- **Fixed 3.36V VOUT REF voltage with ±0.6% accuracy**
- **Support Ultrasonic Mode selection on EN Pin**
- **Support built-in fixed Soft Start time 2.4ms**
- **Integrated 25mΩ N-Channel MOSFET For High Side MOS**
- **Integrated 12mΩ N-Channel MOSFET For Low Side MOS**
- **Built in Open-Drain Type POK function and EN control**
- **Built in 3.36V / 100mA LDO and Switch-over MOSFET with PWM output**
- **UVP setting at 70%of VREF & OVP setting at 125% of VREF & Thermal Shutdown**
- **Built in Over Current Protection and Current Limit Protection using high-side MOSFET $R_{DS(on)}$ and low-side MOSFET $R_{DS(on)}$ sensing**
- **Flip-Chip TQFN 2x3-12P with Lead Free & RoHS compliant**

Applications

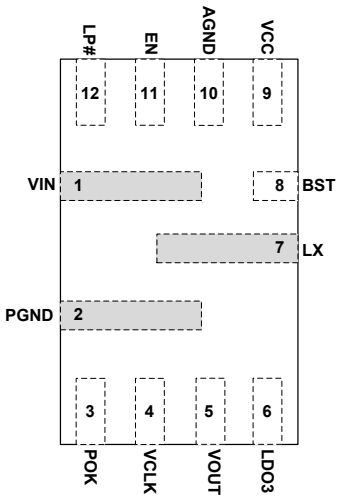
- **Notebook**
- **Graphic card**
- **Motherboard**

General Description

The APW8879A is a 8A, synchronous buck converter with integrated 25mΩ High-Side MOSFET and 12mΩ Low-Side MOSFET. The APW8879A designed with a constant on-time control architecture can step down high voltage to accommodate low-voltage chipset for IMPV8 applications.
The APW8879A is equipped with an automatic PFM/PWM mode operation. At light load, the converter operates in the PFM mode to reduce the switching losses and provide high efficiency. At heavy load, the converter works in PWM mode and operates nearly at constant frequency for low-noise requirements.
The APW8879A is also equipped with Power-on-reset, soft-start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature, over-current and current-limit) into a single package.
The charge pump circuit with 250kHz clock driver uses VOUT as its power supply to generate approximately 10~12V DC voltage.
This device, available in TQFN 2x3-12 package, provides a very compact system solution to minimize external components and PCB area.

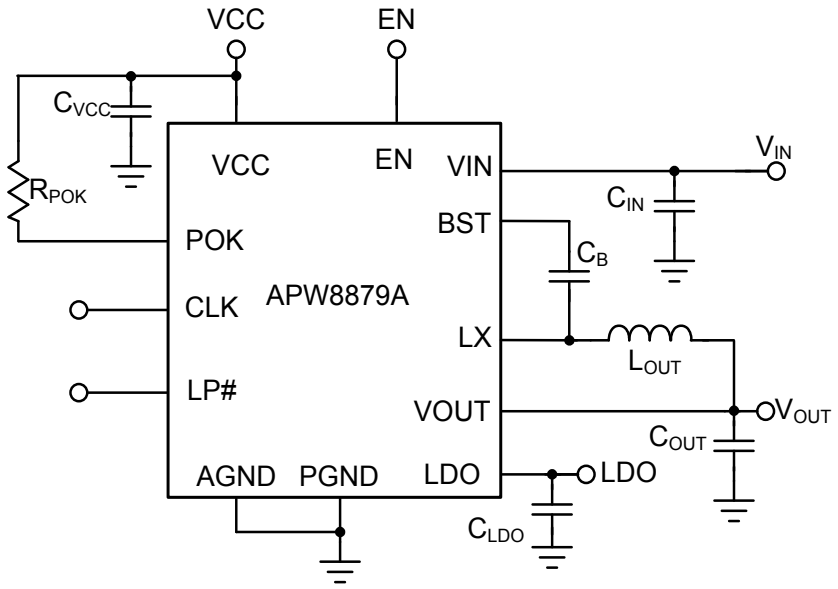
Pin Configuration

APW8879A QBI



FC - TQFN 2x3 -12P
(TOP VIEW)

Simplified Application Circuit



Ordering and Marking Information

APW8879A □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB: TQFN2x3-12 Operating Ambient Temperature Range I : -40 to 85 C° Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device G : Halogen and Lead Free Device
APW8879A QB : 8879A XXXXX	XXXXX - Date Code

Note 1: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 2)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to AGND)		-0.3 ~ 28	V
V_{BOOT}	BOOT Supply Voltage (BOOT to LX)		V_{LX} -0.3 ~ V_{LX} +7	V
V_{GND}	AGND to PGND		-0.3 ~ +0.3	V
	All Other Pins (POK, EN, LP#, VOUT, CLK, LDO, VCC)		-0.3 ~ 7	V
V_{LX}	LX Voltage (LX to GND)		-0.3 ~ V_{IN}+0.3	V
P_D	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C
V_{ESD}	Minimum ESD Rating (Note 3)	Human Body Mode	±2	kV
		MM Mode	0.2	kV

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 3: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 4) – TQFN2x3-12	45	°C/W

Note 4: θ_{JA} is measured with the component mounted on a four-layer Anpec evaluation board in free air.

Recommended Operating Conditions (Note 5)

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	5.5 ~ 24	V
I_{OUT}	Converter Output Current	0 ~ 8	A
L_{OUT}	Converter Output Inductor	1.0 ~ 2.2	µH
C_{IN}	Converter Input Capacitor (MLCC)	20 ~ 30	µF
C_{OUT}	Converter Output Capacitor (MLCC)	44 ~ 66	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 5: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test condition	APW8879A			Unit
			Min.	Typ.	Max.	
INPUT VOLTAGE						
V_{IN}	VIN POR Voltage Threshold	V_{IN} Rising	4.5	4.7	4.9	V
	VIN POR Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE & SOFT START						
V_{OUT}	Reference Output Voltage	LP#=H	-	3.36	-	V
		LP#=L	-	3.23	-	V
	Reference Voltage Accuracy	T_A = 25 degree	-0.6	-	+0.6	%
		T_A = -40 ~ 85 degree	-1	-	+1	%
T_{SS}	Soft Start Time	From EN high to POK high	-	2.4	-	ms
VCC POR THRESHOLD						
V_{CC}	VCC POR Voltage Threshold	V_{CC} Rising	-	4.3	-	V
	VCC POR Hysteresis		-	0.2	-	V
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	At no switching	-	80	100	uA
I_{VIN_SD}	VIN Shutdown Current	VIN = 19V , EN= L	-	60	80	uA
SWITCHING FREQUENCY						
F_{OSC}	Switching Frequency		-	0.7	-	MHz
$T_{ON(min)}$	Minimum On Time		-	50	-	ns
$T_{OFF(min)}$	Minimum Off Time		-	200	-	ns
CONTROL (EN , LP#)						
V_H	High Level Input Threshold Voltage	For EN	1.2	-	-	V
V_L	Low Level Input Threshold Voltage	For EN	-	-	0.4	V
	EN High Level at Ultrasonic Mode	For EN	-	-	1.7	V
	EN Low Level at Normal	For EN	2.3	-	-	V
T_{USM}	Ultrasonic Mode operation period		-	32	-	us
V_H	High Level Input Threshold Voltage	For LP#	1.2	-	-	V
V_L	Low Level Input Threshold Voltage	For LP#	-	-	0.4	V
I_{LKG}	Input Leakage Current at EN, LP#	V_{EN} = $V_{LP\#}$ = 5V	-	1.0	-	uA
INTERNAL POWER SWITCH						
$R_{DS(ON)H}$	NMOS_HI ON Resistance	V_{CC}=5V	-	25	-	mΩ
$R_{DS(ON)L}$	NMOS_LO ON Resistance	V_{CC}=5V	-	12	-	mΩ
I_{LX_LKG}	H-side MOS Leakage Current	V_{IN} = 19V, LX=0V, EN=0V	-	0.1	-	uA
LDO REGULATOR						
V_{LDO}	LDO Regulator		3.3	3.36	3.42	V
	LDO Load Regulation	V_{IN} = 19V , I_{OUT} = 10m~100mA	-	2	-	%
I_{LDO_limit}	LDO Current Limit		150	200	300	mA
	LDO Switch bypass R	ILDO =50mA	-	0.8	-	Ω

Electrical Characteristics (Cont.)

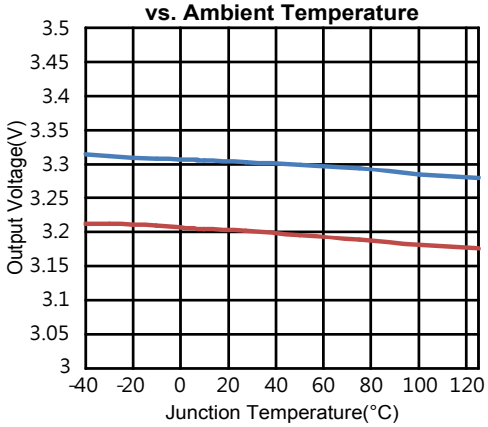
Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN}=5V and T_A= -40 to 85 °C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test condition	APW8879A			Unit
			Min.	Typ.	Max.	
POWER-OK INDICATOR						
V_{POK}	POK Threshold (OTP occur, POK always go low)	VOUT / VREF, POK go high from Lower	85	90	95	%
		Hysteresis	-	5	-	%
		VOUT / VREF, POK go low from Normal	120	125	130	%
	POK Leakage Current		-	0.1	1	uA
	POK High to Low Debounce Time		-	15	-	us
	EN Low to POK Low Delay		-	1	-	us
CURRENT LIMIT & OVER CURRENT PROTECTION						
$I_{\_LIM\_P}$	High side Current Limit		-	16	-	A
$I_{\_LIM\_N}$	Low side Current Limit		-	11	-	A
	High Side Over Current Protection		-	20	-	A
PROTECTION						
V_{OVP}	Over Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	120	125	130	%
	Over Voltage Protection delay time		-	5	-	us
V_{UVP}	Under Voltage Protection	$V_{OUT}/V_{OUT(MON)}$	65	70	75	%
	Under Voltage Protection delay time		-	10	-	us
T_{OTP}	OTP Rising Threshold		-	150	-	°C
	OTP Hysteresis		-	30	-	°C
VCLK Output						
V_{CLKH}	Output High Level Voltage	ICLK = -10mA	3.18	3.23	3.28	V
V_{CLKL}	Output Low Level Voltage	ICLK = 10mA	0	0.05	0.1	V
F_{CLKL}	CLK Switching Frequency		-	250	-	KHz

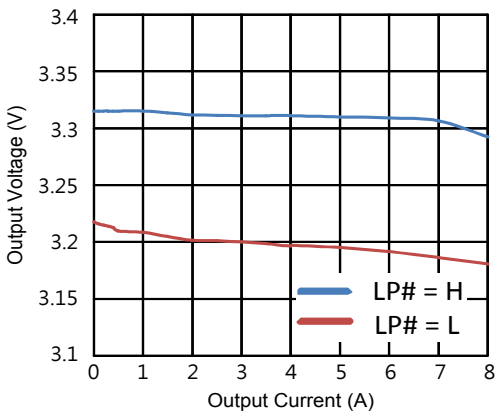
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=19V, L_{OUT}=1.5μH,C_{OUT}=22μF*2 T_A= 25°C unless otherwise specified.

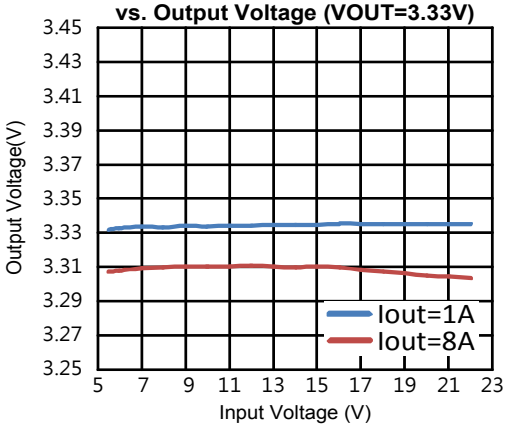
Output Voltage (Iout=2A) vs. Ambient Temperature



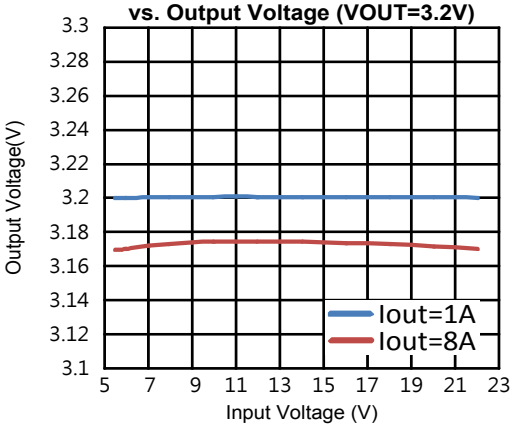
Output Voltage vs. Output Current



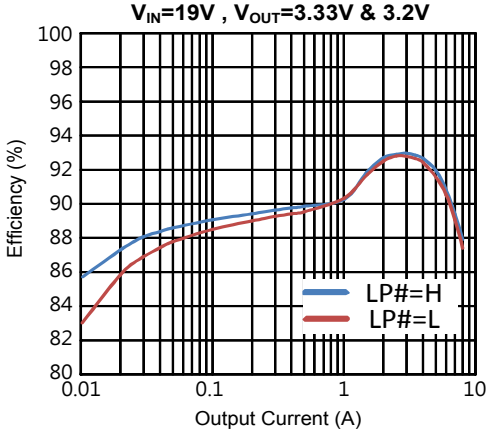
Input Voltage vs. Output Voltage (VOUT=3.33V)



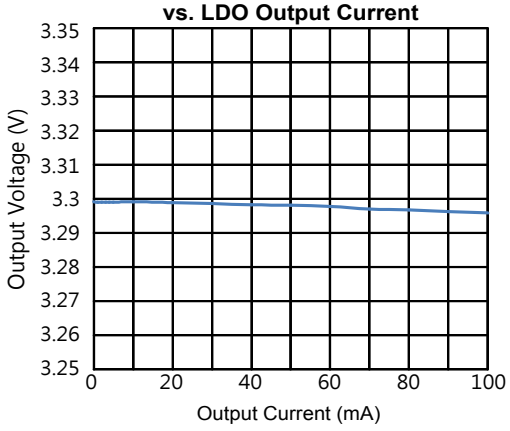
Input Voltage vs. Output Voltage (VOUT=3.2V)



Efficiency vs. Output Current V_{IN}=19V , V_{OUT}=3.33V & 3.2V

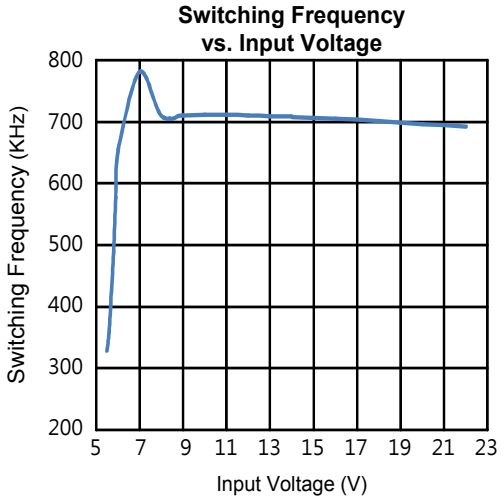


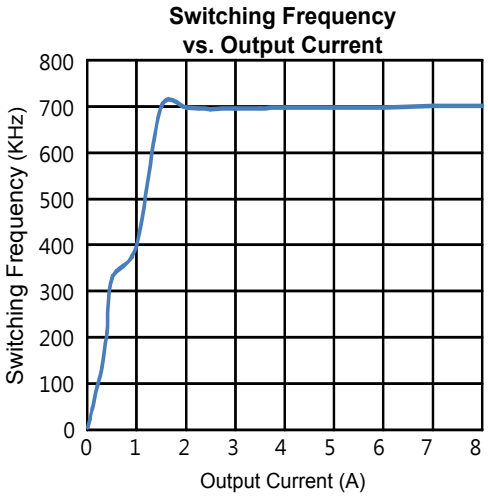
LDO Output Voltage vs. LDO Output Current

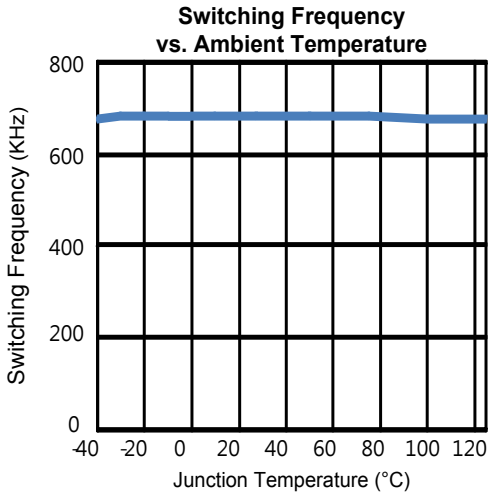


Typical Operating Characteristics (Cont.)

Refer to the typical application circuit. The test condition is V_{IN}=19V, L_{OUT}=1.5μH,C_{OUT}=22μF*2 T_A= 25°C unless otherwise specified.



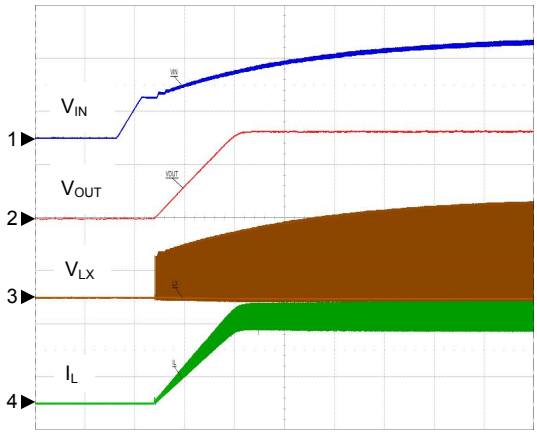




Operating Waveforms

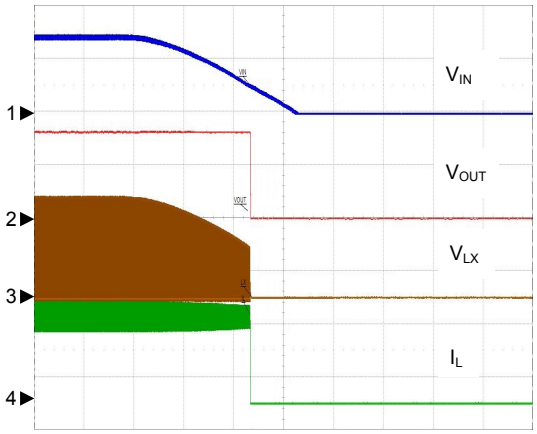
Refer to the typical application circuit. The test condition is V_{IN}=19V, L_{OUT}=1.5µH,C_{OUT}=22µF*2 T_A= 25°C unless otherwise specified.

Power ON



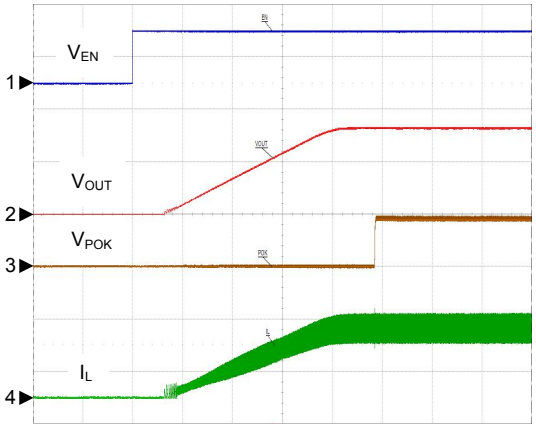
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 5A/Div, DC
TIME: 1ms/Div

Power OFF



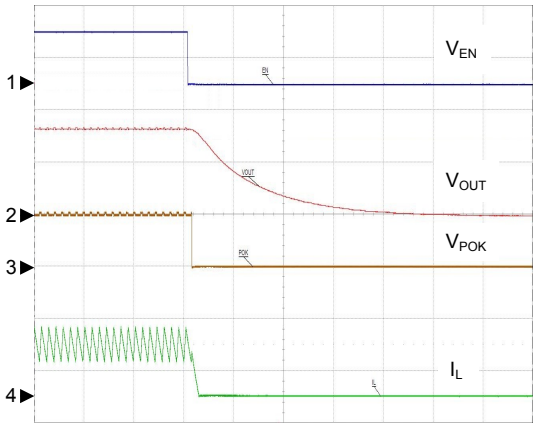
CH1: V_{IN}, 10V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 5A/Div, DC
TIME: 2ms/Div

Enable



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 5A/Div, DC
TIME: 500µs/Div

Disable

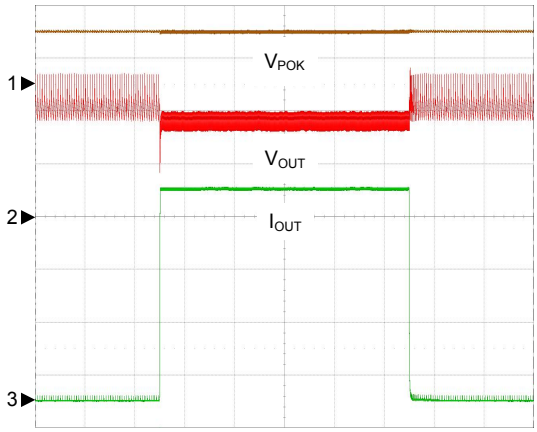


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: V_{POK}, 5V/Div, DC
CH4: I_L, 5A/Div, DC
TIME: 10µs/Div

Operating Waveforms (Cont.)

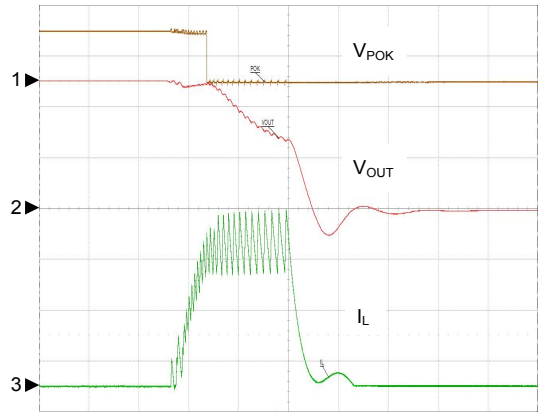
Refer to the typical application circuit. The test condition is V_{IN}=19V, L_{OUT}=1.5µH,C_{OUT}=22µF*2 T_A= 25°C unless otherwise specified.

Load Transient



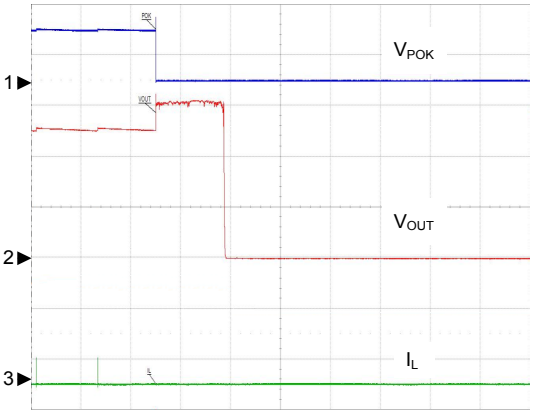
CH1: V_{POK}, 5V/Div, DC
CH2: V_{OUT}, 200mV/Div, DC, Offset=4.65V
CH3: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

Current Limit



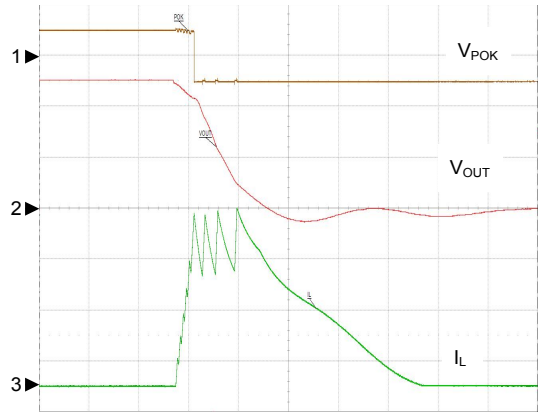
CH1: V_{POK}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_L, 5A/Div, DC
TIME: 20µs/Div

Over Voltage Protection



CH1: V_{POK}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 20ms/Div

Under Voltage Protection

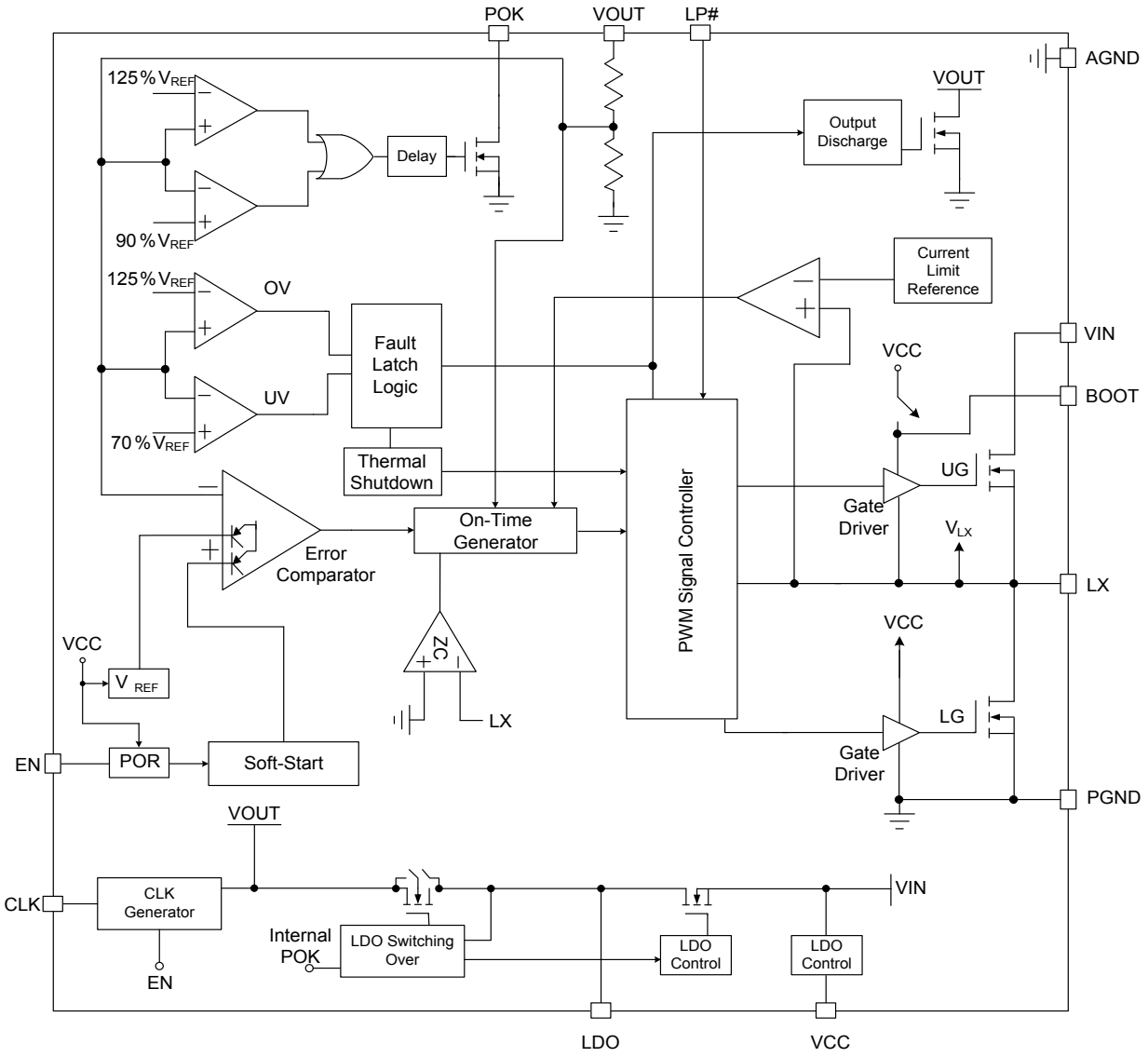


CH1: V_{POK}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_L, 5A/Div, DC
TIME: 10µs/Div

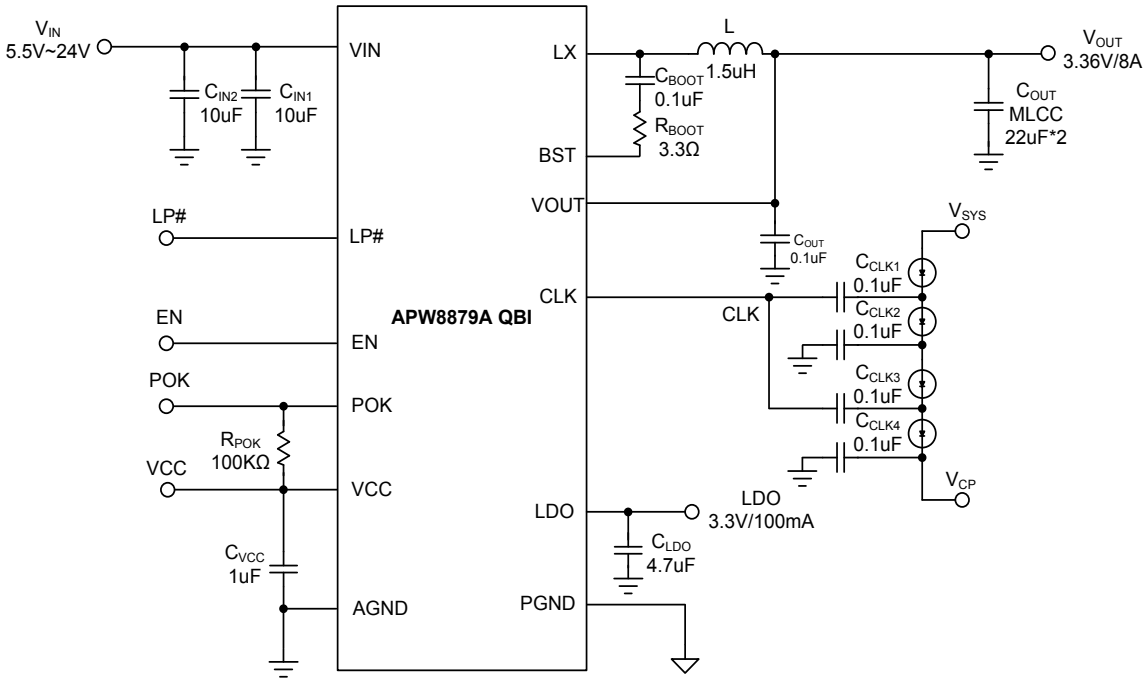
Pin Descriptions

PIN		FUNCTION
NO.	NAME	
1	VIN	Battery Voltage Input. The APW8879A operates from a +5.5V to +24V input rail. Must be closely decoupled to GND with two 10μF or greater ceramic capacitor.
2	PGND	Power Ground of The LGATE Low-Side MOSFET Drivers.
3	POK	Power good indicator. POK is an open-drain output used to indicate the status of the PWM output voltage. Connect a resistor from POK to a pull-high voltage.
4	CLK	250kHz Clock Output for 10-12V Charge Pump. Control by EN also.
5	VOUT	Output Voltage Feedback Pin. This pin is connected to the output voltage.The pin also provide the bypass input for internal LDO.
6	LDO	3.3V Linear Regulator Output. LDO can provide 100mA current for external load. Bypass to GND with a minimum of 4.7uF ceramic capacitor for stability.
7	LX	Power Switching Output. The LX is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter.
8	BST	High-side Gate Driver Supply Voltage Input. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
9	VCC	5V Linear Regulator Output for internal control circuit. And VCC to GND with a 1.0uF ceramic capacitor for stability.
10	AGND	Signal ground for this IC .
11	EN	PWM enable pin. Logic high enables the PWM output. Logic low disables the PWM output. EN pin also be used to set Ultrasonic mode. When EN is between 1.2V and 1.7V, it will enter the Ultrasonic mode. If EN is higher than 2.3V, then it enters the normal mode. Do not float this pin.
12	LP#	Low powermode control signal input pin. Pull high in the normally operation (VOUT=3.36V), and pull low to enter low power mode.

Block Diagram



Typical Application Circuit



Function Descriptions

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudofixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal.
In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.
The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant on-time controller, which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.
Another one-shot sets a minimum off-time (typical: 200ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time oneshot has timed out.

Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode. Similarly, the on-time of ultrasonic mode is the same with PFM mode. The description of ultrasonic mode will be illustrated later.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\,to\,PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM}$$
$$= \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if the enable pin is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.3V, typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 4.1V (typical), the POR disables the chip.

EN Pin Control

When V_{EN} is above the EN high threshold (1.2V, minimum), the converter is enabled. When V_{EN} is below the EN low threshold (0.4V, maximum), the chip is in the shutdown and only low leakage current is taken from VCC. When EN is between 1.2V to 1.7V, and APW8879A will enter the Ultrasonic mode. The unique ultrasonic mode maintains the switching frequency above 32kHz, which eliminates noise in audio application.

Power-Up Control Logics

State	EN	VCC	VOUT	CLK	LDO
S0	1	ON	ON	ON	ON
S3/S5	0	ON	OFF	OFF	ON

LP# Pin Control

APW8879A uses the LP# pin to control voltage scaling function on thelow power mode.

LP# Control Voltage Table

State	LP#	VOUT
S0	H	3.36
S3/S5	L	3.23

Function Descriptions (Cont.)

Soft-Start

The APW8879A has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up to replace the reference voltage until the voltage ramp reaches the reference voltage. Then, the voltage on FB regulated at reference voltage.
In the event of under-voltage, over-voltage, over-temperature or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltages using an internal MOSFET.

Power OK Indicator

POK is actively held low in shutdown and soft-start. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is released. In normal operation, the POK window is from 90% to 125% of the converter reference voltage.When the output voltage stays within this window, POK signal will become high. When the output voltage outruns 90% or 125% of the target voltage, POK signal is pulled low immediately.
In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage protection circuit continually monitors the VOUT voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under voltage threshold, the under voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 3us de-bounce time, the device turns off both high side and low-side MOSFET with latched.
Toggling EN pin to low or recycling VIN will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over voltage function monitors the output voltage by VOUT pin. Should the VOUT voltage increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over voltage protection comparator will turn off the power MOSFET and shut down the IC. Once an over-voltage fault condition is set, it can only be reset by toggling EN or VIN power-on-reset signal.

Current Limit

The APW8879A uses the high-side MOSFET's $R_{DS(ON)}$ and the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. The high side current limit circuit employs a "peak" current-sensing algorithm, and the Low side current limit circuit employs a "valley" current-sensing algorithm(See Figure 1).
If the magnitude of the current-sense signal at LX pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage.
The PWM controller uses the low-side MOSFETs on-resistance $R_{DS(ON)}$ to monitor the current for protection against shorted outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.
The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at LX. Place the hottest power MOSFETs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

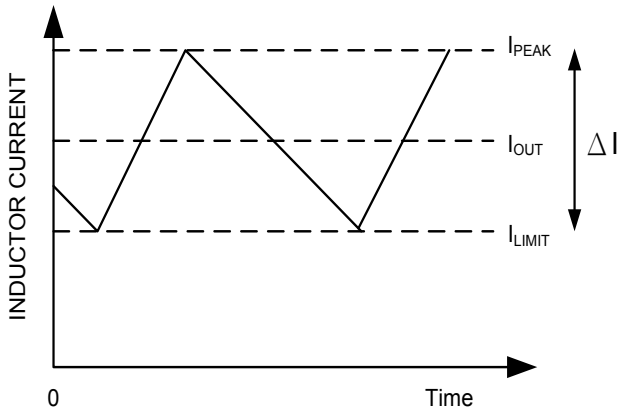


Figure 1. Current Limit algorithm

Function Descriptions (Cont.)

Current Limit (Cont.)

An over-current condition will shut down the device, the VOUT voltage is also discharged to the GND by an internal resistor, requiring a VIN or EN re-enable again to restart IC. When the OCP fault is detected, the POK pin will pull down and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage or if VCC has decayed below the falling POR threshold voltage.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTP}, the IC will enter the over temperature protection state that suspends the PWM, which forces the UG and LG gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP designed with a 30°C hysteresis lowers the average T_J during continuous thermal overload conditions, which increases lifetime of the APW8879A.

Linear Regulator

The LDO regulators can supply up to 100mA for external loads. Bypass to GND with a minimum of 4.7uF ceramic capacitor for stability. In APW8879A, the VLDO is fixed 3.3V in standby mode. When PWM output voltage is over Its bypass threshold (PWM is 3.0V), the internal LDO to VOUT switchover is active. These actions change the current path to power the loads from the PWM regulator voltage, rather than from the internal linear regulator. This LDO is not controlled by EN and LP#.

CLK for Charge Pump

The 250kHz clock signal drives an external charge pump circuit, the charge pump circuit can generate approximate 10-12V DC voltage. The example of charge pump circuit is shown in typical application circuit.

Application Information

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, IRIPPLE, and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator.
Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a trade off exists between the inductor's ripple current and the regulator load transient response time.
A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current.
Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage.
A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta C_{OUT} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1μF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.
To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power-up, the input capacitors have to handle great amount of surge current. For low-duty notebook applications, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Thermal Consideration

Because the APW8879A build-in high-side and low-side MOSFET, the heat dissipated may exceed the maximum junction temperature of the part in applications. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the LX node will become high impedance. To avoid the APW8879A from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The main power dissipated by the part is approximated:

$$P_{UPPER} = I^2_{OUT}(1+T_C)(R_{DS(ON)})D + 0.5(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{LOWER} = I^2_{OUT}(1+T_C)(R_{DS(ON)})(1-D)$$

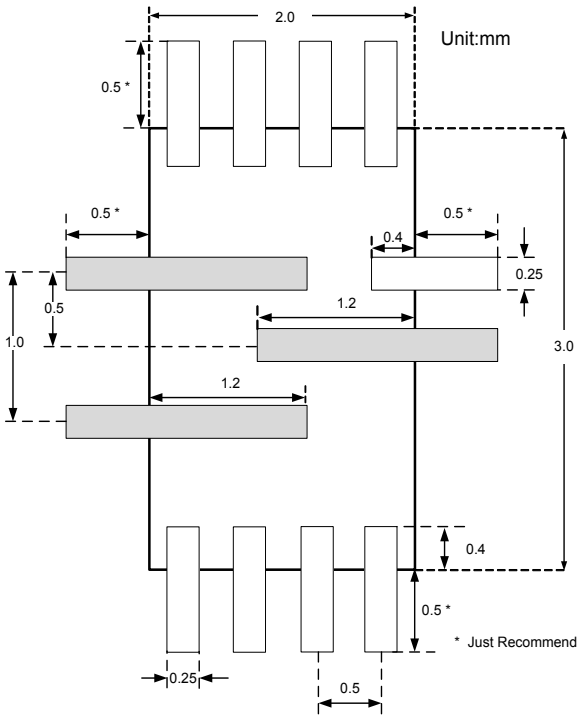
I_{OUT} is the load current
T_C is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both internal MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The $(1+T_C)$ term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET. In APW8879A case, the $R_{DS(ON)}$ is about 25mΩ from specification table.

Application Information (Cont.)

Recommended Minimum Footprint

FC - TQFN 2x3 -12

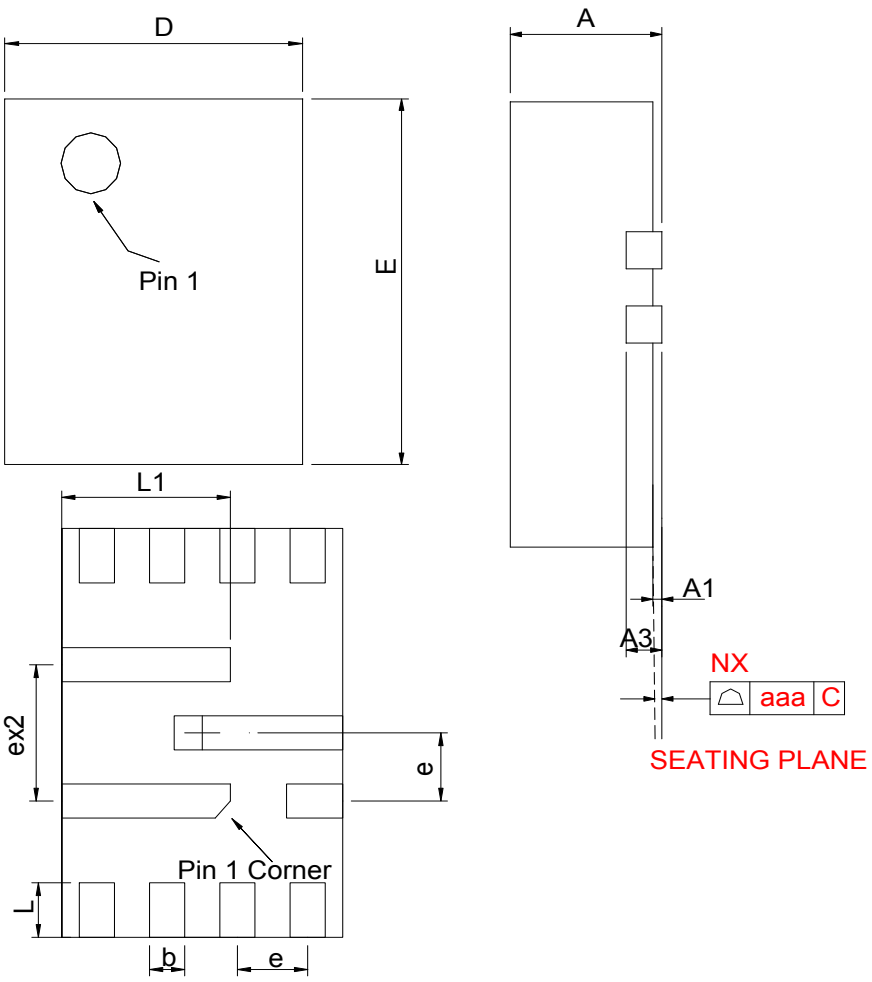


Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.
In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike.
In addition, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point rounding.
The signal ground and the power ground is at the negative Side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:
1. Keep the switching nodes (BOOT, and LX) away from sensitive small signal nodes(VOUT) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
2. Place the high-current paths (VIN, GND and LX) very close to the device and wide traces. The PGND trace should be as wide as possible (It should be the top priority).
3. Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible and on the same layer as the IC.)
4. The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. the input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
5. Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (BOOT, and LX).
6. A 4-layer layout is strongly recommended to achieve better thermal performance.

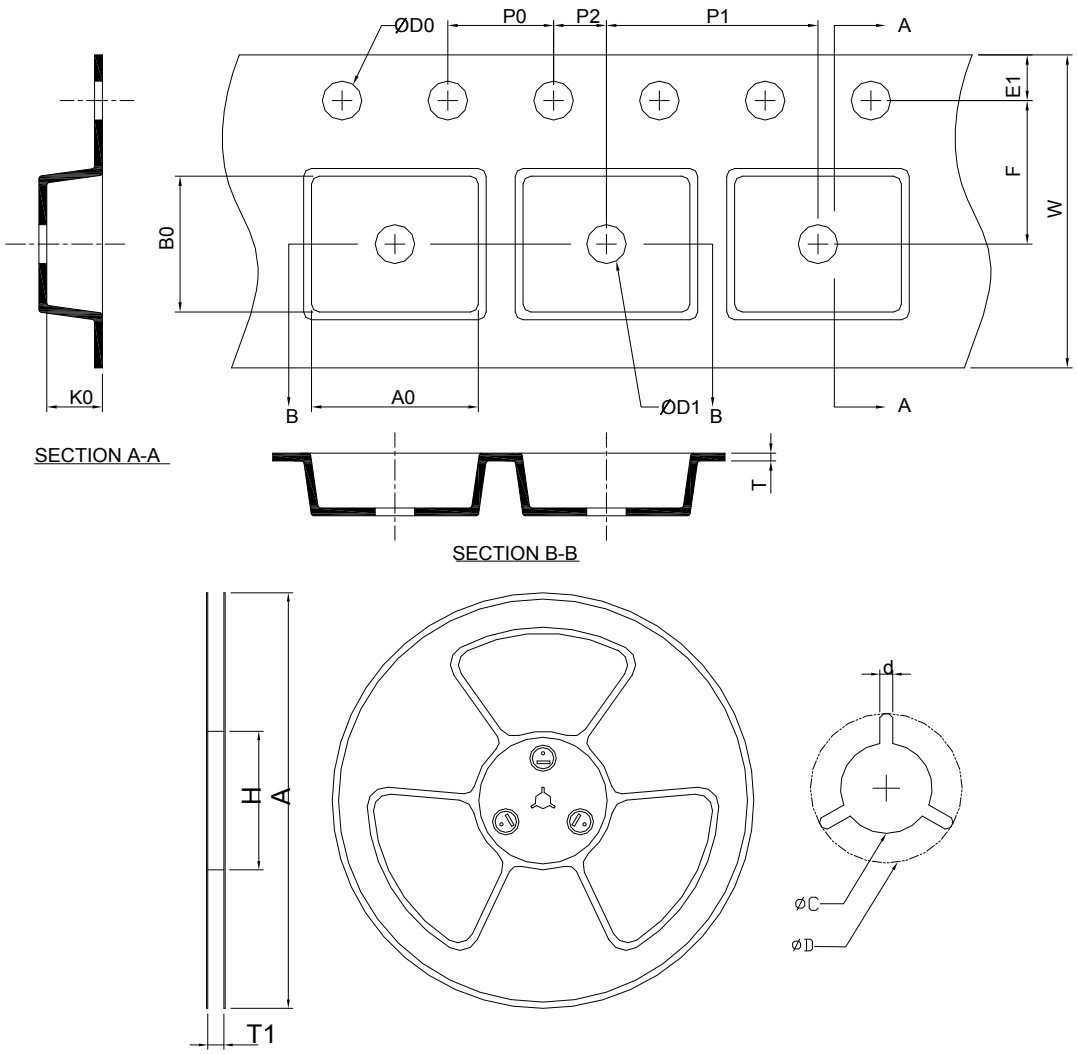
Package Information

TQFN2x3-12P



SYMBOL	TQFN2*3-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	1.90	2.10	0.075	0.083
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
L1	1.15	1.25	0.045	0.049
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN2x3	178.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.20	1.75±0.10	5.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.30±0.05	2.30±0.20	3.30±0.20	1.00±0.20

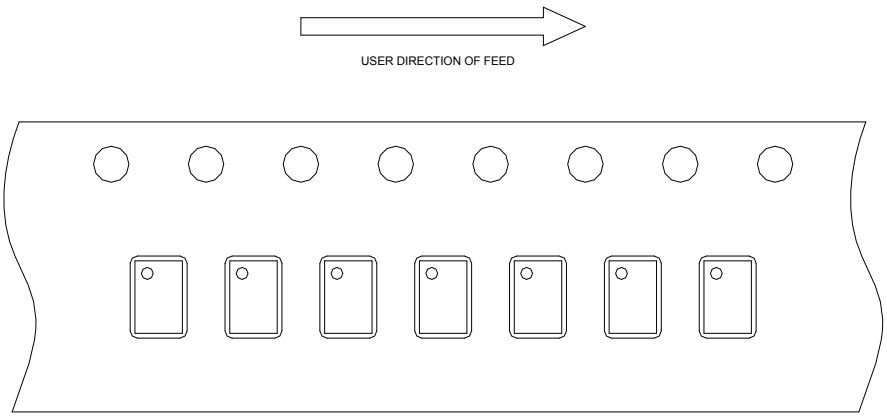
(mm)

Devices Per Unit

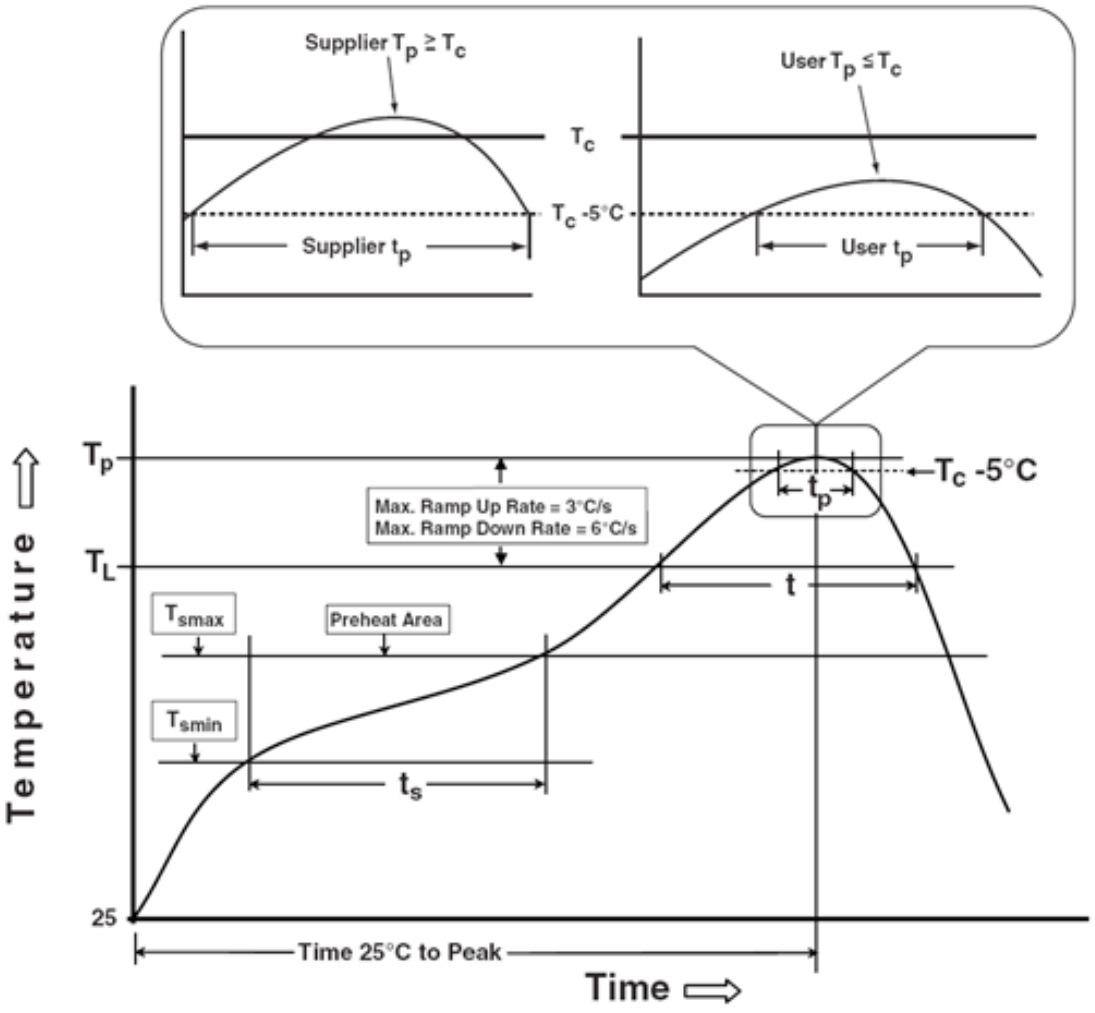
Package type	Packing	Quantity
TQFN(2x3)	Tape & Reel	1500

Taping Direction Information

TQFN2x3-12P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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