APW9103

3A, 18V, 600kHz Synchronous Step-Down Converter

Features

- **Input Voltage range : 4.5V to 18V.**
- **3A Output Current**
- **Typical 0.6V ±1% Internal Reference Voltage.**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **– N-CH MOSFET (70mΩ) for High Side**
  - **– N-CH MOSFET (38mΩ) for Low Side**
- **DyncBandwidth™ Technology**
- **Built in OVP, UVP, Current Limit and OTP.**
- **Low Cost TSOT23-8 package.**
- **Lead Free and Green Devices Available (RoHS Compliant).**

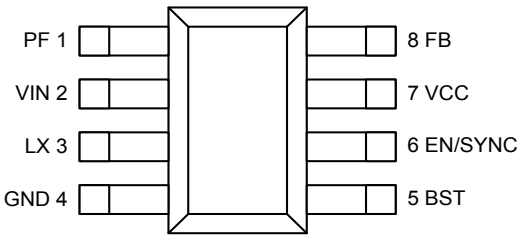
General Description

The APW9103 is a high efficiency synchronous buck converter with integrated 70mΩ/38mΩ of upper/lower power MOSFET and offers 3A continuous current capability.
The APW9103 uses a peak current mode control scheme to regulate the output voltage. The internal switching frequency is set at 600kHz. And EN/SYNC supports external clock synchronization..
The APW9103 is also equipped with Power-on-reset, soft start, and whole protections (over-temperature, overvoltage, under-voltage, over-current) into a single package.
The APW9103 is offered in a TSOT23-8 package allowing small size while having an excellent thermal capability for power dissipation.

Applications

- **Set-Top-Box**
- **DDR4, LPDDR4, LPDDR4X**
- **Digital Subscriber Line**
- **Passive Optical Network**
- **G.fast**
- **Wi-Fi Router**

Pin Configuration (Top View)



Order and Marking Information

APW9103 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code AZ: TSOT-23-8 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW9103 AZ : 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN to PGND		-0.3 ~ 19	V
V_{BS}	BST to LX		-0.3 ~ 5.5	V
V_{LX}	LX to GND	>10ns	-0.6 ~ 19	V
		<10ns	-6 ~ 21	V
$V_{I/O}$	VCC, PF, EN/SYNC, FB to GND		-0.3 ~ 6	V
PD	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	100	°C/W
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 3)	65	°C/W

Note 2: θ_{JA} is measured on 4 layers test board following the EIA/JESD51-7.
Note 3: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operation Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN supply voltage	4.5 ~ 18	V
$V_{EN/SYNC}$	EN/SYNC input voltage	0 ~ 5	V
V_{OUT}	Converter output voltage	0.6 ~ 5	V
I_{OUT}	Converter output current	3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY						
V_{UVLO_R}	UVLO Upper Threshold	VIN Rising	-	4.2	-	V
V_{UVLO_HYS}	UVLO Hysteresis Voltage	VIN Falling	-	0.4	-	V
I_{VIN}	VIN Input Current	V_{FB}=0.7V, LX=NC	-	100	-	μA
I_{VIN_SHDN}	VIN Shutdown Current	EN=PGND	-	3	-	μA
EN/SYNC Threshold						
V_{EN_H}	EN Input Threshold High Voltage		-	1	1.15	V
V_{EN_Hys}	EN Input Hysteresis Voltage		-	0.25	-	V
$T_{DB\_EN\_OFF}$	EN Turn Off Debounce Time		-	20	-	μs
T_{D_EN}	EN Turn On Delay Time	When EN High to LX Switching	-	550	-	μs
I_{EN}	EN Input Current	VEN=2V	-	2	-	μA
R_{DIS}	Discharge Resistor	When EN goes Low	-	20	-	Ω
F_{SYNC}	SYNC Frequency Range		400	-	2000	kHz
	SYNC Minimum off Time		180	-	-	ns
	EN/SYNC Input High Level	For SYNC Function	1.8	-	-	V
	EN/SYNC Input Low Level	For SYNC Function	-	-	0.25	V
REGULATOR AND VCC						
V_{REF}	Reference Voltage	T_J=25°C	594	600	606	mV
V_{POR}	VCC POR Threshold Voltage	VCC Rising	-	4	-	V
V_{POR_Hys}	VCC POR Hysteresis Voltage	VCC Falling	-	0.4	-	V
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A	-	5	-	V
	VCC Load Regulation	I_{VCC}=10mA	-	3	-	%
	VCC Maximum Current	When VCC drop to 4.75V	40	-	-	mA
t_{SS}	Output Soft Start Time	VOUT form 0% to 90%	-	1	-	ms
OSCILLATOR FREQUENCY						
F_{OSC}	Oscillator Frequency		-	600	-	kHz
	Frequency Accuracy	T_J=-40~125°C	-20	-	+20	%
	Minimum on Time		-	70	-	ns
	Maximum Duty	(Note5)	-	90	-	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

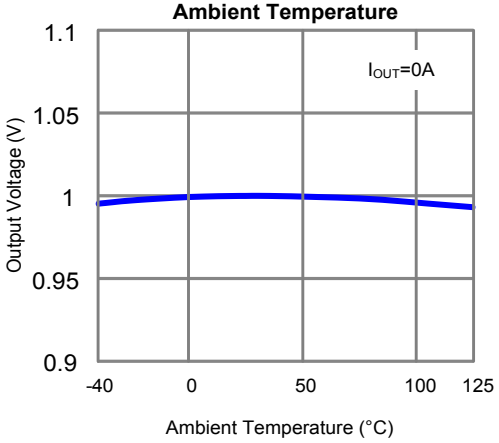
Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
POWER MOSFET						
	High Side MOSFET Resistance		-	70	-	mΩ
	Low Side MOSFET Resistance		-	38	-	mΩ
	High Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=AGND	-	-	1	μA
	Low Side MOSFET Leakage Current	V_{EN}=5V, V_{LX}=VIN, FB=0.7V	-	-	1	μA
BOOTSTRAP POWER						
R_{BST}	BST Switch On Resistance		-	14	-	Ω
	BST Leakage Current	V_{BST-LX}=5V	-	-	1	μA
PROTECTIONS						
I_{LIM}	High Side MOSFET current-limit		-	5	-	A
	Over-temperature Trip Point	(Note6)	-	150	-	°C
	Over-temperature Hysteresis	(Note6)	-	30	-	°C
	Under Voltage Protection		-	50	-	%V_{REF}
	Over Voltage Protection		-	125	-	%V_{REF}
Power Flag						
	PF Restart Delay Time		-	30	-	ms
VBO	Brown Out Voltage	VIN Falling	-	10	-	V
	Brown Out Voltage Hysteresis	VIN Rising	-	0.5	-	V

Note5: Typical value is designed for switching frequency 600kHz
Note6: Guarantee by design

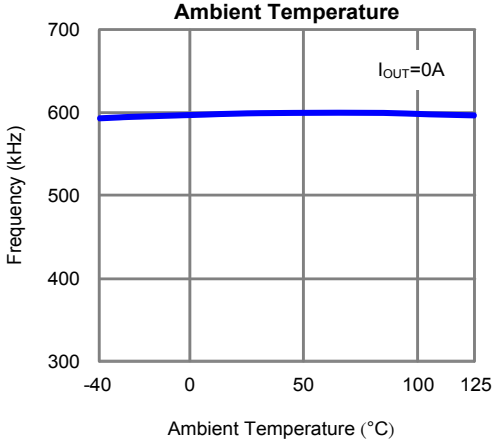
Typical Operating Characteristics

Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

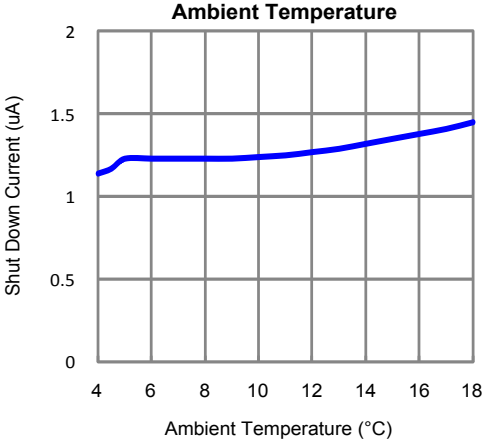
Output Voltage vs. Ambient Temperature



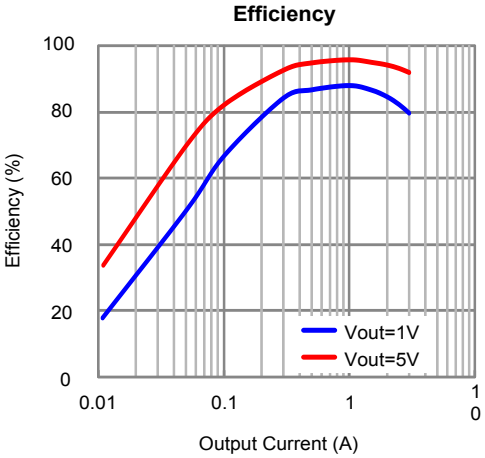
Switching Frequency vs. Ambient Temperature



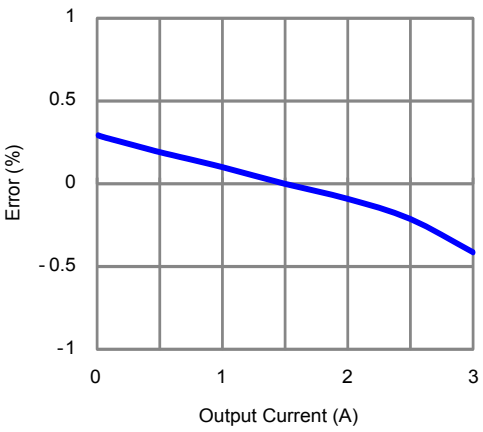
Shut Down Current vs. Ambient Temperature



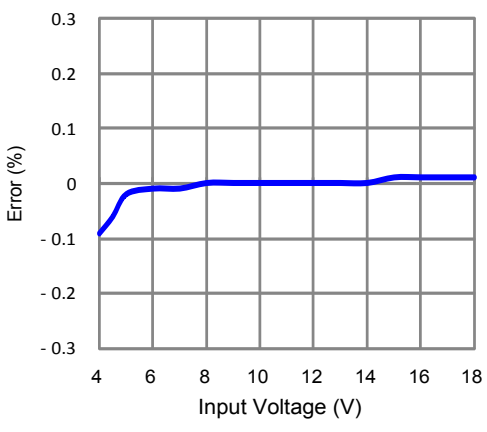
Efficiency



Load Regulation



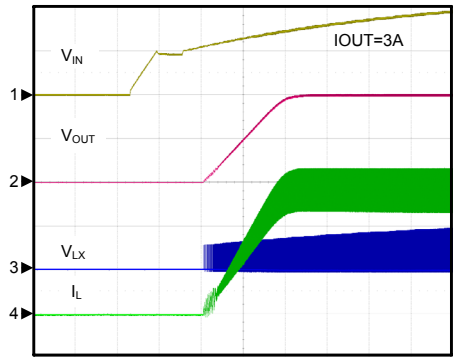
Line Regulation



Operating Waveforms

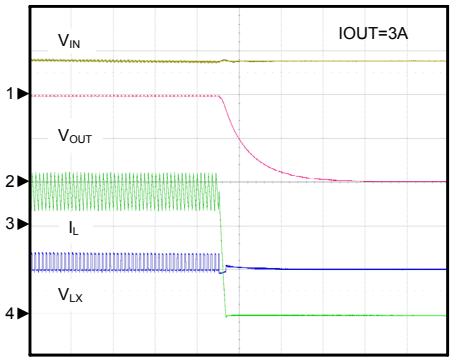
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Start Up through V_{IN}



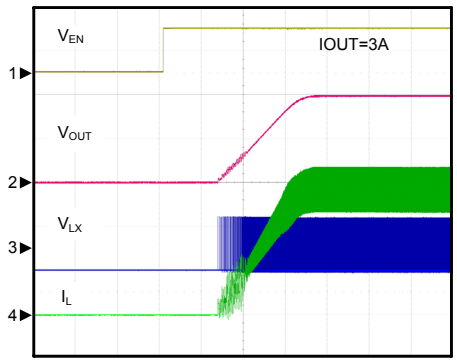
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 500µs/Div

Shut Down through V_{IN}



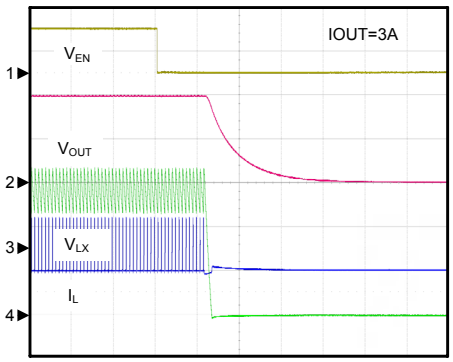
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 20µs/Div

Start Up through V_{EN}



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 500µs/Div

Shut Down through V_{EN}

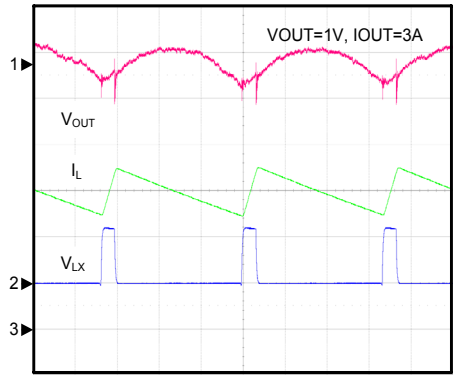


CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{LX}, 10V/Div, DC
CH4: I_L, 1A/Div, DC
TIME: 20µs/Div

Operating Waveforms (Cont.)

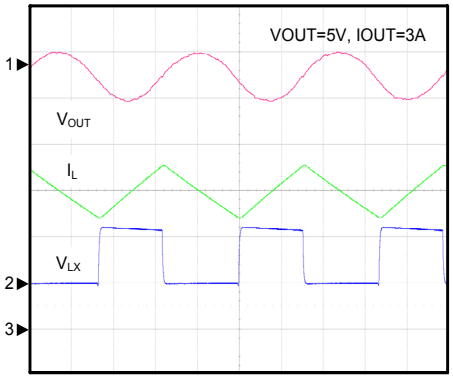
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Output Ripple



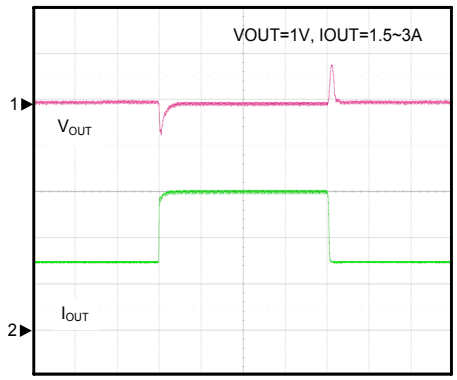
CH1: V_{OUT},10mV/Div, AC
CH2: V_{LX}, 10V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 500ns/Div

Output Ripple



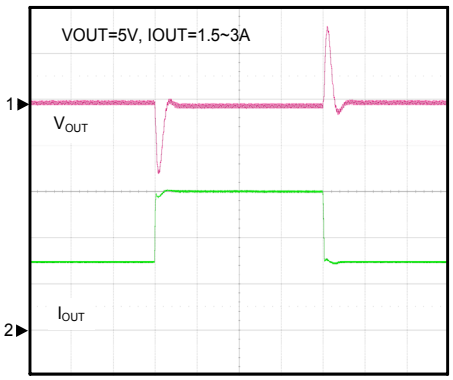
CH1: V_{OUT}, 20mV/Div, AC
CH2: V_{LX}, 10V/Div, DC
CH3: I_L, 1A/Div, DC
TIME: 500ns/Div

Load Transient



CH1: V_{OUT}, 100mV/Div, AC
CH2: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Load Transient

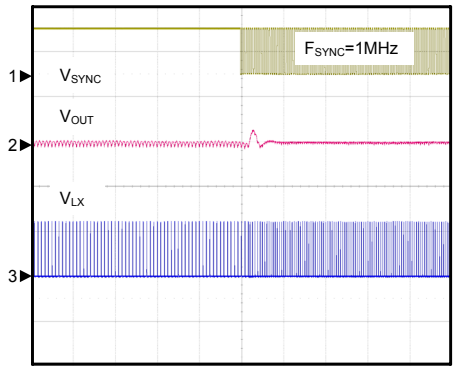


CH1: V_{OUT}, 200mV/Div, AC
CH2: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

Operating Waveforms (Cont.)

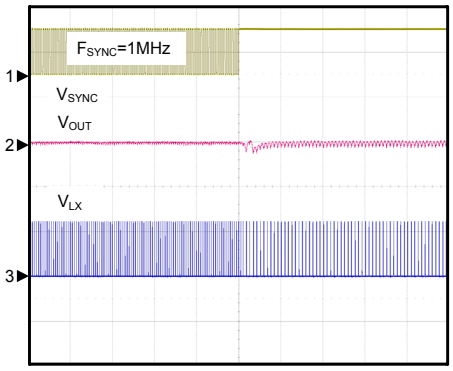
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

SYNC Transient



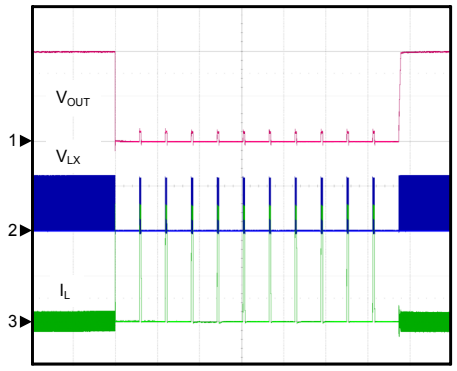
CH1: V_{SYNC}, 5V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: V_{LX}, 5V/Div, DC
TIME: 20µs/Div

SYNC Transient



CH1: V_{SYNC}, 5V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: V_{LX}, 5V/Div, DC
TIME: 20µs/Div

Short Circuit Protection

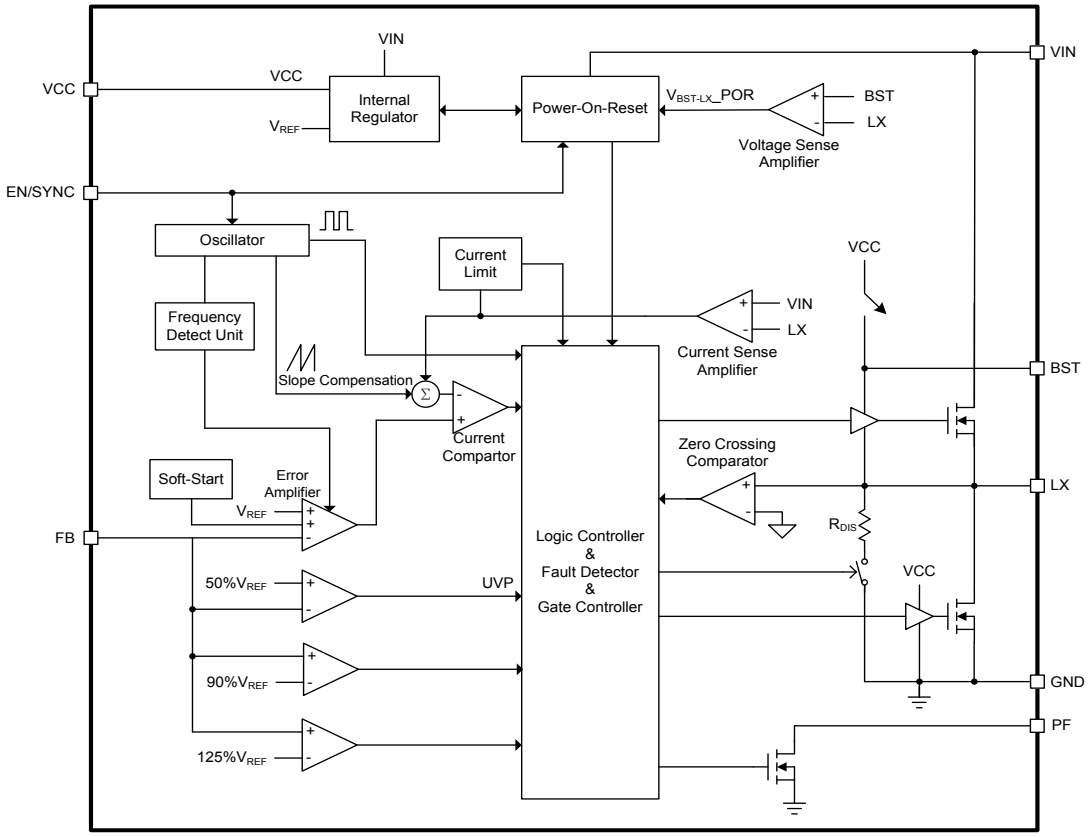


CH1: V_{OUT}, 500mV/Div, DC
CH2: V_{LX}, 10V/Div, DC
CH3: I_L, 2A/Div, DC
TIME: 20ms/Div

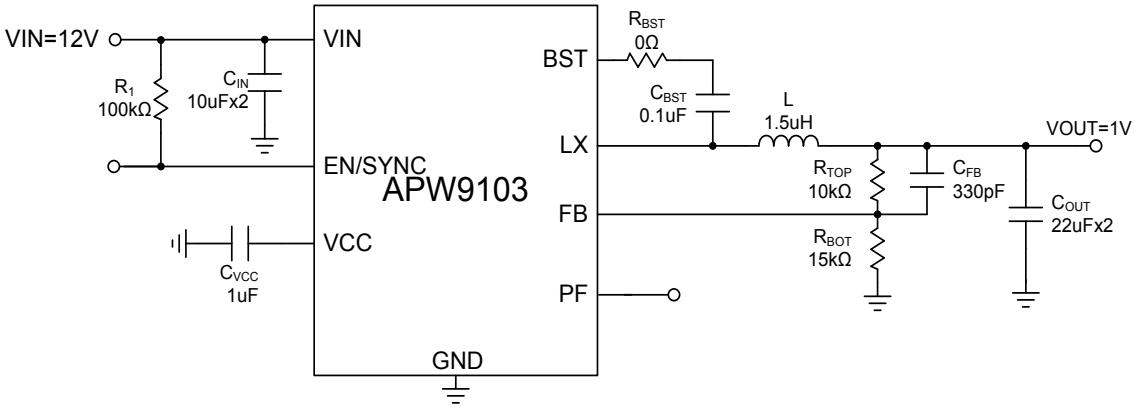
Pin Description

PIN		FUNCTION
NO.	NAME	
1	PF	Power Flag pin. The output is an open drain signal. When its final value, this pin is pulled high. This pin switches low when brown out threshold is reached.
2	VIN	Power Input Pin. VIN supplies the power to the buck converter.
3	LX	Power Switching Output. This pin is the junction of the high side power MOSFET and the low side power MOSFET. Connect this pin to the output inductor.
4	GND	Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance vias.
5	BST	High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
6	EN/SYNC	Enable/Synchronous Clock Input Pin. Drive EN high to turn the converter on and drive it low to turn it off. And Input an external clock signal to this pin for synchronization function.
7	VCC	Internal Regulator Output Pin. The VCC pin is the output of an internal 5V regulator for internal control circuitry. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
8	FB	Output Feedback Pin. FB senses the output voltage and regulates it. Connect the resistor divider from the output through FB to the ground to set the output voltage.

Block Diagram



Typical Application Circuit



Components Selection for Different Output Voltage

VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
12	0.8	0 ~ 3A	10µ × 2	1.5µ	22µ × 2	5.1k (1%)	15k (1%)	330p
12	1	0 ~ 3A	10µ × 2	1.5µ	22µ × 2	10k (1%)	15k (1%)	330p
12	1.8	0 ~ 3A	10µ × 2	2.2µ	22µ × 2	30k (1%)	15k (1%)	160p
12	3.3	0 ~ 3A	10µ × 2	4.7µ	22µ × 2	68k (1%)	15k (1%)	100p
12	5	0 ~ 3A	10µ × 2	4.7µ	22µ × 2	110k (1%)	15k (1%)	Open

Function Descriptions

Main Control Loop

The IC uses current mode control to regulate the output voltage. The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier. The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage. The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Under Voltage Lock Out (UVLO)

When the IC is powered up, the internal circuitry except VCC remains inactive until the VIN voltage exceeds the VIN UVLO high threshold voltage. When VIN is below the VIN UVLO low threshold voltage, the IC is turned off and the output discharge is triggered.

VCC Power-On-Reset (POR)

VCC is an internal voltage regulator that is activated when the IC is powered by VIN and EN goes high. The IC continuously monitors the voltage on the VCC pin. The soft start is activated, when the VCC voltage is higher than the POR threshold and the VIN voltage is higher than the UVLO threshold and the EN voltage is higher than the enable threshold.
VCC POR is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC POR also has hysteresis to resist ripple on the VCC voltage.

Over-Voltage Protection (OVP)

The IC monitors the output voltage through the FB pin to implement the OVP function. When the FB voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the FB voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures. Then the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot. The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Enable/Shutdown and Frequency synchronization

The IC provides the EN/SYNC pin, which is a digital input that turns the converter on or off. Drive EN/SYNC high to turn the converter on and drive it low to turn it off.
To synchronize the internal operating frequency of the IC with the external clock, connect the EN/SYNC pin to an external 50% duty cycle clock. The rising edge of the internal clock is synchronized with the rising edge of the external clock.

Over-Current-Protection and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit. When the current limit protection is activated, the output current will be limited and the output voltage will drop. When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode. In hiccup mode, the converter will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over current condition is removed, the IC will exit the hiccup mode.

Fast Discharge

When the EN signal goes low or the VIN voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered. The discharge MOSFET between the LX of the converter and ground is turned on, allowing the output capacitor to be quickly discharged through this MOSFET.

Power Flag (PF)

If its final value, the PF pin is pulled high through an external pull-up resistor.
Once the VIN voltage is below the UVLO low threshold, the PF pin will switch low.

DyncBandwidth™ Technology

DyncBandwidth, dynamic bandwidth compensation, is a technique to allow the converter running with the best transient response over a wide range of switching frequencies. When receiving an external clock, the converter will automatically adjust the internal compensation through the internal Frequency Detection Unit.

Application Information

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage.
Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients.
Since the input capacitor (CIN) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.
The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to filter the output and provide load transient current. The higher capacitance value will provide the smaller output ripple and better load transient.
Ceramic electrolytic capacitors with X5R or X7R dielectrics and low ESR are recommended to keep the output voltage ripple low. The output voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

Output Inductor Selection

The inductance value will determine the inductor ripple current and affects the load transient response and output ripple voltage.
The larger inductance value will result in a smaller ripple current, which will result in a lower output ripple voltage but a slower transient response, while a smaller inductance value will have opposite result.
A good rule is to choose the inductor ripple current that is about 30% of the maximum output current. Use the following equation to derive the inductance value for most designs:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

To avoid inductor saturation, the inductor current rating should be at least the converter's maximum output current plus the inductor ripple current. The maximum inductor peak current can be estimated by:

$$I_{L(MAX)} = I_{OUT} + \frac{\Delta I_L}{2}$$

In addition, choosing an inductor with a smaller DCR will provide better efficiency, and it is recommended that the inductor's DCR should be less than 15m ohms.

Output Voltage Setting

The output voltage is set by a resistor voltage divider between output terminal and ground. For detailed voltage divider settings, please refer to "Typical Application Circuits" The output voltage can be calculated as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Application Information (Cont.)

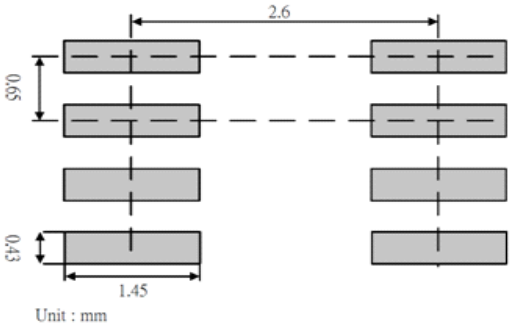
Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The VIN input capacitor should be placed close to the VIN and PGND pins. Connecting the capacitor and VIN/PGND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN / PGND to capacitor less than 2mm respectively is recommended.
2. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
3. The ground of the output capacitor and input capacitor and the PGND of the IC should be as close as possible.
4. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
5. For better heat dissipation, it is strongly recommended to enlarge the thermal pad area as much as possible and place a large ground plane on each PCB layer below the thermal pad position, and place as many vias as possible from the top layer to the bottom layer on the thermal pad and around the ground plane.
6. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the PGND of the IC.

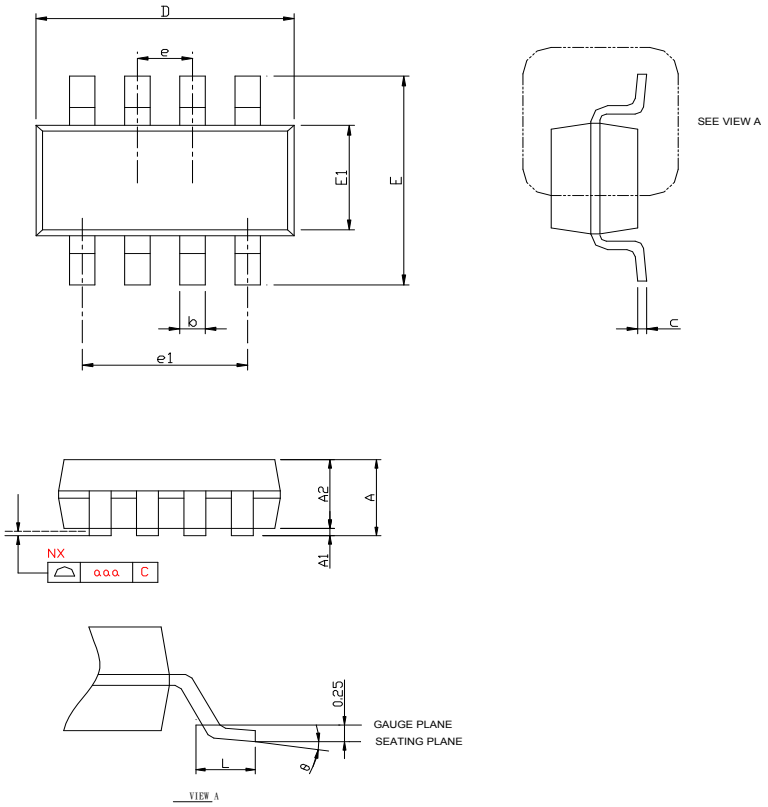
Recommended Minimum Footprint

(Top View)



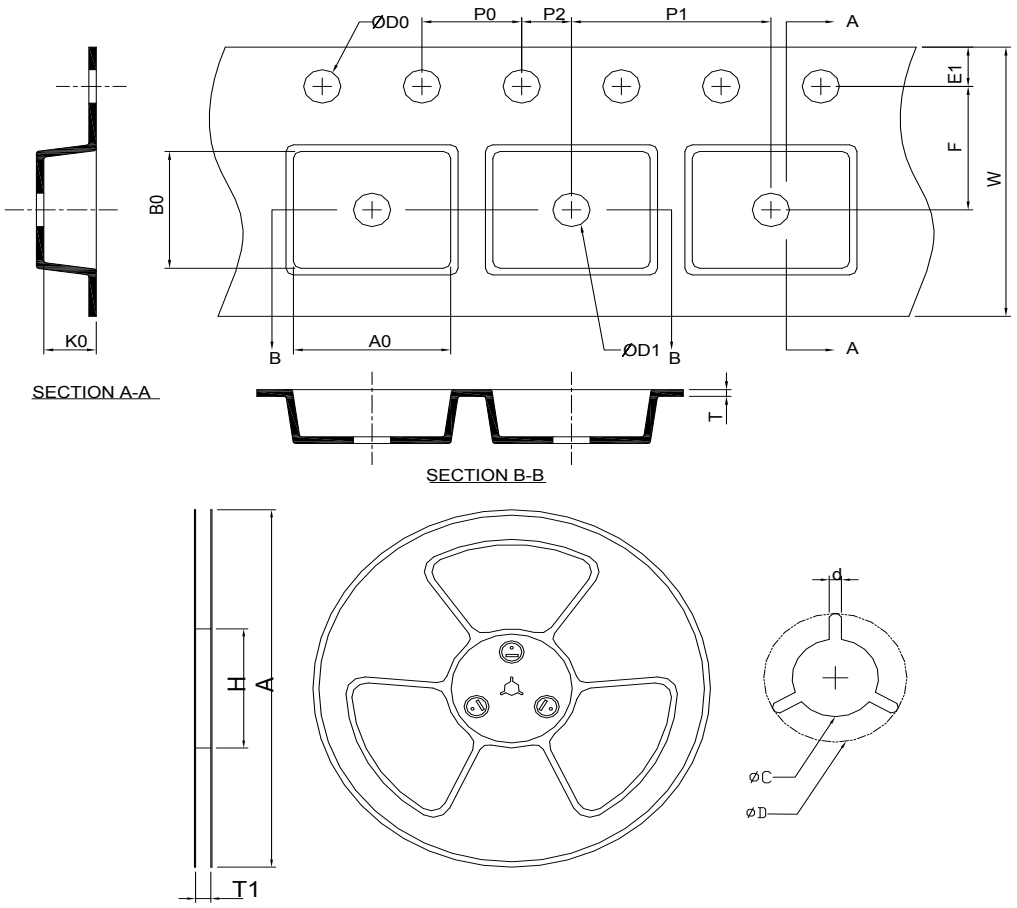
Package Information

TSOT-23-8A



SYMBOL	TSOT-23-8A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.01	0.10	0.000	0.004
A2	0.70	0.90	0.028	0.035
b	0.22	0.40	0.009	0.016
c	0.08	0.20	0.003	0.008
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.65 BSC		0.026 BSC	
e1	1.95 BSC		0.077 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSOT 23-8(A)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.20±0.20

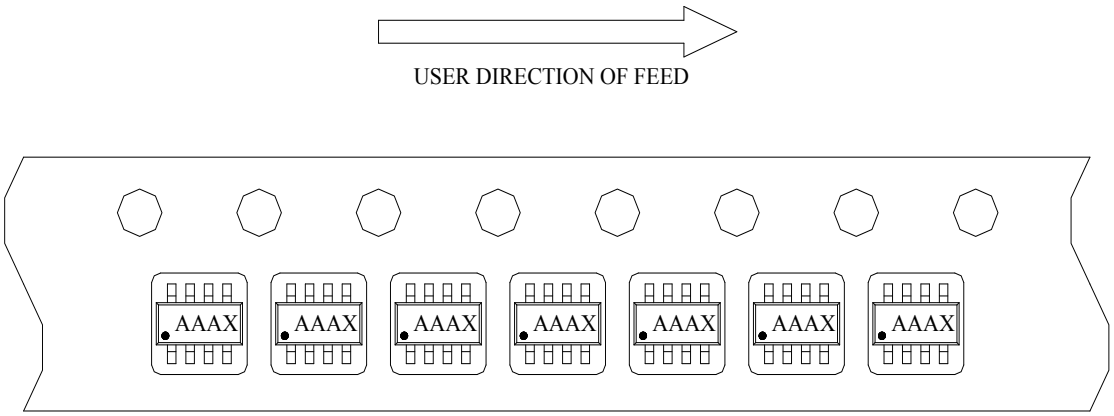
(mm)

Devices Per Unit

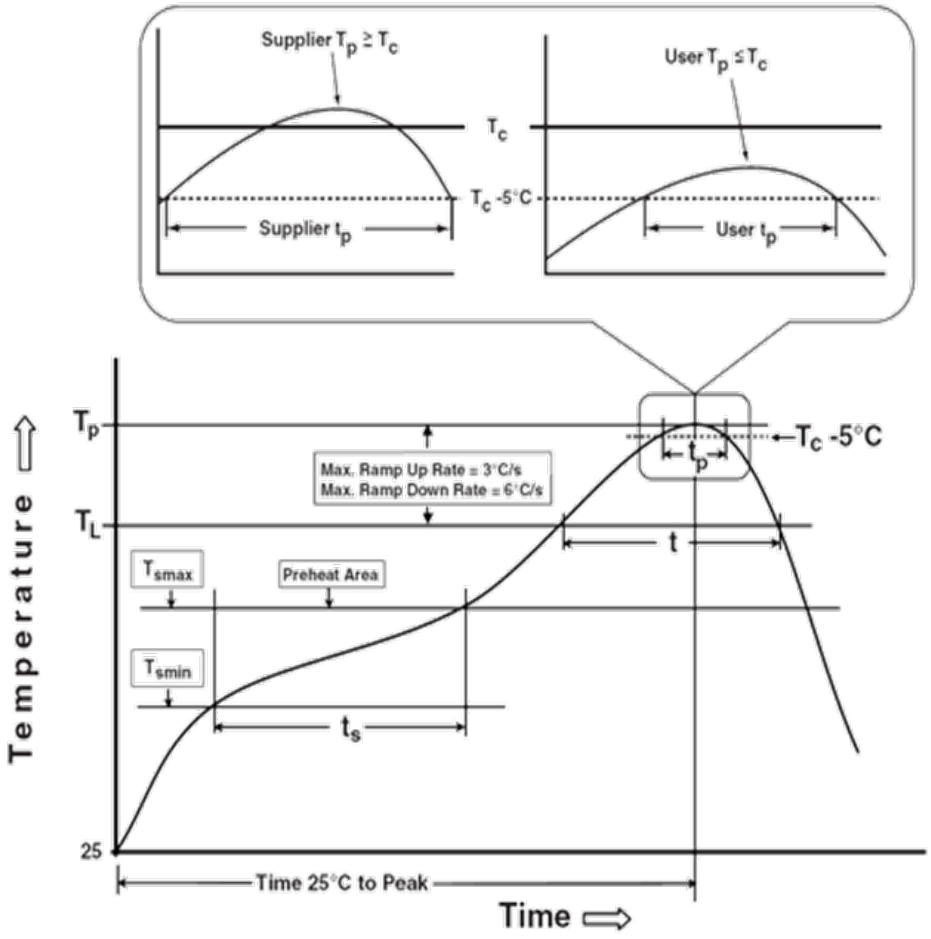
Package type	Packing	Quantity
TSOT-23-8(A)	Tape & Reel	3000

Taping Direction Information

TSOT-23-8A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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