High Efficiency 18V, 2-CH Buck Converter

Features

- **Input Voltage range : 4.5V to 18V.**
- **3A/2A Output Current on Channel1/2.**
- **Low I_Q=155μA (typ.) to improve Light Load Efficiency**
- **Typical 0.6V ±1% Internal Reference Voltage.**
- **Optimized Upper and Lower MOSFETs R_{DS_on} for max Efficiency:**
  - **N-CH MOSFET (95 mΩ) for CH1 High Side.**
  - **N-CH MOSFET (50 mΩ) for CH1 Low Side.**
  - **N-CH MOSFET (105 mΩ) for CH2 High Side.**
  - **N-CH MOSFET (60 mΩ) for CH2 Low Side.**
- **Channel Swap Function (APW9202S)**
- **Level Shifter Output is Referenced to External DC Voltage (APW9202L)**
- **Built in OVP, UVP, Current Limit and OTP.**
- **Low Cost VTQFN-13 package.**
- **Lead Free and Green Devices Available (RoHS Compliant).**
- **DyncBandwidth™ Technology**

General Description

The APW9202/S/L is a two-channel synchronous mode PWM converter with 3A continuous current capability for one channel and 2A continuous current capability for the other one.

Each channel of the APW9202/S has independent enable, and it also allows the two regulators to start together by using the same enable signal. Although the switching frequency of the APW9202/S/L is fixed at 800kHz, it can also change the switching frequency via the PWM/SYNC pin.

Another feature of this part is its ability to automatically optimize its BW (DyncBandwidth) to allow better dynamic response once it is synchronized to a higher external clock.

The APW9202/S/L also provides a 180-degree phase shifting technique to minimize switching noise. The output voltage of each channel can be adjusted using an external resistor divider. Other features include UVP, current limit, and OTP.

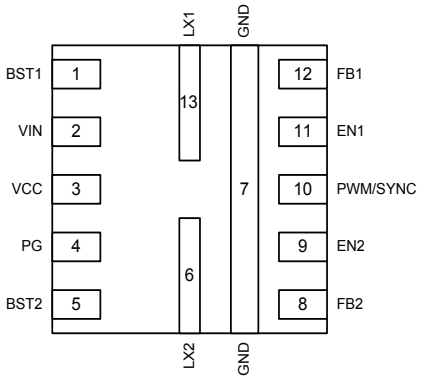
The APW9202/S/L is available in a VTQFN-13 package with small size and excellent thermal capacity.

Applications

- **Set-Top-Box**
- **Passive Optical Network**
- **Router**
- **Digital Subscriber Line**
- **G.Fast**

Pin Configuration (Top View)

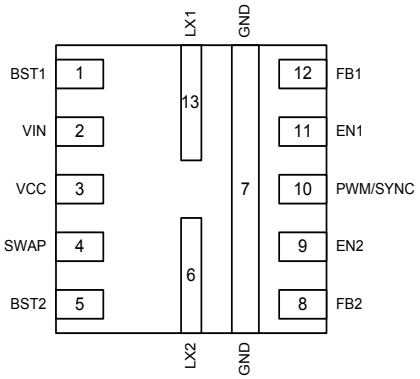
APW9202



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

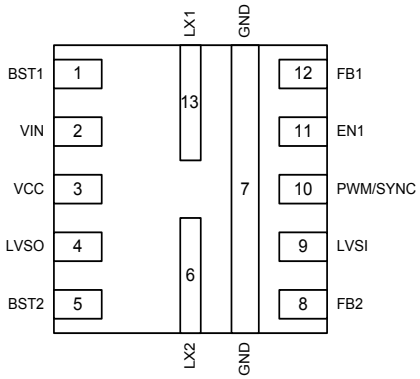
Pin Configuration (Top View)

APW9202S



Pin Configuration (Top View)

APW9202L



Ordering and Marking Information

APW9202 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF: VTQFN2*2-13 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW9202 QF : 9202 X	X - Date Code

APW9202S □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF: VTQFN2*2-13 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW9202S QF : 202S X	X - Date Code

APW9202L □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QF: VTQFN2*2-13 Operating Ambient Temperature Range I : -40 to 85° C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW9202L QF : 202L X	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

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Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{VIN}	VIN to GND		-0.3 ~ 20	V
V_{BS}	BST1/2 to LX1/2		-0.3 ~ 5.5	V
V_{LX}	LX1/2 to GND	>10ns	-0.6 ~ 20	V
		<10ns	-6 ~ 22	V
$V_{I/O}$	VCC, EN1/2, FB1/2, PWM/SYNC, PG, LVSI, LVSO and SWAP to GND		-0.3 ~ 6	V
PD	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	75	°C/W
θ_{JA}	Junction-to-Ambient Resistance (Note 3)	32	°C/W

Note 2: θ_{JA} is measured on 4 layers test board following the EIA/JESD51-7.
Note 3: θ_{JA} is measured on Anpec evaluation board in free air.

Recommended Operation Conditions (Note 4)

Symbol	Parameter		Range	Unit
VIN	VIN supply voltage		4.5 ~ 18	V
V_{ENx}	ENx input voltage		0 ~ 5	V
$V_{PWM/SYNC}$	PWM/SYNC input voltage		0 ~ 5	V
I_{OUT}	Converter output current	CH1	0 ~ 3	A
		CH2	0 ~ 2	
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 4: Refer to the typical application circuit.

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Electrical Characteristics

Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
SUPPLY						
V_{UVLO_R}	UVLO Upper Threshold	VIN Rising	-	4.2	-	V
V_{UVLO_HYS}	UVLO Hysteresis Voltage	VIN Falling	-	0.45	-	V
I_{VIN_SHDN}	VIN Shutdown Current	EN=GND	-	3	-	μA
EN THRESHOLD						
V_{EN_H}	EN Input Threshold High Voltage		1.2	1.4	1.6	V
V_{EN_HYS}	EN Input Hysteresis Voltage		-	0.2	-	V
T_{D_EN}	EN Turn On Delay Time	When EN High to LX Switching (Note 5)	-	700	-	μs
$T_{DB\_EN\_OFF}$	EN Turn Off Debounce Time	EN goes low to VOUT disable	-	15	-	μs
I_{EN}	EN Input Current	EN=VCC	-	1	-	μA
R_{DIS}	Discharge Resistor	VCC=5V, EN=Low		15		Ω
VCC and REGULATOR						
V_{POR}	VCC POR Threshold Voltage	VCC Rising	-	4.3	-	V
V_{POR_HYS}	VCC POR Hysteresis Voltage	VCC Falling	-	0.4	-	V
V_{REF}	Reference Voltage	T_J=25°C	594	600	606	mV
	Load Regulation	VOUT1=5V/0~2.5A, VOUT2=3.3V/0~2A	-	1	-	%
V_{VCC}	VCC Regulator Output Voltage	I_{VCC}=0A	-	5	-	V
	VCC Load Regulation	I_{VCC}=10mA	-	3	-	%
	VCC Maximum Current	When VCC drop to 4.75V	40	-	-	mA
t_{SS}	Channel Output Soft Start Time	VOUT from 0% to 90%	-	1	-	ms
OSCILLATOR FREQUENCY						
F_{OSC}	Oscillator Frequency		-	800	-	kHz
	Frequency Accuracy	T_J=-40~125°C	-20	-	+20	%
	Minimum on Time		-	55	-	ns
	Maximum Duty		-	80	85	%
PHASE SHIFT						
	CH1 and CH2 Phase Shift		-	180	-	degree
POWER MOSFET (for CH1, CH2)						
	CH1 High Side MOSFET Resistance		-	95	-	mΩ
	CH1 Low Side MOSFET Resistance		-	50	-	mΩ
	CH2 High Side MOSFET Resistance		-	105	-	mΩ
	CH2 Low Side MOSFET Resistance		-	60	-	mΩ
	High Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=GND	-	1	-	μA
	Low Side MOSFET Leakage Current	V_{EN}=0V, V_{LX}=VIN	-	1	-	μA

Note 5: Only the first output voltage has EN Turn ON Delay Time.

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Electrical Characteristics (Cont.)

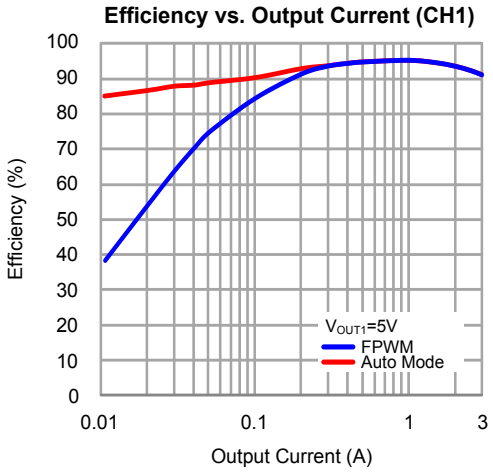
Unless otherwise specified, these specifications apply over VIN=12V, T_A=25°C

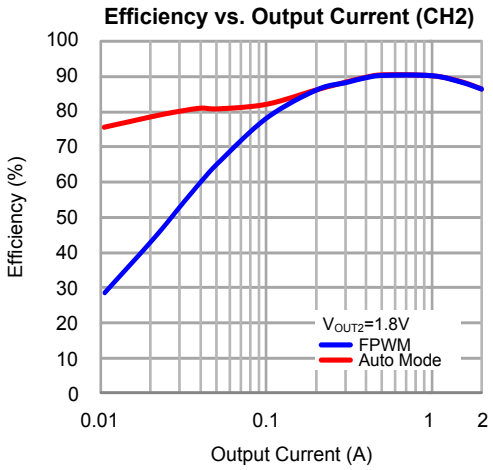
Symbol	Parameter	Test condition	Specification			Unit
			Min.	Typ.	Max.	
BOOTSTRAP POWER						
R_{BST}	BST Switch On Resistance		-	10	-	Ω
	BST Leakage Current	V_{BST-LX}=5V	-	-	1	μA
PROTECTIONS						
I_{LIM}	High Side MOSFET current-limit	For CH1		5		A
		For CH2		4		
	Over-temperature Trip Point	(Note 6)	-	150	-	°C
	Over-temperature Hysteresis	(Note 6)	-	30	-	°C
	Under Voltage Protection		40	50	60	%V_{REF}
	Hiccup Count Ratio		-	10.5	-	
PWM/SYNC						
	PWM/SYNC Input High Level	For SYNC Function	1.8	-	-	V
	PWM/SYNC Input Low Level	For SYNC Function	-	-	0.25	V
F_{SYNC}	SYNC Frequency Range		500	-	2000	kHz
Power Good (APW9202)						
	PG High Threshold	VOUT rising, PG in from lower (PG goes high)	-	90	-	%
	PG High Threshold Hysteresis	VOUT falling, PG low hysteresis (PG goes low)	-	6	-	%
	PG Leakage Current	VPG =VCC	-	-	1	uA
	PG Sink Capability	When PG pin pull low, PG pin sink 30mA	-	-	0.4	V
Channel Swap (APW9202S)						
V_{SWAP_H}	SWAP Input Threshold High Voltage		-	1	-	V
V_{SWAP_HYS}	SWAP Input Hysteresis Voltage		-	0.25	-	V
R_{SWAP}	SWAP Pull Low Resistor	VSWAP=2V	-	1	-	MΩ
Level Shifter (APW9202L)						
V_{LVSI_H}	LVSI Input Threshold High Voltage		1.2	1.4	1.6	V
V_{LVSI_HYS}	LVSI Input Hysteresis Voltage		-	0.2	-	V
I_{LVSI}	LVSI Input Current	VLVSI=VCC	-	1	-	μA
	LVSO Leakage Current	VLVSO =VCC	-	1	-	uA
	LVSO Sink Capability	When LVSO pin pull low, LVSO pin sink 30mA	-	-	0.4	V

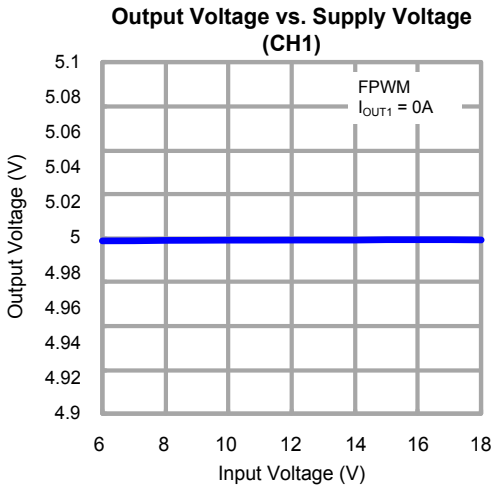
Note 6 : Guarantee by design

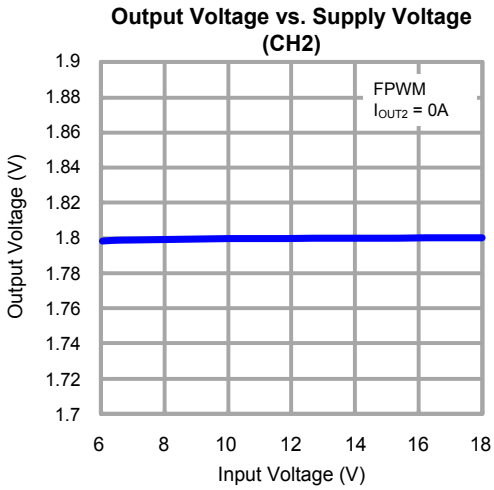
Typical Operating Characteristics

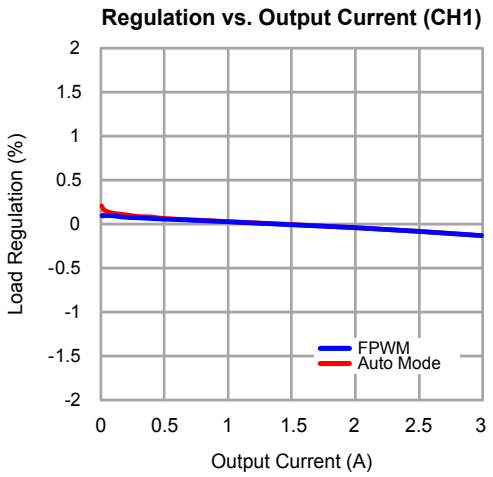
Refer to the typical application circuit. The test condition is V_{IN}=12V, V_{OUT1}=5V, V_{OUT2}=1.8V. L_1=4.7μH, L_2=3.3μH, C_{OUT}=22μF*2, T_A= 25°C unless otherwise specified.

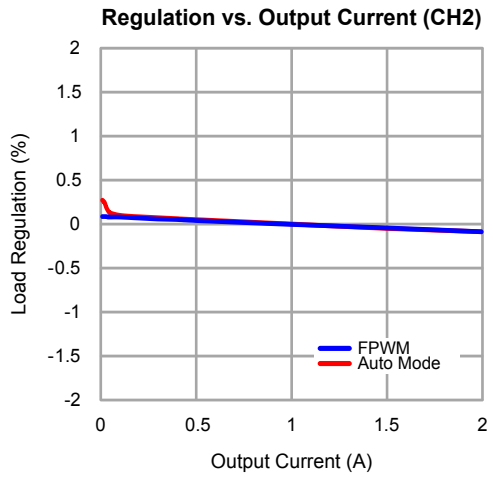








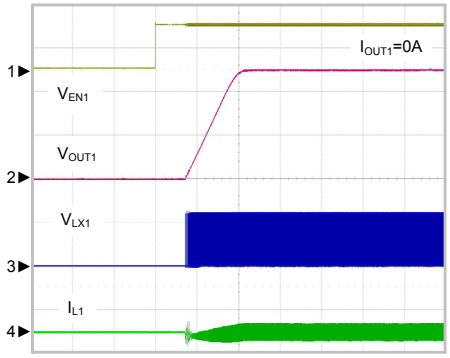




Operating Waveforms

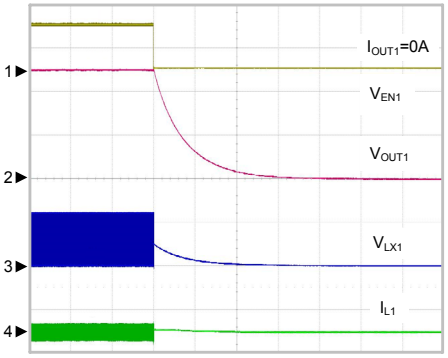
Refer to the typical application circuit. The test condition is V_{IN}=12V, V_{OUT1}=5V, V_{OUT2}=1.8V. L_1=4.7µH, L_2=3.3µH, C_{OUT}=22µF*2, T_A= 25°C unless otherwise specified.

CH1 Star-Up by Enable



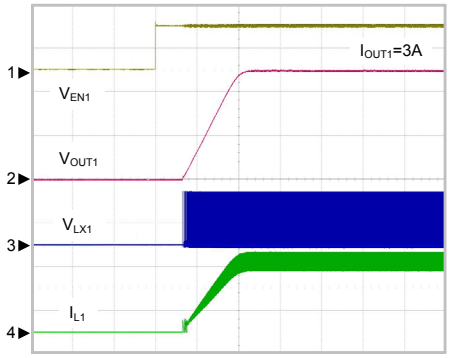
CH1: V_{EN1}, 5V/Div, DC
CH2: V_{OUT1}, 2V/Div, DC
CH3: V_{LX1}, 10V/Div, DC
CH4: I_{L1}, 2A/Div, DC
TIME: 1ms/Div

CH1 Shutdown by Enable



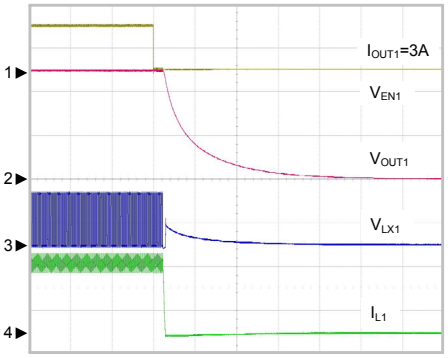
CH1: V_{EN1}, 5V/Div, DC
CH2: V_{OUT1}, 2V/Div, DC
CH3: V_{LX1}, 10V/Div, DC
CH4: I_{L1}, 2A/Div, DC
TIME: 1ms/Div

CH1 Star-Up by Enable



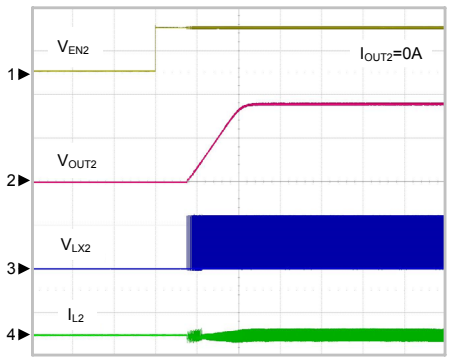
CH1: V_{EN1}, 5V/Div, DC
CH2: V_{OUT1}, 2V/Div, DC
CH3: V_{LX1}, 10V/Div, DC
CH4: I_{L1}, 2A/Div, DC
TIME: 1ms/Div

CH1 Shutdown by Enable



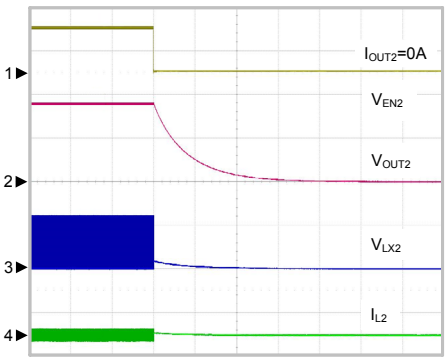
CH1: V_{EN1}, 5V/Div, DC
CH2: V_{OUT1}, 2V/Div, DC
CH3: V_{LX1}, 5V/Div, DC
CH4: I_{L1}, 2A/Div, DC
TIME: 50µs/Div

CH2 Star-Up by Enable



CH1: V_{EN2}, 5V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 2A/Div, DC
TIME: 1ms/Div

CH2 Shutdown by Enable



CH1: V_{EN2}, 5V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 2A/Div, DC
TIME: 1ms/Div

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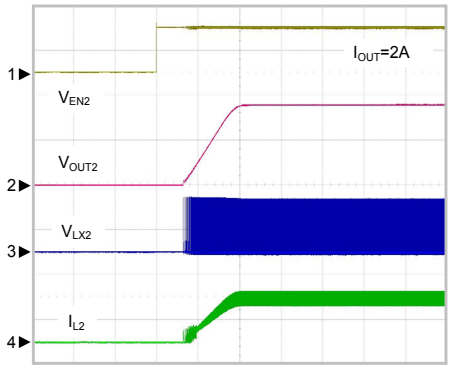
Operating Waveforms (Cont.)

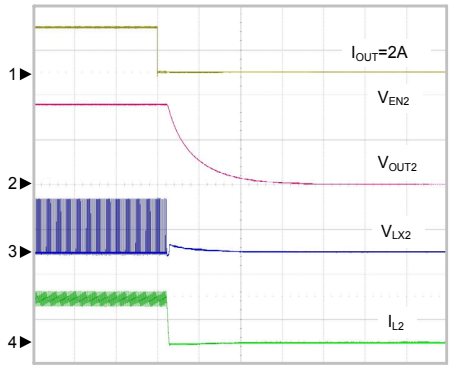
Refer to the typical application circuit. The test condition is V_{IN}=12V, V_{OUT1}=5V, V_{OUT2}=1.8V. L_1=4.7µH, L_2=3.3µH, C_{OUT}=22µF*2, T_A= 25°C unless otherwise specified.

CH2 Star-Up by Enable



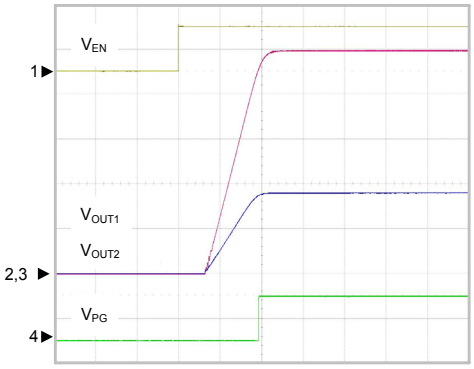
CH1: V_{EN2}, 5V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 2A/Div, DC
TIME: 1ms/Div

CH2 Shutdown by Enable



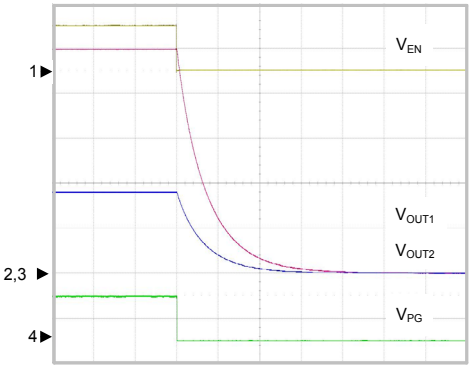
CH1: V_{EN2}, 5V/Div, DC
CH2: V_{OUT2}, 2V/Div, DC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 2A/Div, DC
TIME: 50µs/Div

Power On Sequence



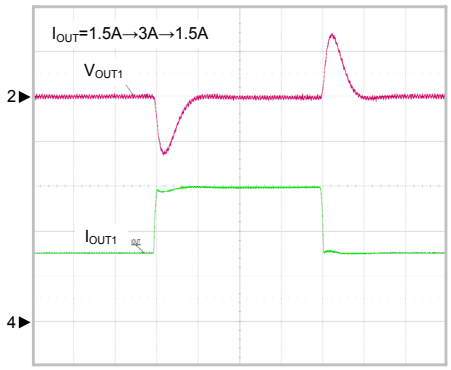
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 1ms/Div

Power Off Sequence



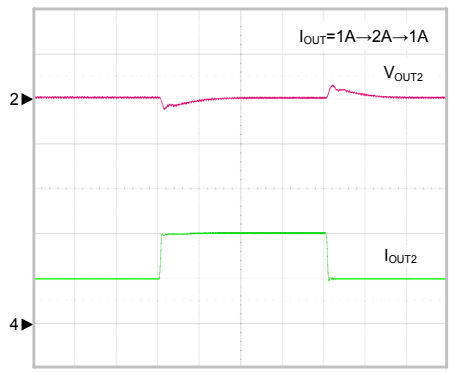
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT1}, 1V/Div, DC
CH3: V_{OUT2}, 1V/Div, DC
CH4: V_{PG}, 5V/Div, DC
TIME: 1ms/Div

Load Transient (CH1)



CH2: V_{OUT1}, 200mV/Div, AC
CH4: I_{OUT1}, 1A/Div, DC
TIME: 20µs/Div

Load Transient (CH2)

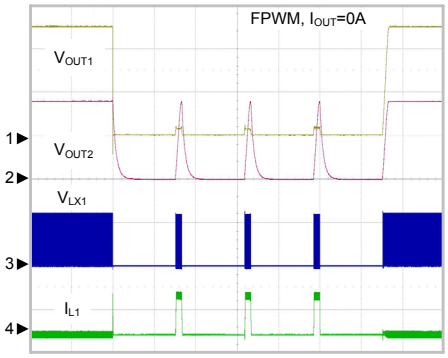


CH2: V_{OUT2}, 200mV/Div, AC
CH4: I_{OUT2}, 1A/Div, DC
TIME: 20µs/Div

Operating Waveforms (Cont.)

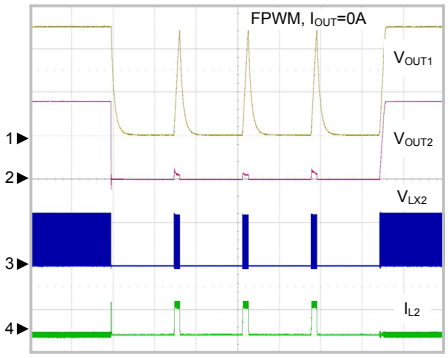
Refer to the typical application circuit. The test condition is V_{IN}=12V, V_{OUT1}=5V, V_{OUT2}=1.8V. L_1=4.7μH, L_2=3.3μH, C_{OUT}=22μF*2, T_A= 25°C unless otherwise specified.

CH1 Short Circuit Protection



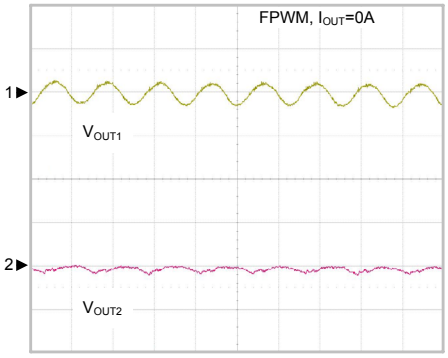
CH1: V_{OUT1}, 2V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{LX1}, 10V/Div, DC
CH4: I_{L1}, 5A/Div, DC
TIME: 10ms/Div

CH2 Short Circuit Protection



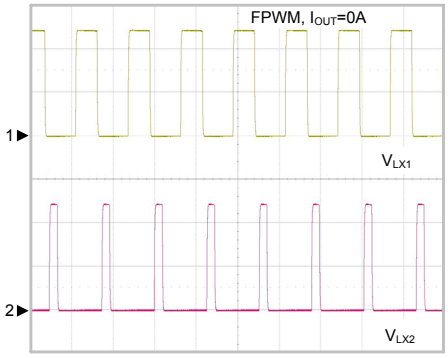
CH1: V_{OUT1}, 2V/Div, DC
CH2: V_{OUT2}, 1V/Div, DC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 5A/Div, DC
TIME: 10ms/Div

Output Ripple



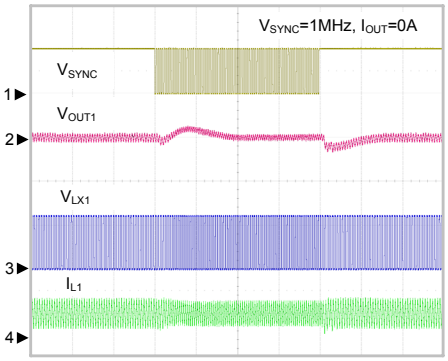
CH1: V_{OUT1}, 20mV/Div, AC
CH2: V_{OUT2}, 20mV/Div, AC
TIME: 1μs/Div

Phase Shift



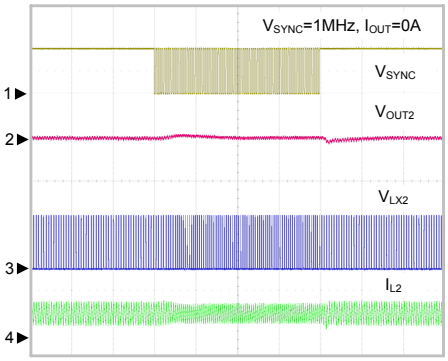
CH1: V_{LX1}, 5V/Div, DC
CH2: V_{LX2}, 5V/Div, DC
TIME: 1μs/Div

CH1 SYNC Transient



CH1: V_{SYNC}, 5V/Div, DC
CH2: V_{OUT1}, 50mV/Div, AC
CH3: V_{LX1}, 10V/Div, DC
CH4: I_{L1}, 1A/Div, DC
TIME: 20μs/Div

CH2 SYNC Transient



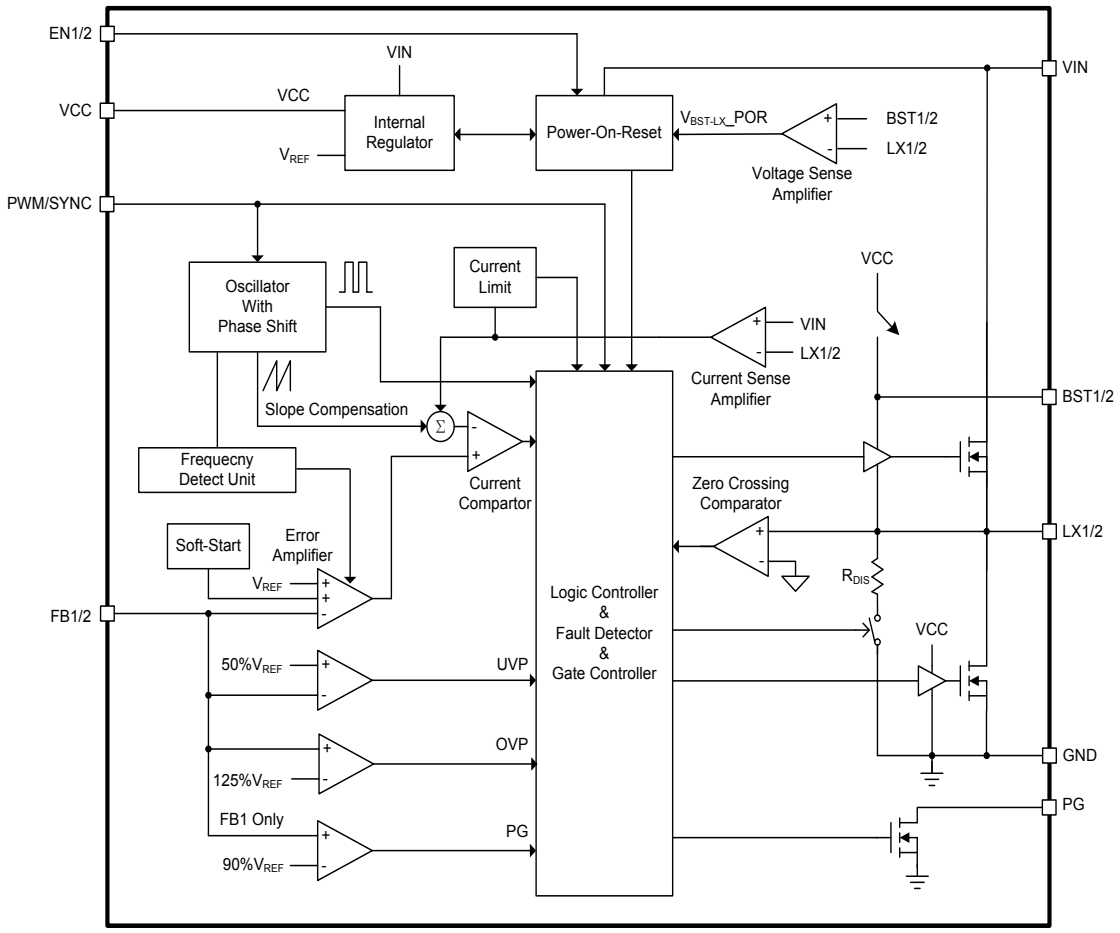
CH1: V_{SYNC}, 5V/Div, DC
CH2: V_{OUT2}, 50mV/Div, AC
CH3: V_{LX2}, 10V/Div, DC
CH4: I_{L2}, 1A/Div, DC
TIME: 20μs/Div

Pin Descriptions

PIN				FUNCTION
APW9202 NO.	APW9202S NO.	APW9202L NO.	NAME	
1	1	1	BST1	CH1 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX1 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
2	2	2	VIN	Power Input Pin. The VIN supplies the two step-down converter switches. Connect a ceramic bypass capacitor from VIN to GND.
3	3	3	VCC	Internal Regulator Output Pin. The VCC pin is the output of an internal 5V regulator for internal control circuitry. It is recommended to connect a 1uF X5R capacitor from the VCC pin to ground to ensure stability and regulation. Do not apply an external load to VCC.
4	-	-	PG	Output Power Good Indicator Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage for the PG function.
-	4	-	SWAP	Channel Swap Pin. This pin controls the order in which the high side MOS of both channels is turned on in one cycle. When this pin is low, Ch1 turns on first; when this pin is high, it turns on ch2 first. And SWAP pin cannot be left floating
-	-	4	LVSO	Level Shifter Output Pin. This pin is an open-drain device; connect a pull-up resistor to an external supply voltage.
5	5	5	BST2	CH2 High-Side Gate Driver Supply Voltage Input Pin. A 0.1uF X5R ceramic capacitor is connected from this pin to the LX2 pin to provide a bootstrap voltage for the gate driver to drive the upper MOSFET.
6	6	6	LX2	CH2 Power Switching Output. These pins are the junction of the high side power MOSFET and the low side power MOSFET. Connect these pins to the output inductor.
7	7	7	GND	Power Ground. This pin must be connected directly to the GND plane of the PCB using low inductance large vias. In order to get better thermal dissipation, all layers, top to bottom, below to GND PAD define as PAD plane and connected by via holes.
8	8	8	FB2	CH2 Output Feedback Pin. FB2 senses the output voltage of channel2 and regulates it. Connect the resistor divider from the output through FB2 to the ground to set the output voltage.
9	9	-	EN2	CH2 Enable Input Pin. Drive EN2 high to turn the CH2 converter on and drive it low to turn it off. The EN2 pin cannot be left floating.
-	-	9	LVSI	Level Shifter Input Pin
10	10	10	PWM/ SYNC	Auto Mode and FPWM selection / Synchronous Clock Input Pin. For operating mode selection, when this pin is logic high, the converter operates in Force PWM Mode. When this pin is logic low, the converter operates in automatic PWM/PSM mode. For SYNC function, connecting this pin to an external clock will synchronize the switching frequency to the external clock and put the converter in Force PWM Mode. And PWM/SYNC pin cannot be left floating.
11	11	-	EN1	CH1 Enable Input Pin. Drive EN1 high to turn the CH1 converter on and drive it low to turn it off. The EN1 pin cannot be left floating.
-	-	11	EN	IC Enable Input Pin. Drive EN high to turn the CH1 and CH2 converter on and drive it low to turn them off. The EN pin cannot be left floating.
12	12	12	FB1	CH1 Output Feedback Pin. FB1 senses the output voltage of channel1 and regulates it. Connect the resistor divider from the output through FB1 to the ground to set the output voltage.
13	13	13	LX1	CH1 Power Switching Output. These pins are the junction of the high side power MOSFET and the low side power MOSFET. Connect these pins to the output inductor.

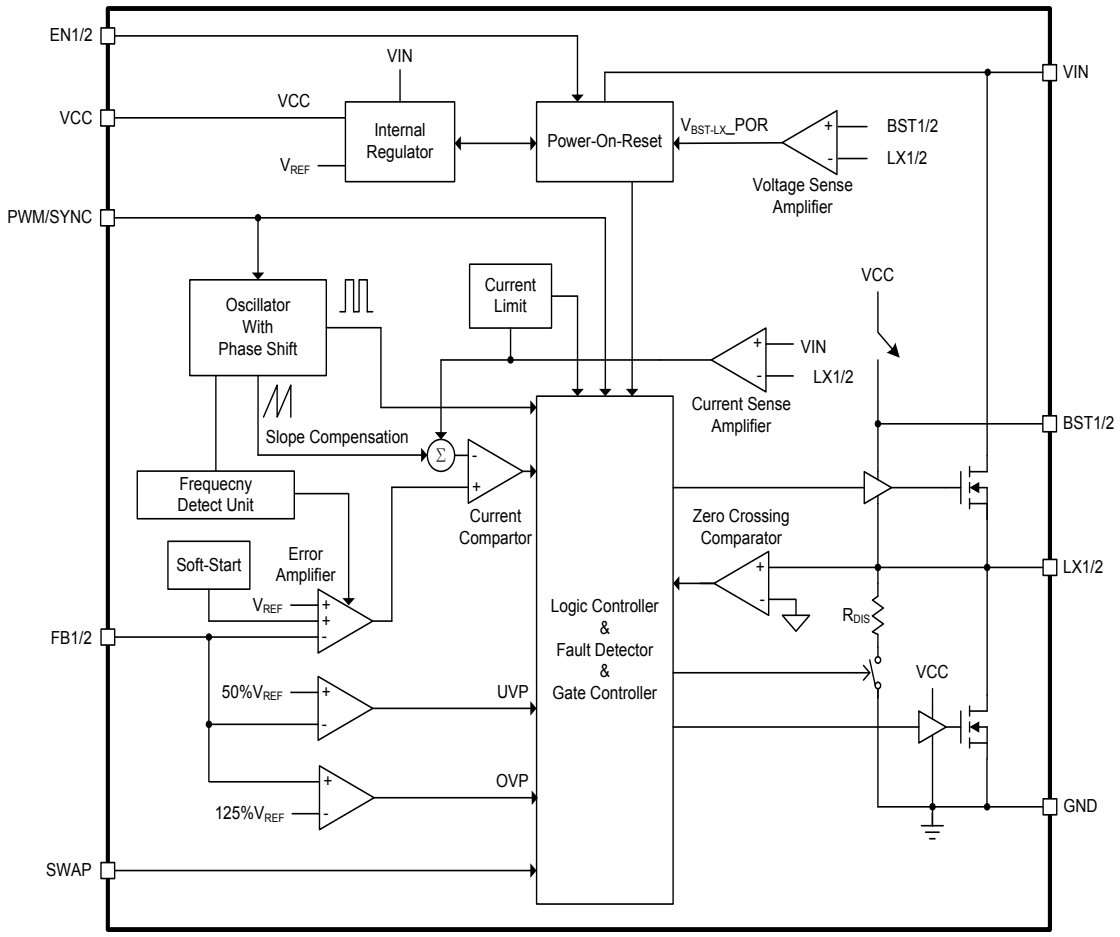
Block Diagram (Shows only one channel for regulator function)

APW9202



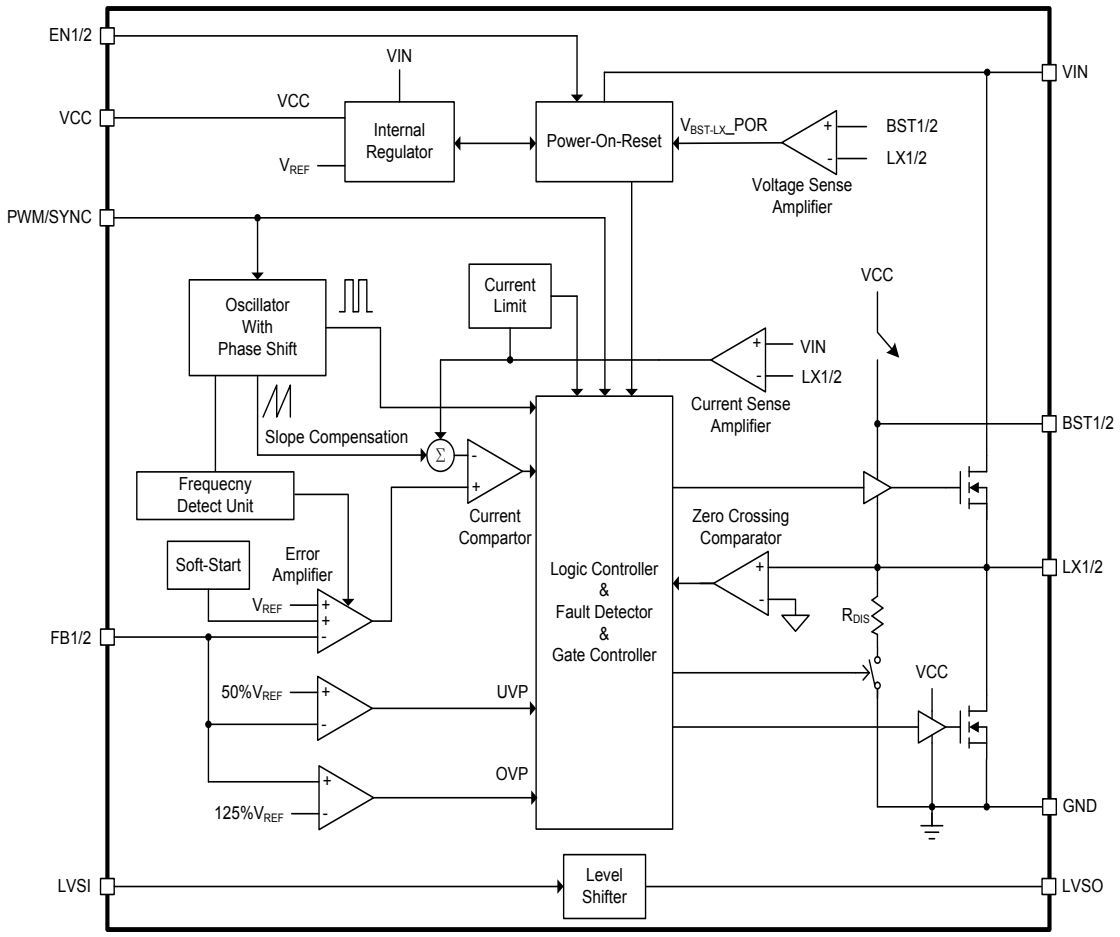
Block Diagram (Shows only one channel for regulator function)(Cont.)

APW9202S



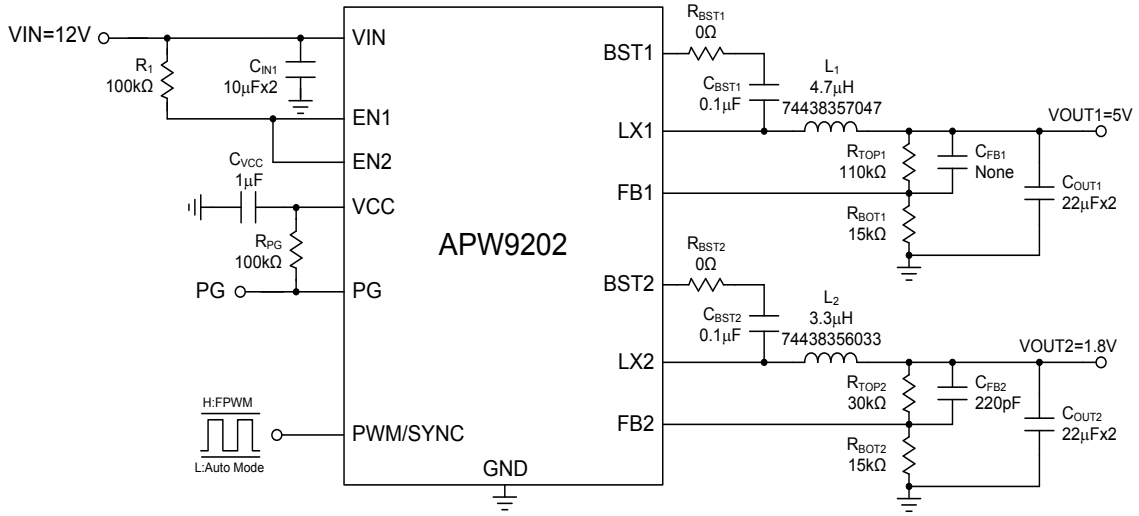
Block Diagram (Shows only one channel for regulator function)(Cont.)

APW9202L

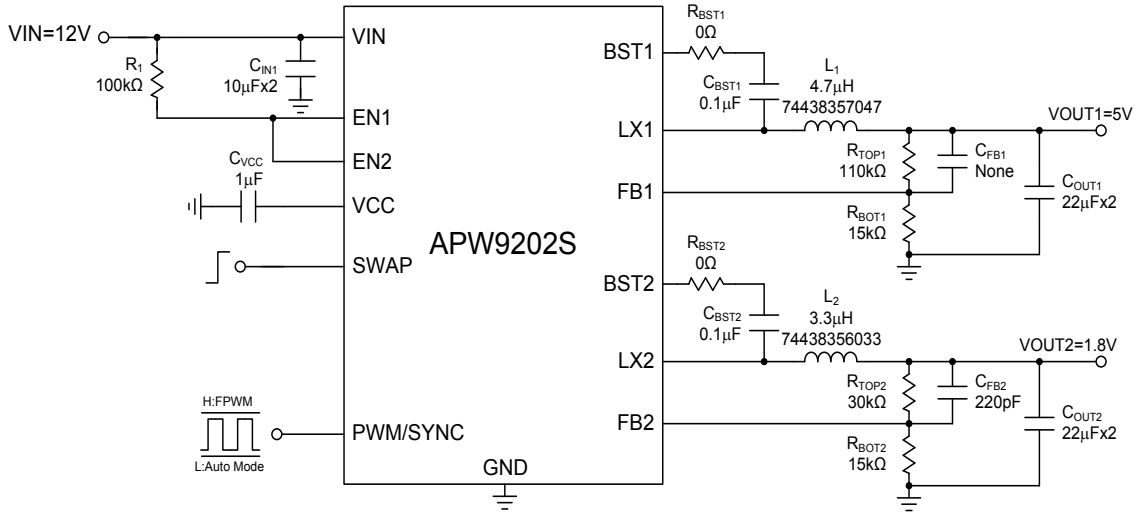


Typical Application Circuit (VOUT1/2: 5V/1.8V)

APW9202

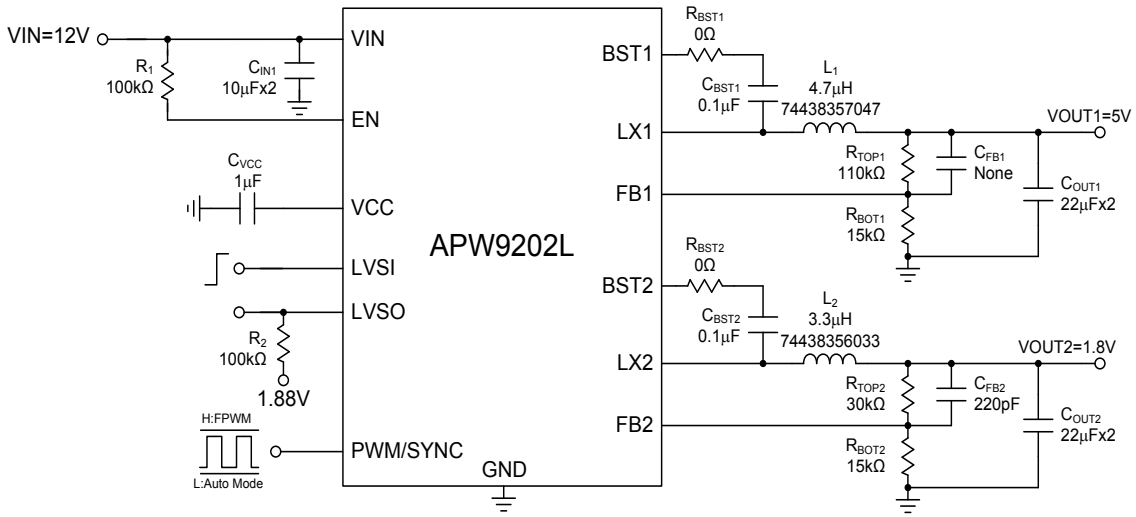


APW9202S



Typical Application Circuit (VOUT1/2: 5V/1.8V)(Cont.)

APW9202L



Components Selection for Different Output Voltage

Application	Channel	VIN (V)	VOUT (V)	IOUT (A)	C_{IN} (F)	L (H)	C_{OUT} (F)	R_{TOP} (Ω)	R_{BOT} (Ω)	C_{FB} (F)
1	1	12	5	0 ~ 3	10µ × 2	4.7µ	22µ × 2	110k	15k	Open
	2	12	1.8	0 ~ 2	10µ × 2	3.3µ	22µ × 2	30k	15k	220p
2	1	12	3.3	0 ~ 3	10µ × 2	3.3µ	22µ × 2	68k	15k	100p
	2	12	1.35	0 ~ 2	10µ × 2	2.2µ	22µ × 2	15k	12k	330p
3	1	12	1	0 ~ 3	10µ × 2	1.5µ	22µ × 2	10k	15k	330p
	2	12	2.5	0 ~ 2	10µ × 2	4.7µ	22µ × 2	47.5k	15k	120p

Function Description

Main Control Loop

The IC uses current mode control to regulate the output voltage. The output voltage is measured at FB through a resistor divider and amplified by an internal transconductance error amplifier. The output of the transconductance error amplifier is compared to the switching current to adjust the duty cycle to control the output voltage. The benefit of current mode control is the ability to quickly adjust the duty cycle as the output current increases rapidly for fast load transient response.

VIN Under-Voltage Lockout (UVLO)

The IC continuously monitors the voltage on the VIN pin. The soft start is activated when the VIN voltage and the EN voltage are above their respective UVLO thresholds.
VIN UVLO is used to protect the IC from erroneous operation with insufficient VIN voltage. VIN UVLO also has hysteresis to resist ripple on the VIN voltage.

VCC Power-On-Reset (POR)

VCC is an internal voltage regulator that is activated when the IC is powered by VIN and EN goes high. The IC continuously monitors the voltage on the VCC pin. The soft-start is activated when the VCC voltage is above the POR threshold and both VIN voltage and EN voltage are above their respective UVLO thresholds. VCC POR is used to protect the IC from erroneous operation with insufficient VCC voltage. VCC POR also has hysteresis to resist ripple on the VCC voltage.

Soft-Start

The IC has a built-in soft-start function that controls the rise time of the output voltage during start-up to reduce input current surges and prevent output overshoot. The soft start function will be enabled when any condition that can initiate an output start-up, such as VIN power to the
IC or toggle the EN pin, and when the converter is restarted from the OTP and hiccup mode.

Enable/Shutdown Controls

The IC provides two independent enable controls(EN1 and EN2) for the two converters(CH1 and CH2).The on and off of CH1 and CH2 are controlled by EN1 and EN2, respectively. Drive ENx high to turn the respective converter on and drive ENx low to turn the respective converter off. The APW9202L provides the EN pin, which is a digital input the turns the all converters on or off.

PWM / External Frequency Synchronizing

The PWM mode allows the converter to either operate in fixed frequency PWM mode or in an automatic Fixed frequency burst mode/ PWM mode. If this pin is left open or pulled HI, the IC will always be a in a fixed frequency mode regardless of the load current. This frequency will be either fixed internal frequency of 800kHz or the external sync clock frequency. If the PWM/SYNC pin is connected to GND, the IC is in the automatic fixed frequency burst/PWM mode.
Although the switching frequency of the IC is fixed at 800kHz, it can also change the switching frequency via the PWM/SYNC pin. When an external clock is input to the PWM/SYNC pin, the IC can synchronize the switching frequency of the converter with the external clock frequency, which can be synchronized from 500 Hz to 2 MHz.

Single Frequency and Phase shift

The IC has two converters that use the same operating frequency to avoid beat frequencies and improve noise immunity.
But it also increases input current and EMI, so more input capacitors and additional EMI components must be used. Therefore, the IC provides a 180-degree phase shifting technique that allows two high-side power MOSFETs to be turned on at different times to eliminate these defects. It will greatly reduce the RMS input current, resulting in less input capacitance, EMI components and input losses.

Current Limit and Hiccup

The IC monitors the current through the high-side power MOSFET to limits the peak inductor current to prevent IC from being damaged in the event of an overload or short circuit.
When the current limit protection is activated, the output current will be limited and the output voltage will drop. When the output voltage drops below the UVP threshold, UVP is triggered and the converter enters hiccup mode.
In hiccup mode, the converter will restart periodically. This protection mode is especially useful when the output is shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the IC. Once the over current condition is removed, the IC will exit the hiccup mode.

Over-Temperature Protection (OTP)

The IC features over-temperature protection to monitor junction temperature and prevent damage to the chip when operating at extremely high temperatures.
When the junction temperature exceeds the OTP threshold, the IC will be turned off to lower the junction temperature. The OTP circuit has hysteresis that allows the IC to restart when the junction temperature is below the OTP low threshold temperature.

Over-Voltage Protection (OVP)

The IC monitors the output voltage through the VOUT pin to implement the OVP function. When the VOUT voltage exceeds the OVP high threshold voltage, OVP will be triggered and the IC will be turned off until the VOUT voltage is lower than the OVP low threshold voltage. At this time, the OVP will be disabled and the IC will resume normal operation.

Fast Discharge

When the EN signal goes low or the VIN voltage falls below the UVLO threshold, the IC is turned off and the output fast discharge is triggered.
The discharge MOSFET between the VOUT and ground is turned on, allowing the output capacitor to discharge quickly through this MOSFET.

Crosstalk between LX1/2

Crosstalk between switching nodes SW1, SW2 can sometimes cause unstable switching waveforms and unexpectedly large input and output voltage ripple.
For example, when both channels are operating with a duty cycle close to 50%, it is usually unavoidable in this case. The situation improves if the rising and falling edges of the switching node do not coincide.

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Function Description (Cont.)

Power Good Indicator (APW9202)

The IC has an open-drain PG pin that indicates the output regulation state. During soft start, PG goes high when CH1 output reach 90% of the target value. During normal operation, when CH1 output is less than 85% of the target voltage, the PG signal will be pulled low immediately. When the output returns to 90% of the target value, the PG will remain high again. Since PG is an open-drain pulldown device, it usually requires an external pull-up resistor; however, if the pin is not used, no resistor is necessary. Since PG is an open-drain pull-down device, it usually requires an external pull-up resistor; however, if the pin is not used, no resistor is necessary.

Channel Swap (APW9202S)

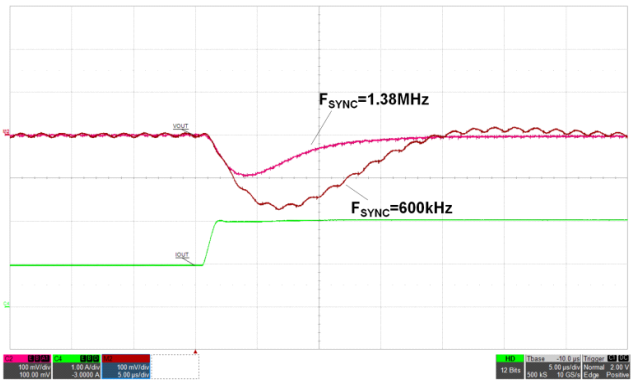
The IC has two functional modes. If set the SWAP low, when IC is synchronize the switching frequency, CH1 will synchronize than CH2 early. On the contrary, If set the SWAP high, CH2 will synchronize than CH1 early.

Level Shifter Function (APW9202L)

The IC has two functional modes. If set the LVSI High, which places the LVSO in a high impedance state. Setting the LVSI low, LVSO will be low. It must be connected to an external resistor pulled up to a voltage source below 5V on the system.

DyncBandwidth™ Technology

DyncBandwidth, dynamic bandwidth compensation, is a technique to allow the converter running with the best transient response over a wide range of switching frequencies. When receiving an external clock, the converter will automatically adjust the internal compensation through the internal Frequency Detection Unit.



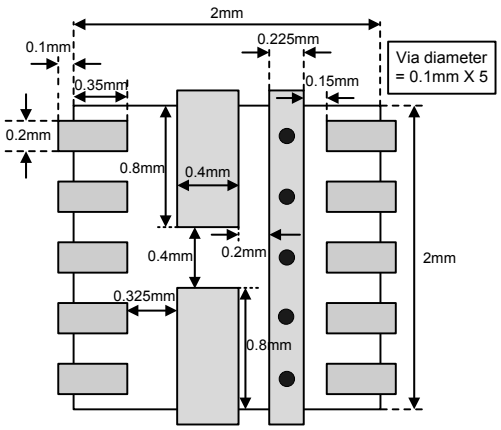
Application Information

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

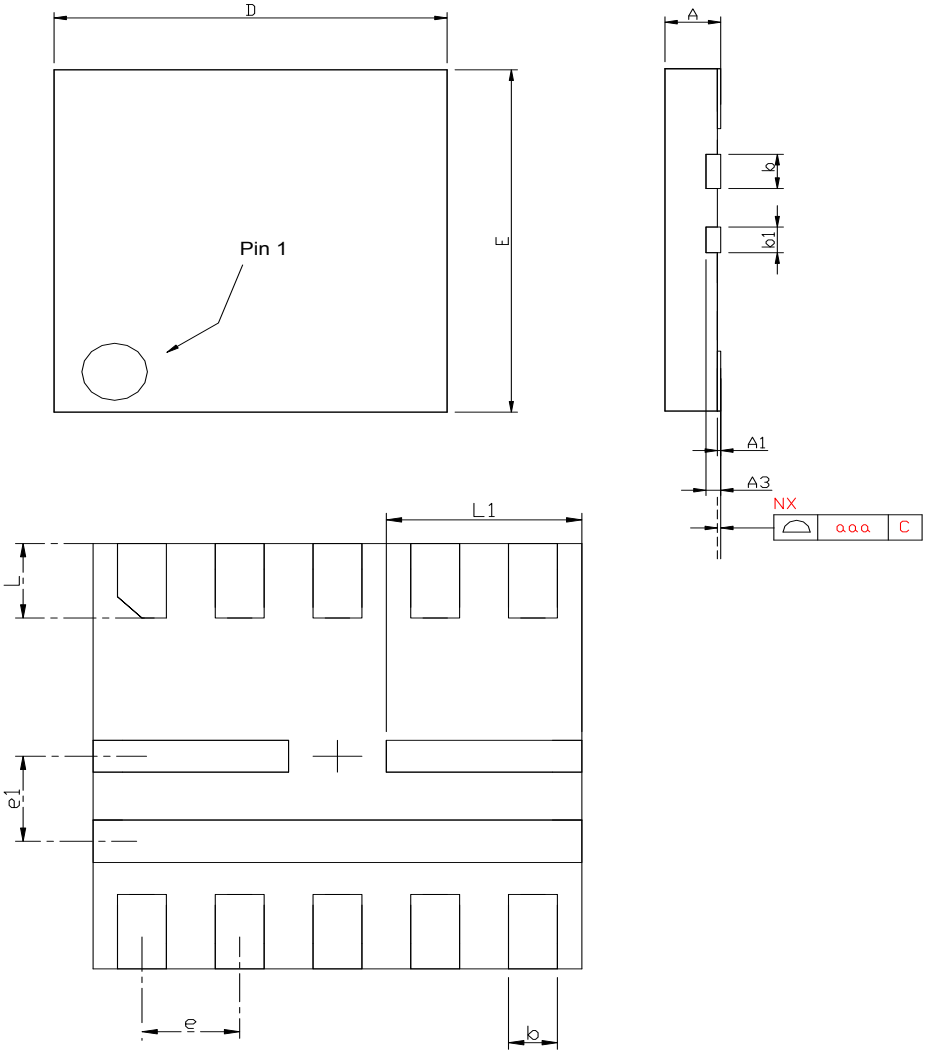
1. The VIN input capacitor should be placed close to the VIN and GND pins. Connecting the capacitor and VIN/ GND pins with short and wide trace without any via holes for good input voltage filtering. The distance between VIN/ GND to capacitor less than 2mm respectively is recommended.
2. Place the VCC capacitor to VCC pin and GND pin as close as possible.
3. Place the inductor as close as possible to the LX pin to minimize noise coupling into other circuits.
4. The ground of the output capacitor and input capacitor and the GND of the IC should be as close as possible.
5. Place the feedback resistor divider as close as possible to the FB pin to minimize FB high impedance trace. In addition, the FB pin trace cannot be routed close to the switching signal.
6. For better heat dissipation, it is highly recommended to place a large ground plane under the thermal pad of all PCB layers and place as many vias as possible on the thermal pad from the top layer to the bottom layer.
7. It is recommended to place the input capacitor, output capacitor and inductor on top layer, and use a large power GND plane to connect the ground of the input capacitor, the ground of the output capacitor, and the GND of the IC.

Recommended Minimum Footprint



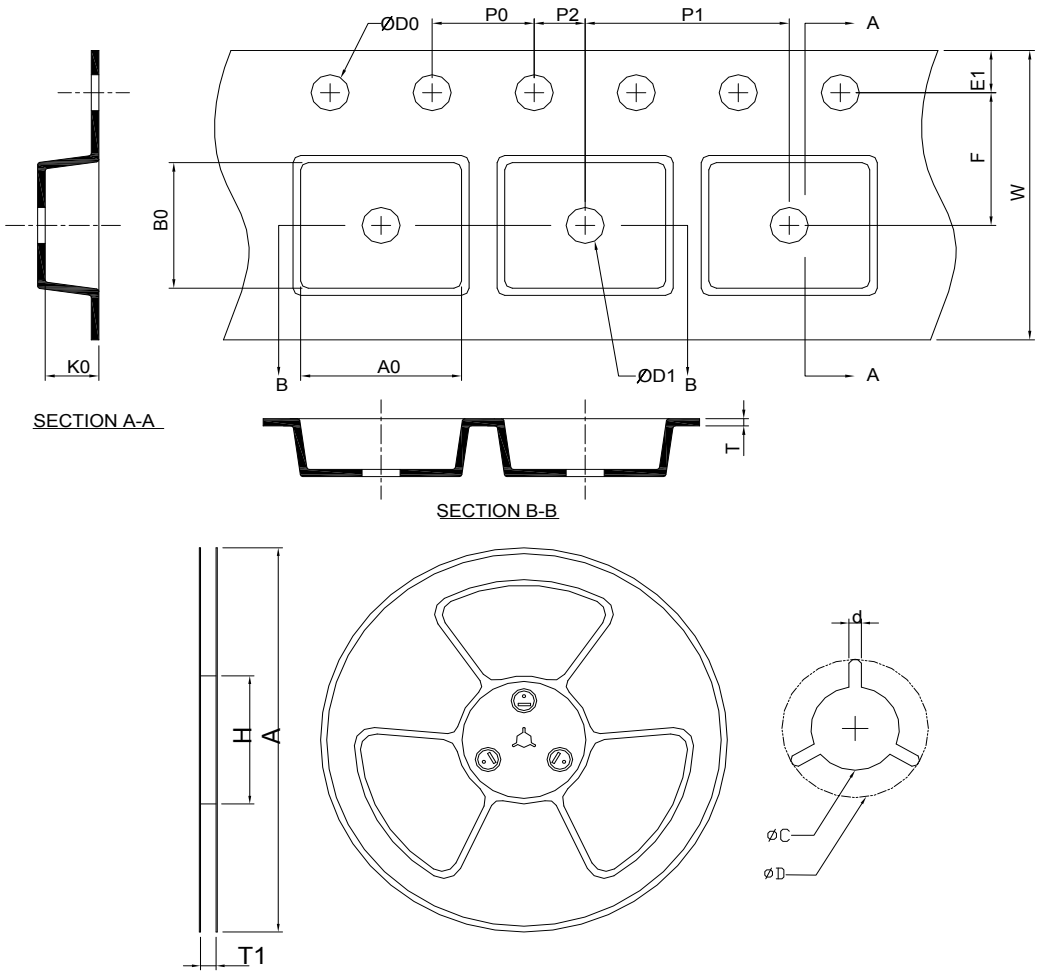
Package Information

VTQFN 2x2-13



SYMBOL	VTQFN2x2-13			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 REF		0.006 REF	
b	0.15	0.25	0.006	0.010
b1	0.10	0.20	0.004	0.008
D	2.00 BSC		0.079 BSC	
E	2.00 BSC		0.079 BSC	
e	0.40 BSC		0.016BSC	
e1	0.40 BSC		0.016BSC	
L	0.30	0.40	0.012	0.016
L1	0.75	0.85	0.030	0.034
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTQFN(2x2)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.20±0.15	2.20±0.15	0.75±0.05

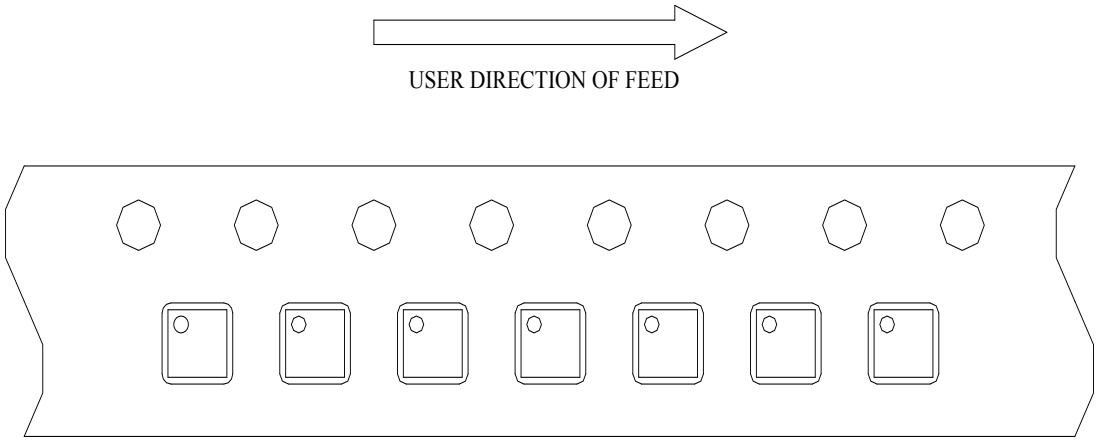
(mm)

Devices Per Unit

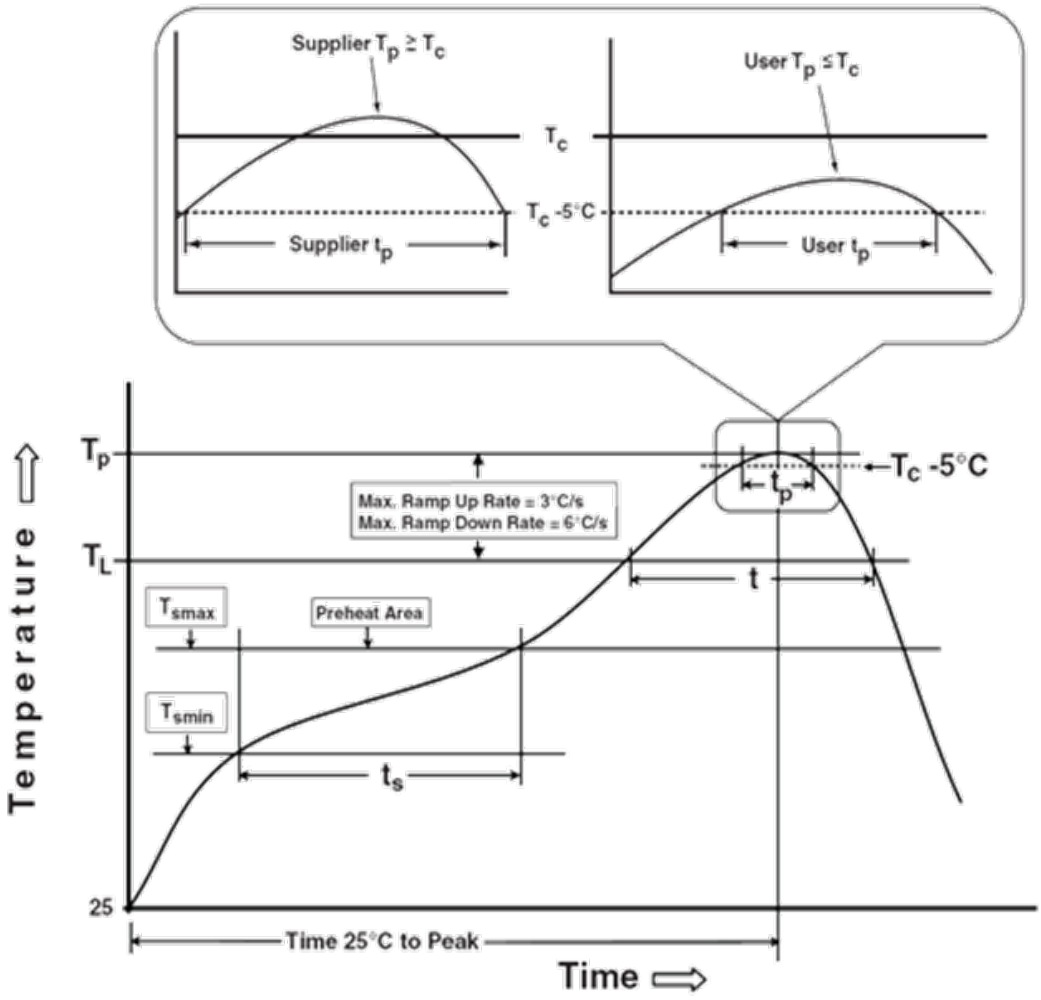
Package type	Packing	Quantity
VTQFN(2x2)	Tape & Reel	3000

Taping Direction Information

VTQFN 2x2-13



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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