

3W Mono Class-D Audio Power Amplifier With Auto-Recovering Short-Circuit Protection

Features

- Operating Voltage: 2.4V-6V
- **Low Supply Current**
 - $-I_{pp}=1.8$ mA at $V_{pp}=5$ V
 - $-I_{DD}$ =1.5mA at V_{DD} =3.6V
- **Low Shutdown Current**
 - $-I_{DD} = 0.1 \text{ mA}$ at $V_{DD} = 5 \text{ V}$
- **Output Power** at 1% THD+N
 - 1.41W, at V_{DD} =5V, R₁=8W
 - 0.74W, at V_{pp} =3.6V, R_1 =8W
 - 2.51W, at V_{DD} =5V, R_L =4W
 - 1.32W, at V_{DD} =3.6V, R_{I} =4W at 10% THD+N
 - 1.8W, at V_{DD} =5V, R_L =8W

 - 0.91W, at V_{DD} =3.6V, R_{L} =8W
 - 3.2W, at V_{DD} =5V, R_L =4W
 - 1.62W, at V_{pp} =3.6V, R_1 =4W
- **Less External Components Required**
- Fast Startup Time (4ms)
- High PSRR: 75 dB at 217 Hz
- **Short-Circuit and Thermal Protection**
- 9-Ball, 1.2mm x 1.2 mm Pitch WLCSP

General Description

The APA2012 is a mono, filter-free Class-D audio amplifier available in a WLCSP package. The gain can be setting by external input resistance. High PSRR and differential architecture provide increased immunity to noise and RF rectification. In addition to these features, a fast startup time and small package size make the APA2012 an ideal choice for both cellular handsets and PDAs. The APA2012 is capable of driving 1.3 W at 5 V or 600 mW

at 3.6 V into 8 Ω . The APA2012 is also capable of driving 4 Ω . The APA2012 is designed with a Class-D architecture and operating with highly efficiency compared with Class-AB amplifier. It's suitable for power sensitive application, such as battery powered devices. The filterfree architecture eliminates the output filter, reduces the external component count, board area, and system costs, and simplifies the design.

The APA2012 provides thermal and over circuit protection.

Simplified Application Circuit

APA2012 OUTN INN VON VOP INP OUTP SHUTDOWN Bias

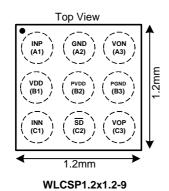
Applications

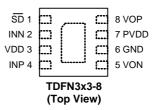
- **Mobile Phones**
- **Handsets**
- **PDAs**
- Portable multimedia devices

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

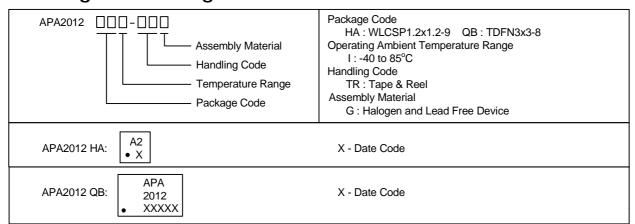


Pin Configuration





Ordering and Marking Information



Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage (VDD, PVDD)	-0.3 to 6.3	V
$V_{IN}, V_{\overline{SD}}$	Input Voltage (SD, INP, INN)	-0.3 to 6.3	V
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C
Ts	Soldering Temperature Range	260	°C
P _D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) WLCSP1.2x1.2-9	165	°C/W
57.	TDFN3x3-8	60	

Note 3 : Please refer to "Layout Recommendation", the ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit	
V _{DD}	Supply Voltage		2.4 ~ 6	
V _{IH}	High Level Threshold Voltage SD		1 ~ 6	V
V _{IL}	Low Level Threshold Voltage	0 ~ 0.35		
T _A	Ambient Temperature Range		-40 ~ 85	°C
TJ	Junction Temperature Range	-40 ~ 125	C	

Electrical Characteristics

 V_{DD} =5V, GND=0V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions			APA2012		Unit
Зупівої	Farameter	lesi Co	Min.	Тур.	Max.	Onne	
I_{DD}	Supply Current	No load		-	1.8	-	mA
I _{IH}	SD High-Level Input Curent	$\overline{SD} = V_{DD}$		-	50	-	μА
I _{IL}	SD High-Level Input Curent	<u>SD</u> = 0V		-	1	-	μА
I _{SD}	VDD shutdown supply current	SD = 0V		-	1	2	μΑ
F_{osc}	Oscillator Frequency			-	300	-	kHz
	Static drain-source	$V_{DD} = 5V$ Static drain-source	P-Channel MOSFET	-	200	-	
R_{DSON}			v _{DD} = 3 v	N-Channel MOSFET	-	200	-
NDSON	on-state resistance	V _{DD} = 3.6V	P-Channel MOSFET	-	220	-	11122
	V _{DD}	N-Channel MOSFET	-	- 220	-		
Vos	Output Offset Voltage	INN and INP connect together, A _V =2V/V		-	1	5	mV
Av	Gain	R_{in} in $k\Omega$		285/R _{in}	300/R _{in}	315/R _{in}	V/V
OTP	Over Temperature Protection			-	170	-	°C
Tstart-up	Start up time			-	4	-	ms



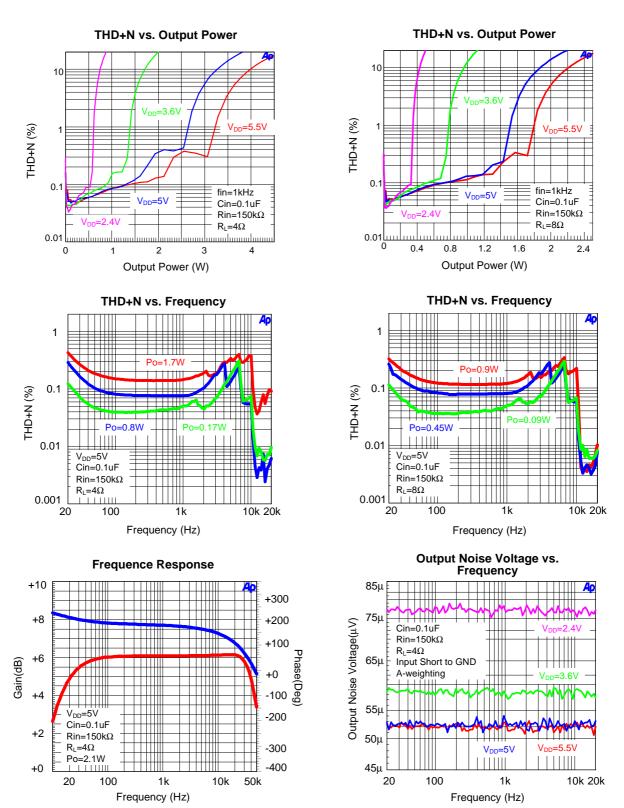
Electrical Characteristics

 V_{DD} =5V, GND=0V, T_A = 25°C (unless otherwise noted)

Symbol Parameter		Test Conditions		APA2012			Unit
Symbol	Parameter	rest conditions		Min.	Тур.	Max.	Unit
V _{DD} =5V, T _A =	:25°C						
		THD+N = 1%,	$R_L = 4\Omega$	-	2.51	-	
Po	Output Power	$f_{in} = 1kHz$	$R_L = 8\Omega$	-	1.41	-	w
F 0	Output Fower	THD+N = 10%,	$R_L = 4\Omega$	-	3.2	-	VV
		$f_{in} = 1kHz$	$R_L = 8\Omega$	1	1.8	-	
THD+N	Total Harmonic Distortion	f _{in} = 1kHz	$R_{L} = 4\Omega$ $P_{O} = 1.7W$	ı	0.1	-	- %
1110111	Pulse Noise	1 n = 11(112	$R_{L} = 8\Omega$ $P_{O} = 0.9W$	-	0.1	-	- %
PSRR	Power Supply Rejection Ratio	Inputs AC floating, V _{PP} =200mV ripple, f = 217Hz		-	75	-	dB
S/N	Signal-to-noise ratio	With A-weighted Fil	-	90	-	dB	
V_n	Noise Output Voltage	Inputs AC grounded 20kHz, A-weighting	I with C_i =2 μ F, f=20Hz to Filter	ı	55	-	μV (rms)
V _{DD} =3.6V, T	_A =25°C						
		THD = 1%	$R_L = 4\Omega$	-	1.32	-	w
Po	Output Power	f = 1KHz	$R_L = 8\Omega$	1	0.74	-	
FU	Output Fower	THD = 10%	$R_L = 4\Omega$	1	1.62	-	
		f = 1KHz	$R_L = 8\Omega$	ı	0.91	-	
THD+N	Total harmonic Distortion	f=1KHz	$R_{L} = 4\Omega$ $P_{O} = 0.84W$	-	0.1	-	%
	Pulse Noise	1-11(1)2	$R_{L} = 8\Omega$ $P_{O} = 0.4W$	1	0.1	-	70
PSRR	Power Supply Rejection Ratio	Inputs AC floating, V _{PP} =200mV ripple, f = 217Hz		-	75	-	dB
S/N	Signal-to-noise ratio	With A-weighted Fil	ter P _O =0.43W, R _L =8Ω	1	90	-	dB
V_n	Noise Output Voltage	Inputs AC grounded 20kHz, A-weighting	I with C_i =2 μ F, f=20Hz to Filter	-	55	-	μV (rms)

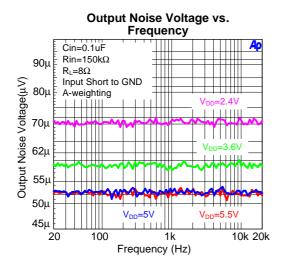


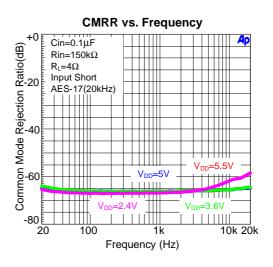
Typical Operating Characteristics

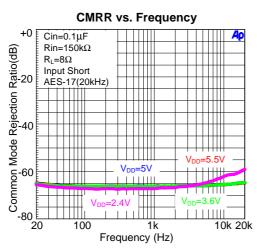


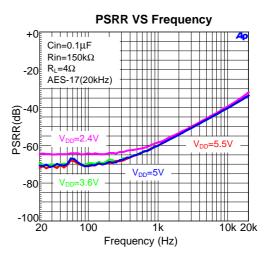


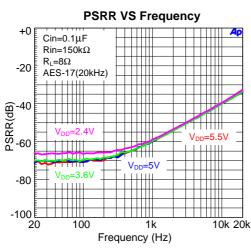
Typical Operating Characteristics (Cont.)

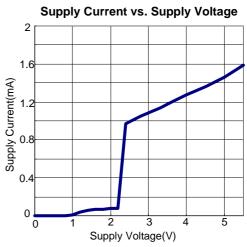






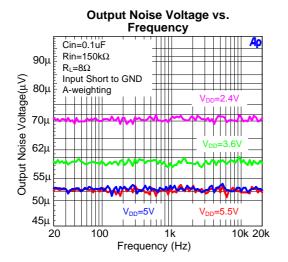


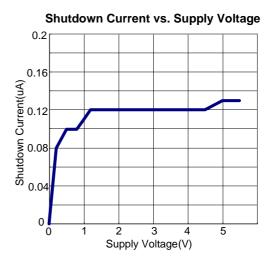






Typical Operating Characteristics (Cont.)



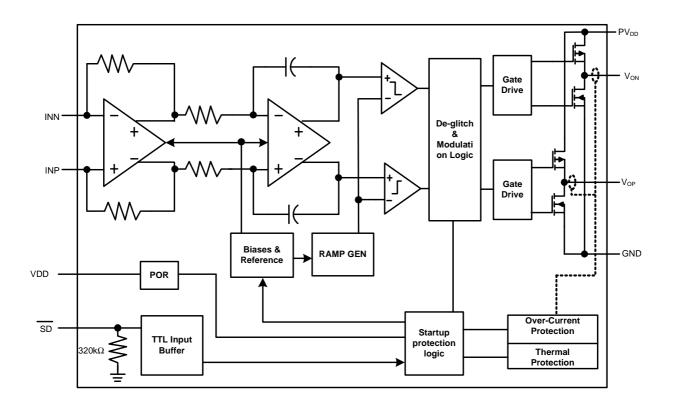




Pin Description

	PIN			
NO.		NAME	1/0	FUNCTION
WLCSP1.2x1.2-9	TDFN3x3-8	NAIVIE		
A1	4	INP	I	The non-inverting input of amplifier. INP is connected to Gnd via a capacitor for single-end (SE) input signal.
A2	6	GND	-	Ground connection for circuitry.
A3	5	VON	0	The negative output terminal of Class-D amplifier.
B1	3	VDD	-	Supply voltage input pin.
B2	7	PVDD	-	Supply voltage only for power stage.
B3	-	PGND	-	Ground connection for power stage
C1	2	INN	I	The inverting input of amplifier. INN is used as audio input terminal, typically.
C2	1	SD	I	Shutdown mode control signal input, place entire IC in shutdown mode when held low.
C3	8	VOP	0	The positive output terminal of Class-D amplifier.

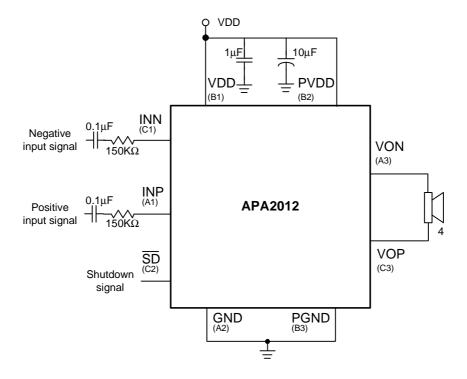
Block Diagram



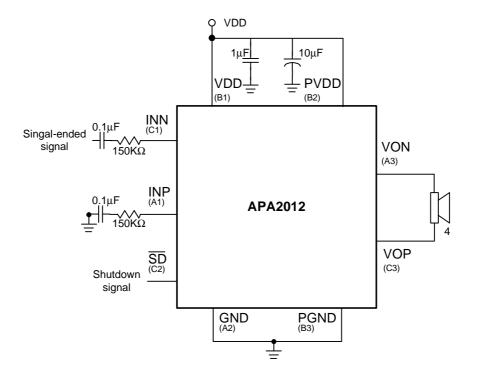


Typical Application Circuit

Differential input mode (WLCSP-9)



Single-ended input mode (WLCSP-9)





Application Information

Fully Differential Amplifier

The APA2012 is a fully differential amplifier with differential inputs and outputs. The fully differential has some advantages versus traditional amplifier. First, there is no need for the input coupling capacitors, because the common-mode feedback will compensate the input bias. The inputs can biased from 0.5V~V_DD^-0.5V, and the outputs still be biased at mid-supply of APA2012. If the inputs are biased out of the input range, the coupling capacitors are required. Second, No need the mid-supply capacitor (C_B), this is because any shift of the mid-supply of APA2012, will have the same affect both positive & negative channel, and will cancel at the differential outputs. Third, The fully differential amplifier will cancel the GSM RF transmitter's signal (217Hz).

Class-D Operation

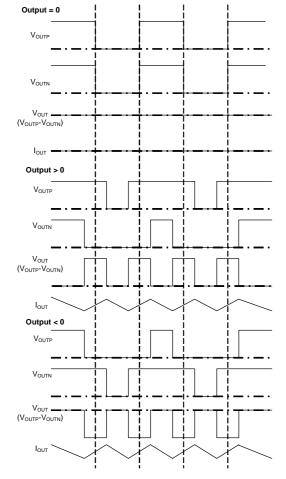


Figure 1. APA2012 Output waveform (Voltage& Current)

The APA2012 modulation scheme is show in figure 1, The outputs V_{OP} and V_{ON} are in phase with each other when no input signals. When output > 0V the duty cycle of VOP is greater than 50% and V_{ON} is less than 50%, and when output <0V, the duty cycle of VOP is less than 50% and V_{ON} is greater than 50%. This method reduces the switching current across the load, and reduces the I^2R losses in the load that improve the amplifier's efficiency. This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminate in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Shutdown Function

In order to reduce power consumption while not in use, the APA2012 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the \overline{SD} pin for APA2012. It is best to switch between ground and the supply voltage VDD to provide maximum device performance. By switching the \overline{SD} pin to low level, the amplifier enters a low-consumption- current state, I $_{DD}$ for APA2012 is in shutdown mode. On normal operating, APA2012's \overline{SD} pin should pull to high level to keeping the IC out of the shutdown mode. The \overline{SD} pin should be tied to a definite voltage to avoid unwanted state changes.

Square Wave Into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jump out the air gap and deface the voice coil. But this depend on the amplitude of square wave is high enough and the bandwidth of speaker is high than the square wave; is frequency. For 250KHz switching frequency, this is not issue for the speaker, because the frequency is beyond the audio band, and can; it significantly move the voice coil, as cone movement is proportional to 1/f² for frequency out of audio band.



Application Information (Cont.)

Over Current Protection

The APA2012 monitors the output current, and when the current exceeds the current-limit threshold, the APA2012 turn-off the output stage to prevent the output device from damages in over-current or short-circuit condition. The IC will turn-on the output buffer after 100ms, but if the over-current or short-circuits condition is still remain, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has be removed.

Thermal Protection

The over-temperature circuit limits the junction temperature of the APA2012. When the junction temperature exceeds $T_J = \pm 170^{\circ} C$, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about $150^{\circ} C$. The thermal protection is designed with a $25^{\circ} C$ hysterics to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Input Resistance, R_{in}

The gain of the APA2012 has been set by the external resistors (R_{in}).

$$Gain(Av) = \frac{2X150k\Omega}{R_{in}}$$
 (1)

For fully differential operating, the $R_{\rm in}$ match is very important for CMRR, PSRR and harmonic distortion performance. It's recommended to use 1% tolerance resistor or better. Keeping the input trace as short as possible to limit the noise injection.

The gain is recommended to set as 2V/V or lower for APA2012 optimal performance.

Input Capacitor, C_{in}

In the typical application, an input capacitor, $C_{\rm in}$, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, $C_{\rm in}$ and the minimum input impedance $R_{\rm in}$ from a high-pass filter with the corner frequency are determined in the following equation:

$$F_{C(highpass)} = \frac{1}{2\pi R_{in} C_{in}}$$
 (2)

The value of C_{in} must be considered carefully because it directly affects the low frequency performance of the circuit. For example, when R_{in} is $100k\Omega$ and the specification calls for a flat bass response are down to 40Hz. The equation is reconfigured as below:

$$C_{in} = \frac{1}{2\pi R_{in} F_c} \tag{3}$$

When input resistance is considered, the C_{in} is $0.2\mu F$. Therefoe, a value in the range of $0.22\mu F$ to $0.1.0\mu F$ would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network $(R_{in} + R_{ir}, C_{in})$ to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' inputs are held at $V_{\rm DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling, C

The APA2012 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically $0.1\mu F$, is placed as close as possible to the device VDD pin for the best operation. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of $10\mu F$ or greater is placed near the audio power amplifier is recommended.



Application Information (Cont.)

Output LC Filter

If the traces from the APA2012 to speaker are short, the APA2012 doesn't require output filter for FCC & CE standard.

A ferrite bead may be needed if it's failing the test for FCC or CE is tested without the LC filter. The Figure 2 is the sample for adding ferrite bead; the ferrite shows when choosing high impedance in high frequency.

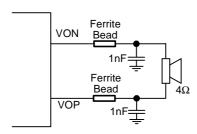


Figure 2. Ferrite bead output filter

Figure 3 is an example for adding the LC filter. It's recommended to eliminate the radiated emission or EMI when the trace from amplifier to speaker is too long.

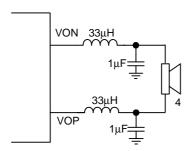


Figure 3. LC output filter

Figure 3's low pass filter cut-off frequency is F_c

$$F_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}}$$
 (4)

Mixing Two Single-Ended Input Signals

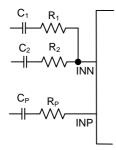


Figure 4. Mixing Two Single-Ended Input Signals

For mixing two Single-Ended (SE) input signals, please refer to Figure 4. The gains of each input can be set difference:

$$A_{V}(1) = \frac{2 \times 150 k\Omega}{R_{A}} \tag{5}$$

$$A_{V}(2) = \frac{2 \times 150 k\Omega}{R_{2}} \tag{6}$$

The corner frequency of each input high- pass-filter also can be set by $R_1\&C_1$, and $R_2\&C_2$.

The non-inverting input's resistor (R_p) and capacitor (C_p) need to match the impedances of invert inputs.

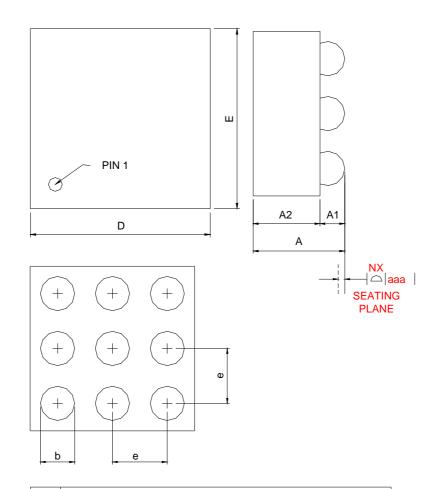
$$C_{P} = C_{1} / / C_{2} = C_{1} + C_{2}$$
 (7)

$$R_{P} = R_{1} / / R_{2} = \frac{R_{1} \times R_{2}}{R_{1} + R_{2}}$$
 (8)



Package Information

WLCSP1.2x1.2-9

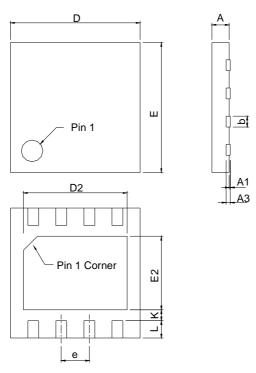


S	WLCSP1.2x1.2-9						
SYMBOL	MILLIM	ETERS	INC	HES			
2	MIN.	MAX.	MIN.	MAX.			
Α		0.63		0.025			
A1	0.12	0.20	0.005	0.008			
A2	0.37	0.43	0.015	0.017			
b	0.20	0.30	0.008	0.012			
D	1.10	1.25	0.043	0.049			
Е	1.10	1.25	0.043	0.049			
е	0.40 BSC		0.010	6 BSC			
aaa	0.05	BSC	0.0	002			



Package Information

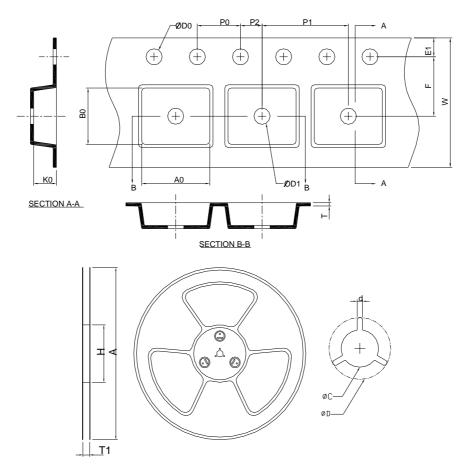
TDFN3x3-8



Ş	TDFN3x3-8					
SYMBOL	MILLIM	MILLIMETERS		HES		
P	MIN.	MAX.	MIN.	MAX.		
Α	0.70	0.80	0.028	0.031		
A1	0.00	0.05	0.000	0.002		
А3	0.20	REF	0.008	8 REF		
b	0.25	0.35	0.010	0.014		
D	2.90	3.10	0.114	0.122		
D2	1.90	2.40	0.075	0.094		
Е	2.90	3.10	0.114	0.122		
E2	1.40	1.75	0.055	0.069		
е	0.65 BSC		0.020	6 BSC		
L	0.30	0.50	0.012	0.020		
K	0.20		0.008			



Carrier Tape & Reel Dimensions



Application	Α	Н	T1	С	d	D	W	E1	F
	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
WLCSP1.2X1.2-9	P0	P1	P2	D0	D1	Т	A0	В0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.30±0.10	1.30±0.10	0.90±0.10
Application	Α	Н	T1	С	d	D	W	E1	F
	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
TDFN3x3-8	P0	P1	P2	D0	D1	Т	A0	В0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

(mm)

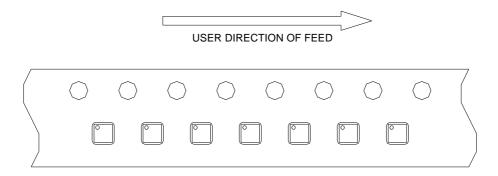
Devices Per Unit

Package Type	Unit	Quantity
WLCSP1.2X1.2-9	Tape & Reel	3000
TDFN3x3-8	Tape & Reel	3000

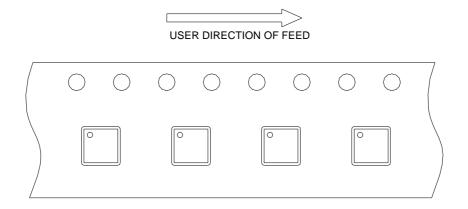


Taping Dircetion Information

WLCSP1.2x1.2-9

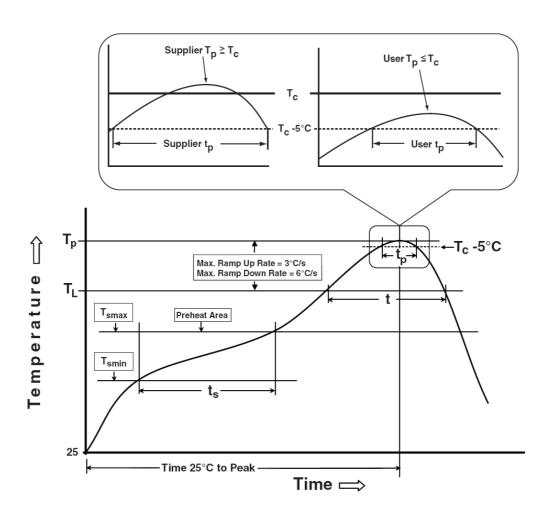


TDFN3x3-8





Classification Profile





Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly		
	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds		
Average ramp-up rate (T _{smax} to T _P)	3 °C/second max.	3°C/second max.		
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds		
Peak package body Temperature $(T_p)^*$	See Classification Temp in table 1	See Classification Temp in table 2		
Time (t _P)** within 5°C of the specified classification temperature (T _c)	20** seconds	30** seconds		
Average ramp-down rate (Tp to Tsmax)	6 °C/second max.	6 °C/second max.		
Time 25°C to peak temperature	6 minutes max.	8 minutes max.		
* Tolerance for peak profile Temperature (Tp) is defined as a supplier minimum and a user maximum.				

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ ³ 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T _i =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
тст	JESD-22, A104	500 Cycles, -65°C~150°C
НВМ	MIL-STD-883-3015.7	VHBM≥2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1 _{tr} ≥100mA

^{**} Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.



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