Stereo 2.6W Audio Power Amplifier (with DC_Volume Control)

Features

- **Low Operating Current with 9mA**
- **Improved Depop Circuitry to Eliminate Turn-on and Turn-off Transients in Outputs**
- **High PSRR**
- **32 Steps Volume Adjustable by DC Voltage with Hysteresis**
- **2.6W per Channel Output Power into 4Ω Load at 5V, BTL Mode**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/$\overline{\text{BTL}}$ Pin**
- **Low Current Consumption in Shutdown Mode (1μA)**
- **Short Circuit Protection**
- **Thermal Shutdown Protection and Over-Current Protection Circuitry**
- **The OUT+ Signal and the IN- Signal are Outphase**
- **Power Enhanced Package (DIP-16 / DIP-16A)**
- **Lead Free and Green Devices Available (RoHS Compliant)**

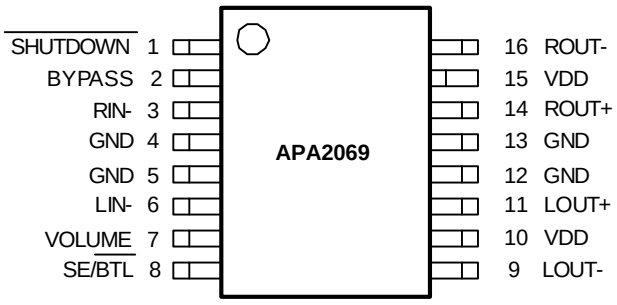
Applications

- **NoteBook PC**
- **LCD Monitor or TV**

General Description

APA2069 is a monolithic integrated circuit, which provides precise DC volume control, and a stereo bridged audio power amplifiers capable of producing 2.6W (2W) into 4Ω with less than 10% (1.0%) THD+N. The attenuator range of the volume control in APA2069 is from 20dB (DC_Vol=0V) to -80dB (DC_Vol=3.54V) with 32 steps. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2069, that reduce pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2069 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal.

Pin Configuration



Ordering and Marking Information

APA2069 □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
J : DIP-16 / DIP-16A
Operating Ambient Temperature Range
I : - 40 to 85 °C
Handling Code
TU : Tube
Assembly Material
L : Lead Free Device
G : Halogen and Lead Free Device

APA2069 J : 

XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage Range	-0.3 to 6	V
V_{IN}	Input Voltage Range, SE/$\overline{BTL}$, $\overline{SHUTDOWN}$	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C
P_D	Power Dissipation	Internal Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air (Note 2) DIP-16 / DIP-16A	45	°C/W
θ_{JC}	Thermal Resistance from Junction to Case in Free Air DIP-16 / DIP-16A	10	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		4.5 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SHUTDOWN}$	2.0 ~	V
		SE/$\overline{BTL}$	4.0 ~	
V_{IL}	Low Level Threshold Voltage	$\overline{SHUTDOWN}$	~ 1.0	V
		SE/$\overline{BTL}$	~ 3.0	
V_{ICM}	Common Mode Input Voltage		~ V_{DD}-0.5	V

Electrical Characteristics

V_{DD}=5V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2069			Unit
			Min.	Typ.	Max.	
I_{DD}	Supply Current	SE/$\overline{BTL}$=0V	-	9	20	mA
		SE/$\overline{BTL}$=5V	-	4	10	
I_{SD}	Supply Current in Shutdown Mode	SE/$\overline{BTL}$=0V $\overline{SHUTDOWN}$=0V	-	1	-	μA
I_{IH}	High Input Current		-	900	-	nA
I_{IL}	Low Input Current		-	900	-	nA
V_{OS}	Output Offset Voltage		-	5	-	mV

Operating Characteristics, BTL mode. V_{DD}=5V, T_A=25°C, R_L=4Ω, A_V=6dB (unless otherwise noted)

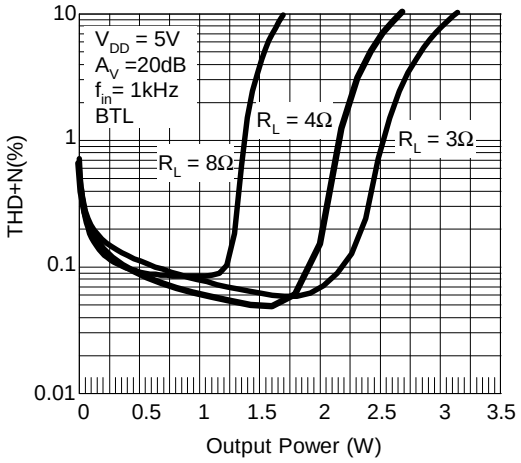
Symbol	Parameter	Test Conditions	APA2069			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N=10%, R_L=3Ω, f_{in}=1kHz	-	2.9	-	W
		THD+N =10%, R_L=4Ω, f_{in}=1kHz	-	2.6	-	
		THD+N =10%, R_L=8Ω, f_{in}=1kHz	-	1.6	-	
		THD+N =1%, R_L=3Ω, f_{in}=1kHz	-	2.4	-	
		THD+N =1%, R_L=4Ω, f_{in}=1kHz	-	2	-	
		THD+N =0.5%, R_L=8Ω, f_{in}=1kHz	1	1.3	-	
THD+N	Total Harmonic Distortion Plus Noise	P_O=1.2W, R_L=4Ω, f_{in}=1kHz	-	0.07	-	%
		P_O=0.9W, R_L=8Ω, f_{in}=1kHz	-	0.08	-	
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.1Vrms, R_L=8Ω, C_B=1μF, f_{in}=120Hz	-	60	-	dB
Crosstalk	Channel Separation	C_B=1μF, R_L=8Ω, f_{in}=1kHz	-	90	-	dB
S/N	Signal to Noise Ratio	P_O=1.1W, R_L=8Ω, A_weighting	-	95	-	dB

Operating Characteristics, SE mode. V_{DD}=5V, T_A=25°C, A_V=0dB (unless otherwise noted)

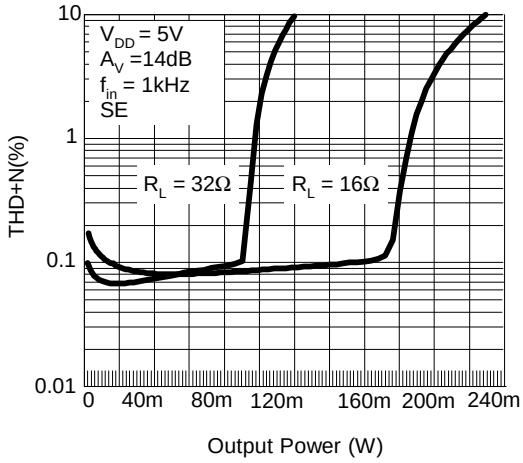
Symbol	Parameter	Test Conditions	APA2069			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N=10%, R_L=16Ω, f_{in}=1kHz	-	220	-	mW
		THD+N =10%, R_L=32Ω, f_{in}=1kHz	-	120	-	
		THD+N =1%, R_L=16Ω, f_{in}=1kHz	-	160	-	
		THD+N =1%, R_L=32Ω, f_{in}=1kHz	-	95	-	
THD+N	Total Harmonic Distortion Plus Noise	P_O=125mW, R_L=16Ω, f_{in}=1kHz	-	0.09	-	%
		P_O=65mW, R_L=32Ω, f_{in}=1kHz	-	0.09	-	
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.1Vrms, R_L=32Ω, C_B=1μF, f_{in}=120Hz	-	60	-	dB
Crosstalk	Channel Separation	C_B=1μF, R_L=32Ω, f_{in}=1kHz	-	60	-	dB
S/N	Signal to Noise Ratio	P_O=75mW, SE, R_L=32Ω, A_weighting	-	100	-	dB

Typical Operating Characteristics

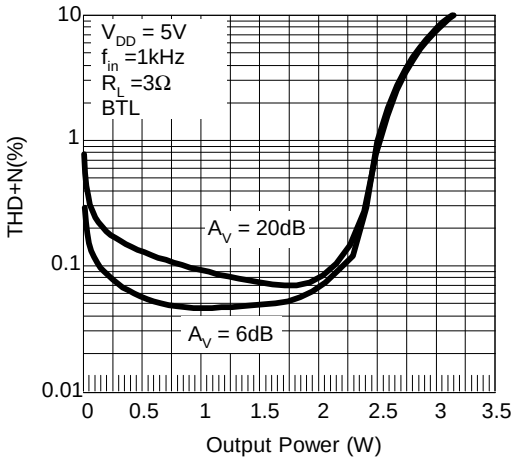
THD+N vs. Output Power



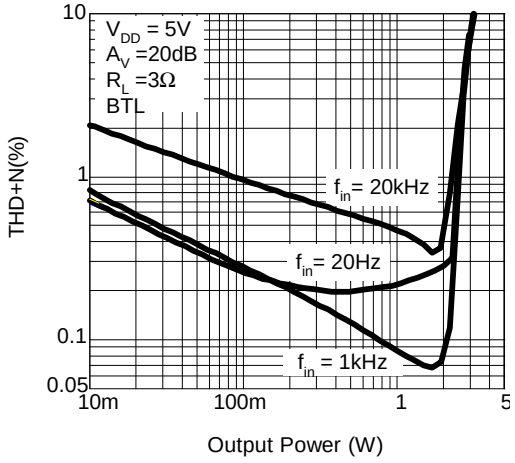
THD+N vs. Output Power



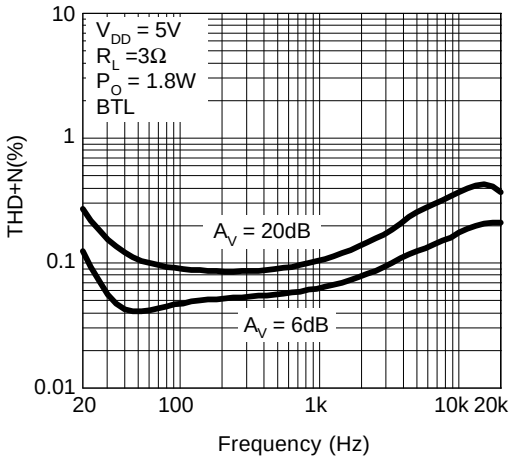
THD+N vs. Output Power



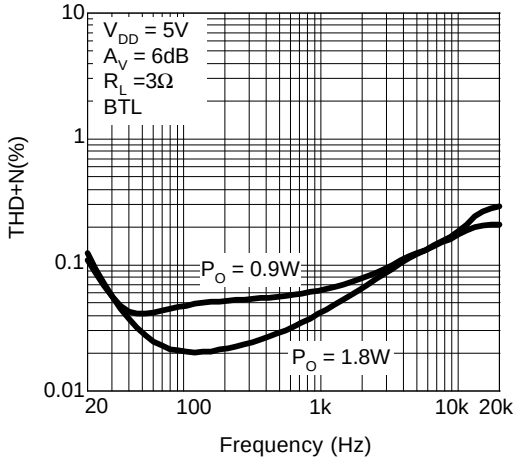
Output Noise Voltage vs. Frequency



THD+N vs. Frequency

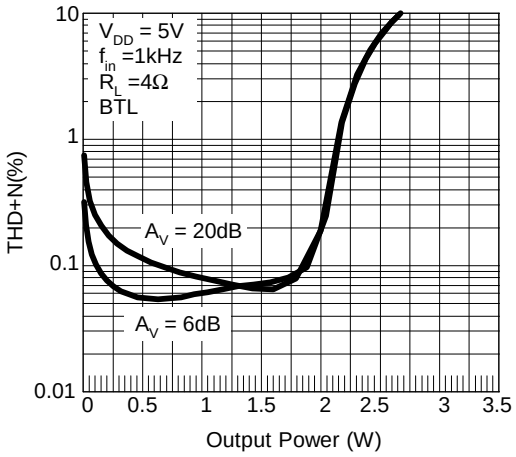


THD+N vs. Frequency

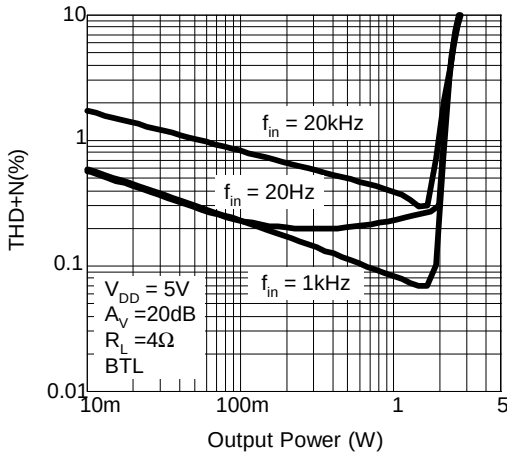


Typical Operating Characteristics (Cont.)

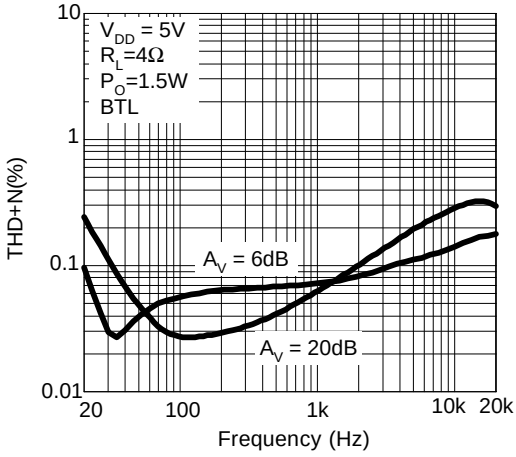
THD+N vs. Output Power



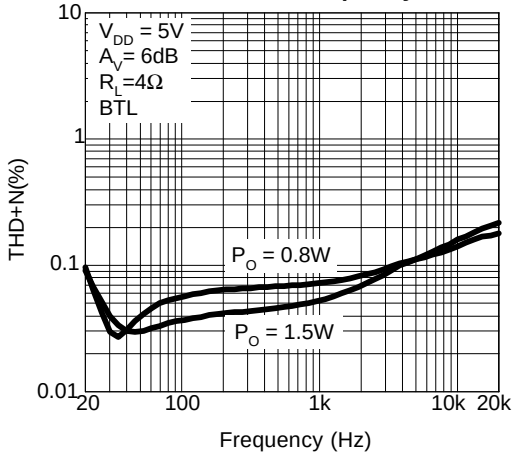
THD+N vs. Output Power



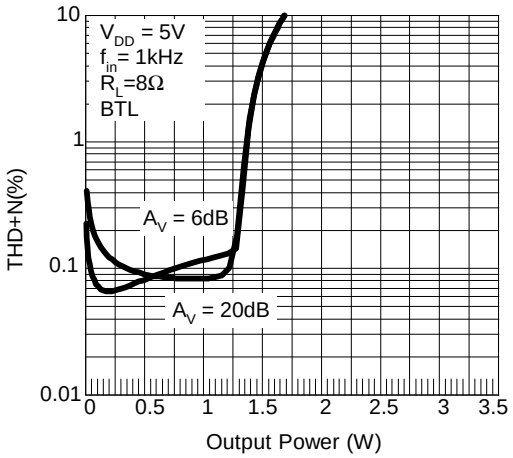
THD+N vs. Frequency



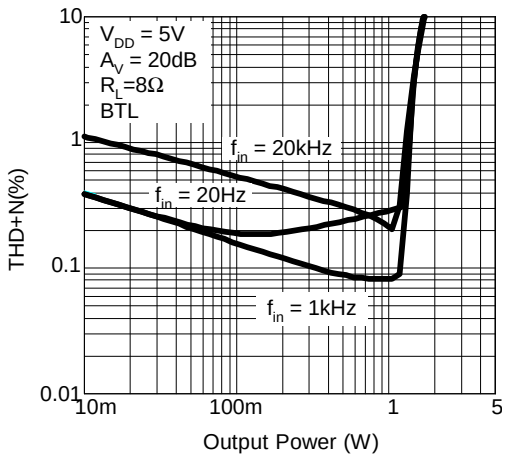
THD+N vs. Frequency



THD+N vs. Output Power

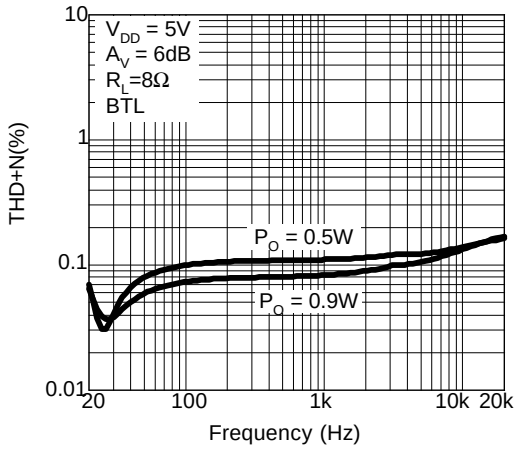


THD+N vs. Output Power

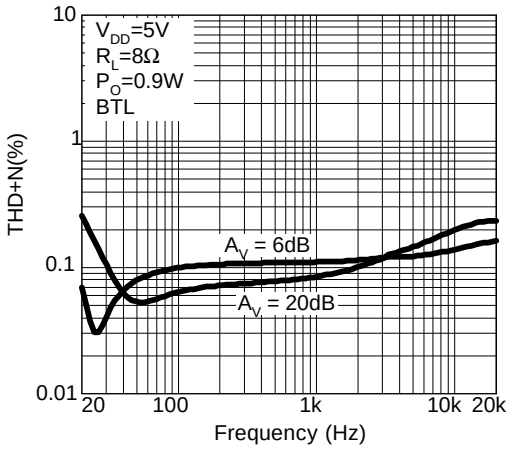


Typical Operating Characteristics (Cont.)

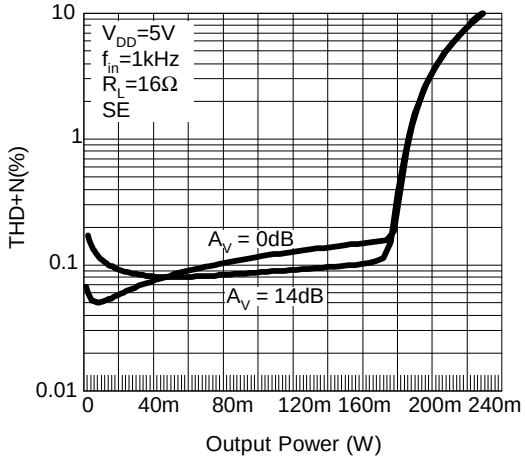
THD+N vs. Frequency



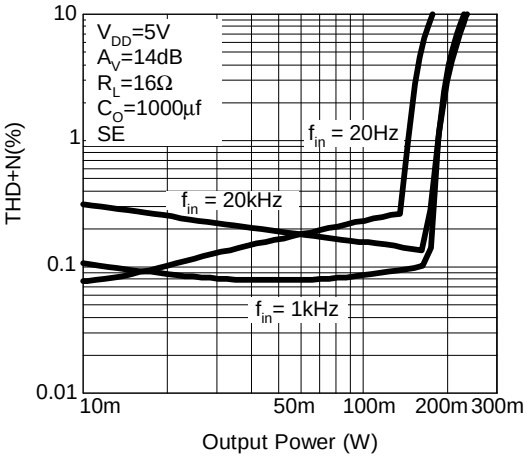
THD+N vs. Frequency



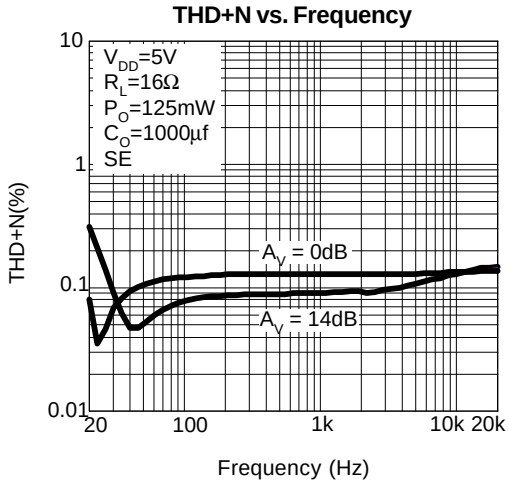
THD+N vs. Output Power



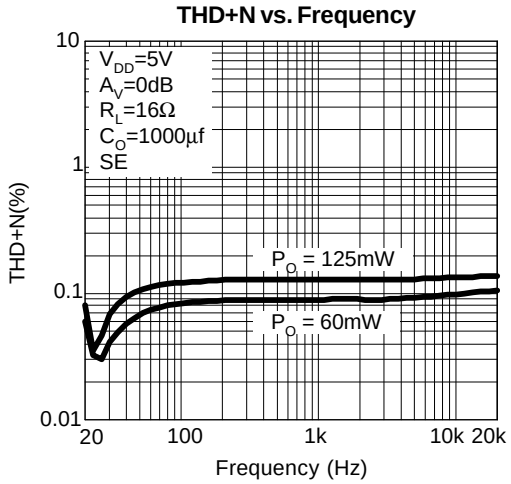
THD+N vs. Output Power



THD+N vs. Frequency

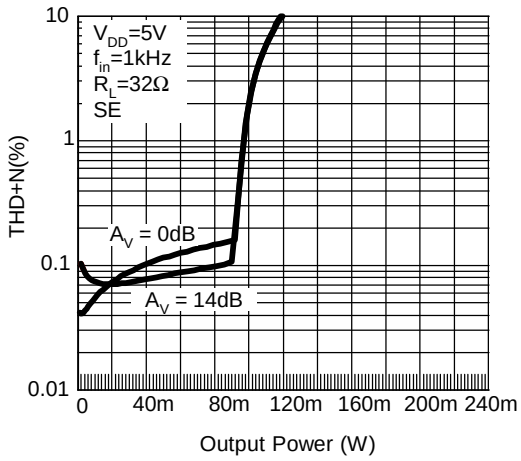


THD+N vs. Frequency

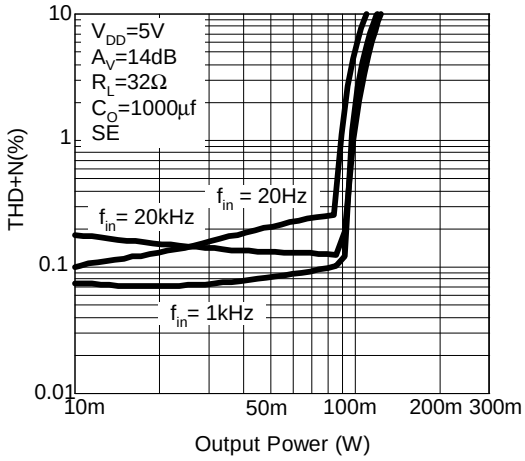


Typical Operating Characteristics (Cont.)

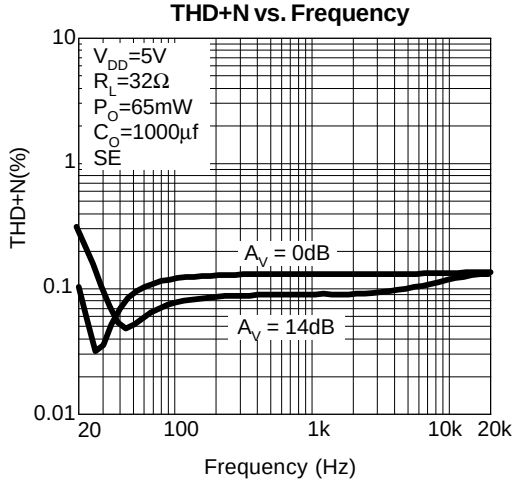
THD+N vs. Output Power



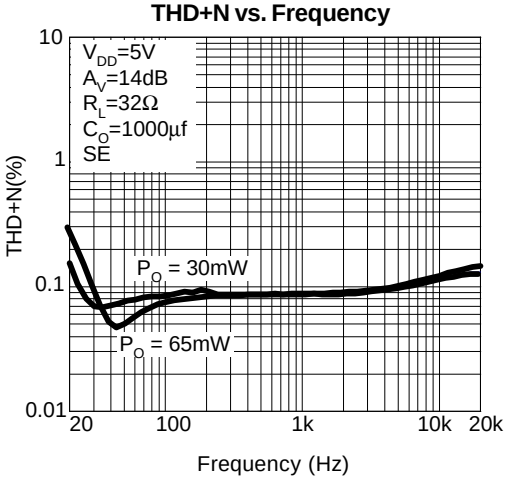
THD+N vs. Output Power



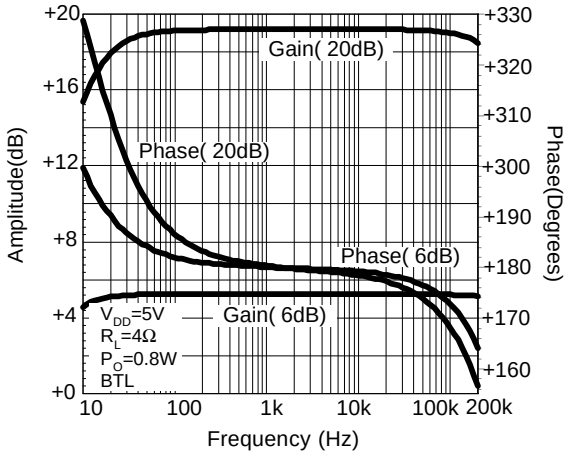
THD+N vs. Frequency



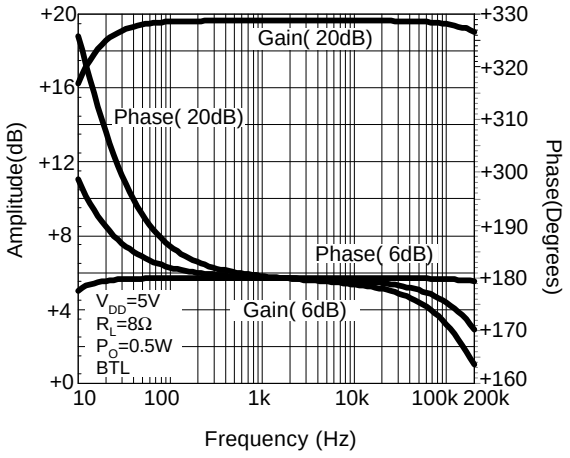
THD+N vs. Frequency



Frequency Response

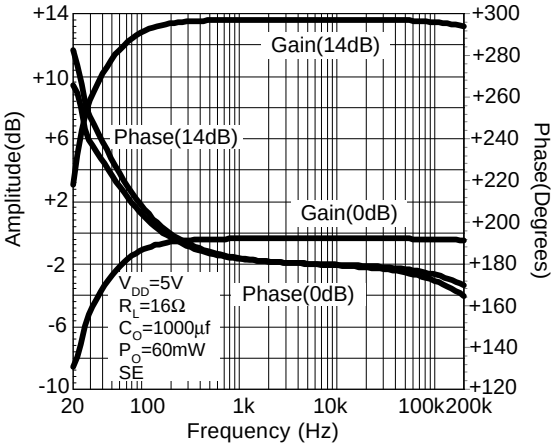


Frequency Response

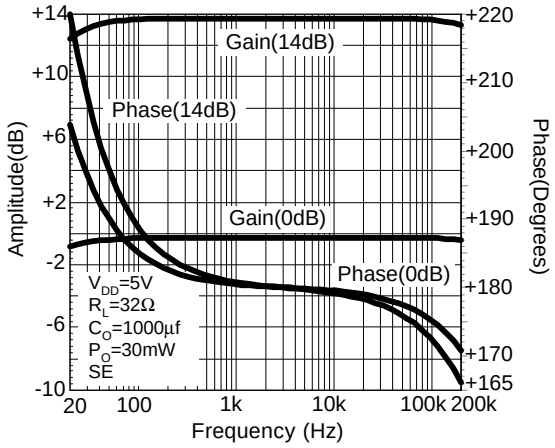


Typical Operating Characteristics (Cont.)

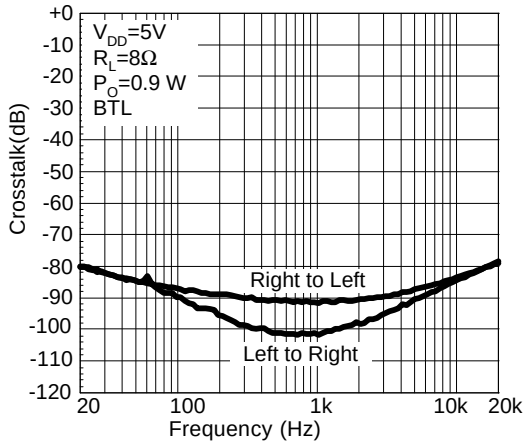
Frequency Response



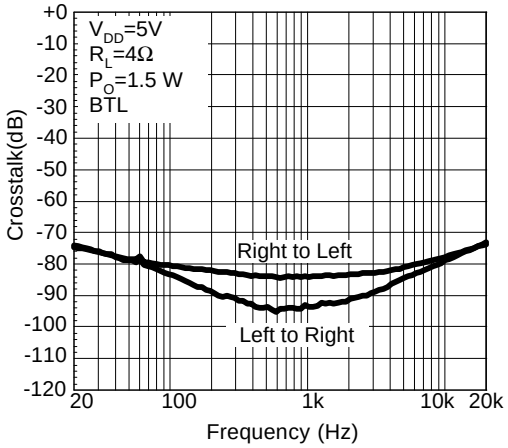
Frequency Response



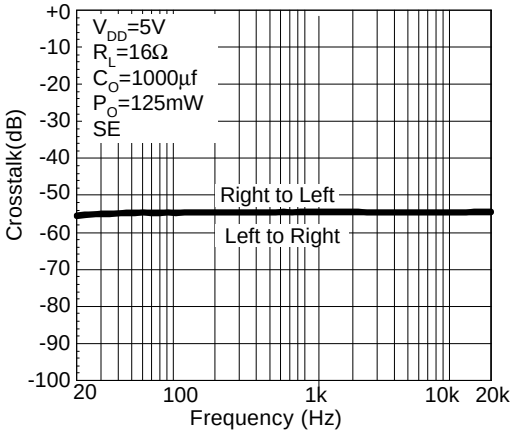
Crosstalk vs. Frequency



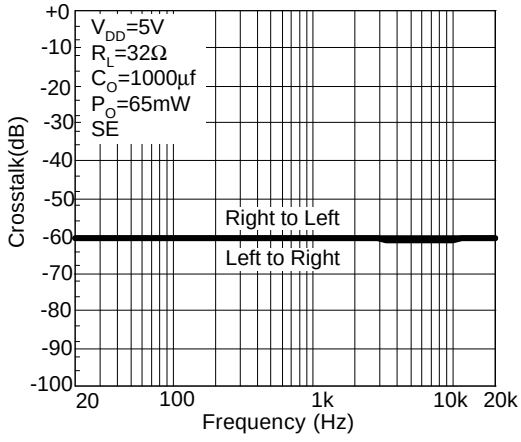
Crosstalk vs. Frequency



Crosstalk vs. Frequency

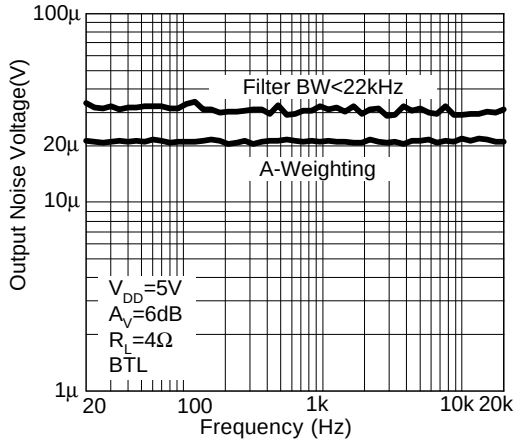


Crosstalk vs. Frequency

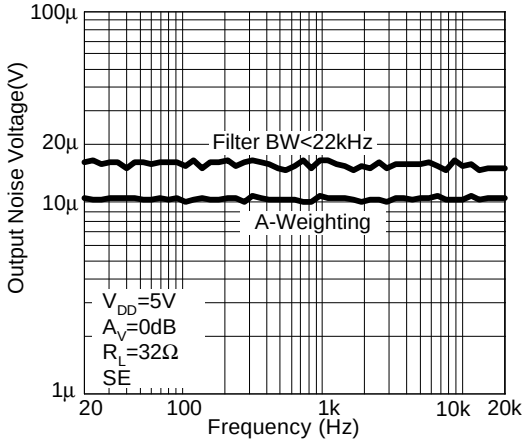


Typical Operating Characteristics (Cont.)

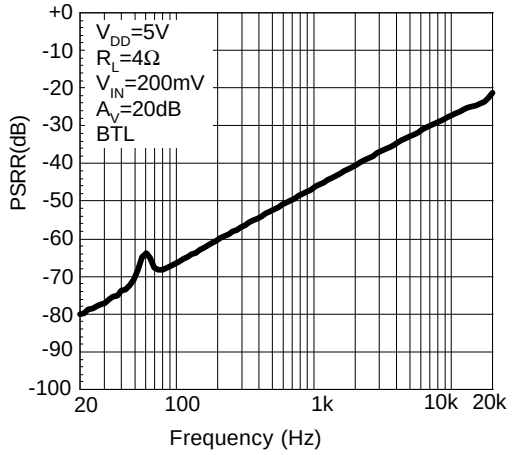
Output Noise Voltage vs. Frequency



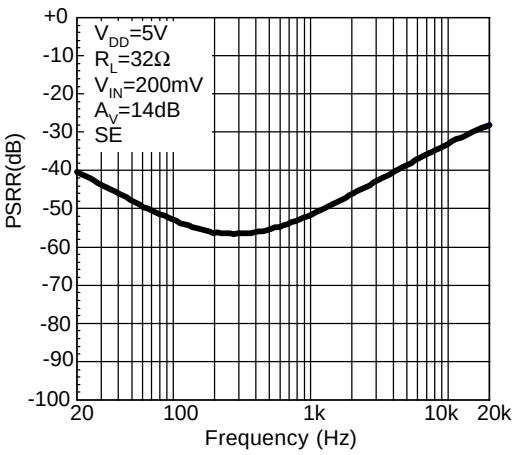
Output Noise Voltage vs. Frequency



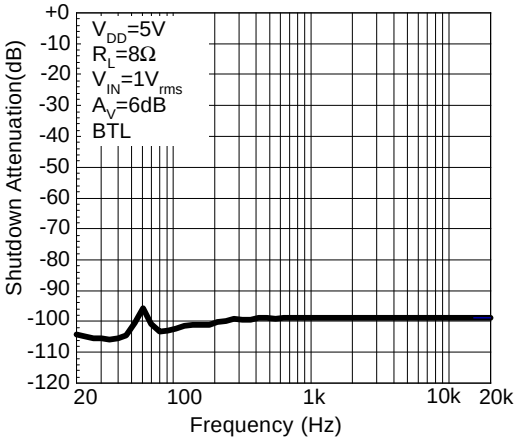
PSRR vs. Frequency



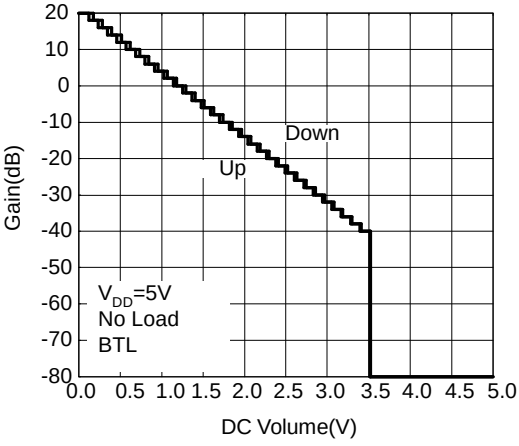
PSRR vs. Frequency



Shutdown Attenuation vs. Frequency

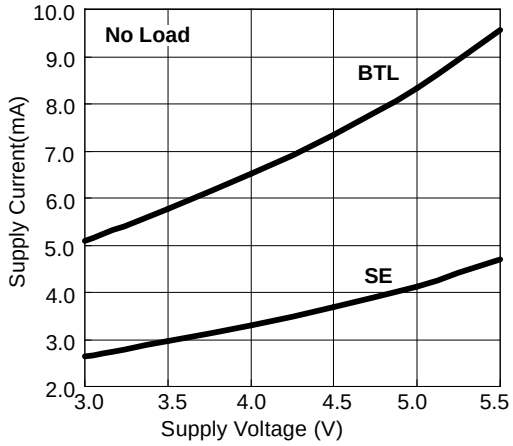


Gain vs. Volume Voltage

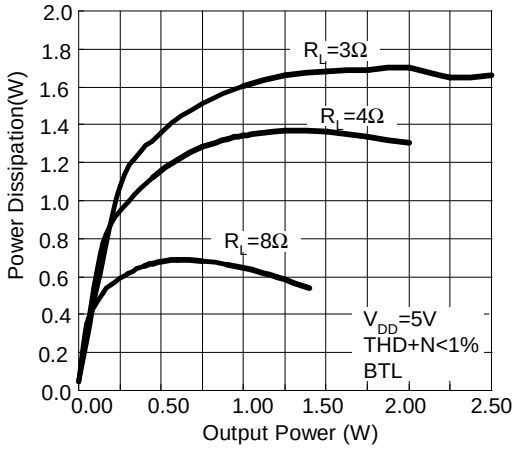


Typical Operating Characteristics (Cont.)

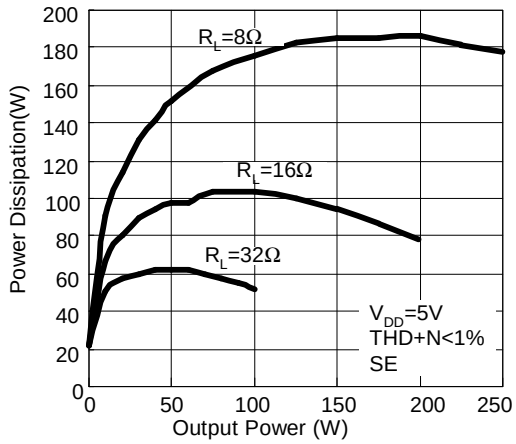
Supply Current vs. Supply Voltage



Power Dissipation vs. Output Power



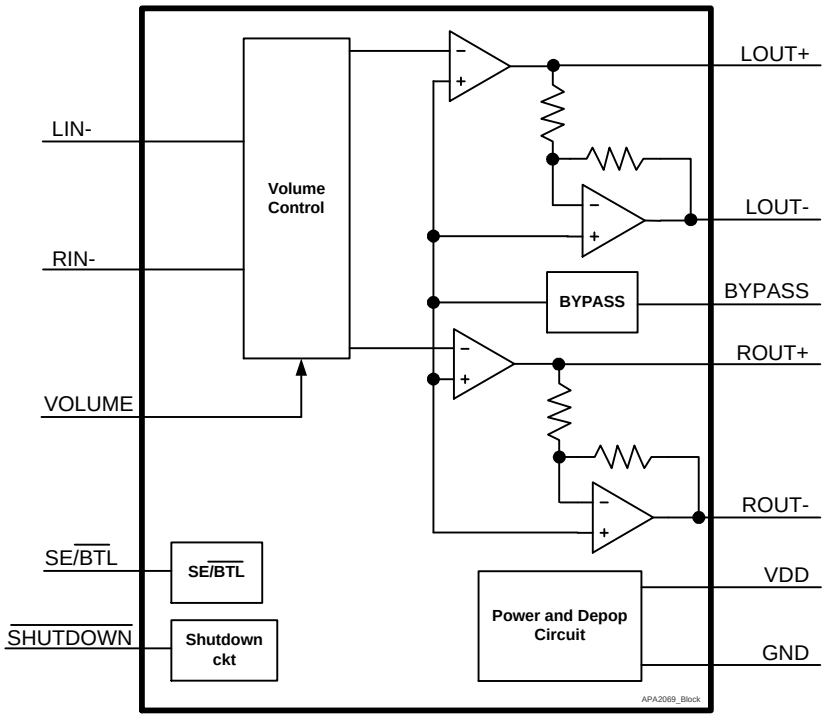
Power Dissipation vs. Output Power



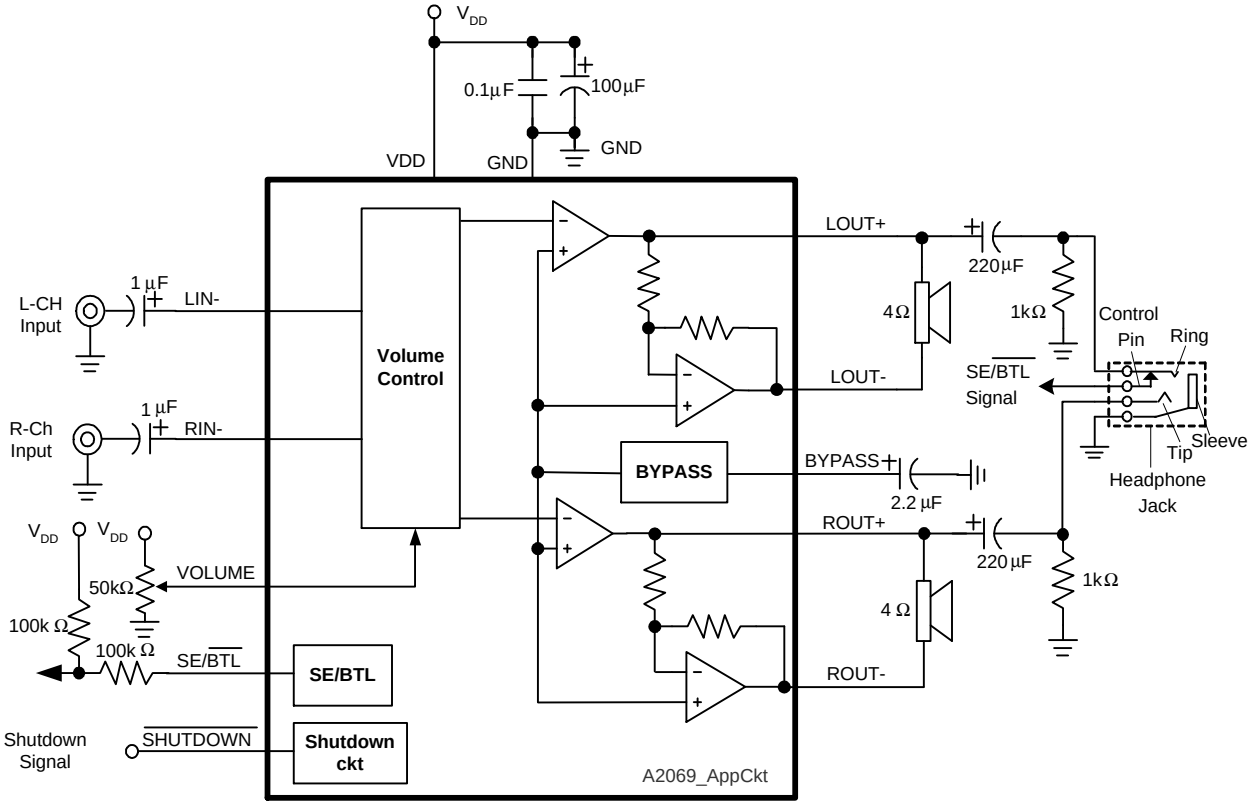
Pin Description

PIN		CONFIG	FUNCTION
NO.	NAME		
1	$\overline{\text{SHUTDOWN}}$	I	It will be into shutdown mode when pull low. I_{SD} = 1μA
2	BYPASS	I	Bias voltage generator
3	RIN-	I	Right channel input terminal
4,5,12,13	GND	-	Ground connection, Connected to thermal pad.
6	LIN-	I	Left channel input terminal
7	VOLUME	I	Input signal for internal volume gain setting.
8	SE/$\overline{\text{BTL}}$	I	Output mode control input, high for SE output mode and low for BTL mode.
9	LOUT-	O	Left channel negative output in BTL mode and high impedance in SE mode.
10,15	VDD	-	Supply voltage
11	LOUT+	O	Left channel positive output in BTL mode and SE mode.
14	ROUT+	O	Right channel positive output in BTL mode and SE mode.
16	ROUT-	O	Right channel negative output in BTL mode and high impedance in SE mode.

Block Diagram



Typical Application Circuit



Volume Control Table_BTL Mode

Supply Voltage V_{DD}=5V

Av(dB)	High(V)	Low(V)	Hysteresis(mV)	Recommended Voltage(V)
20	0.12	0.00		0
18	0.23	0.17	52	0.20
16	0.34	0.28	51	0.31
14	0.46	0.39	50	0.43
12	0.57	0.51	49	0.54
10	0.69	0.62	47	0.65
8	0.80	0.73	46	0.77
6	0.91	0.84	45	0.88
4	1.03	0.96	44	0.99
2	1.14	1.07	43	1.10
0	1.25	1.18	41	1.22
-2	1.37	1.29	40	1.33
-4	1.48	1.41	39	1.44
-6	1.59	1.52	38	1.56
-8	1.71	1.63	37	1.67

Volume Control Table_BTL Mode (Cont.)

Supply Voltage V_{DD}=5V

Av(dB)	High(V)	Low(V)	Hysteresis(mV)	Recommended Voltage(V)
-10	1.82	1.74	35	1.78
-12	1.93	1.85	34	1.89
-14	2.05	1.97	33	2.01
-16	2.16	2.08	32	2.12
-18	2.28	2.19	30	2.23
-20	2.39	2.30	29	2.35
-22	2.50	2.42	28	2.46
-24	2.62	2.53	27	2.57
-26	2.73	2.64	26	2.69
-28	2.84	2.75	24	2.80
-30	2.96	2.87	23	2.91
-32	3.07	2.98	22	3.02
-34	3.18	3.09	21	3.14
-36	3.30	3.20	20	3.25
-38	3.41	3.32	18	3.36
-40	3.52	3.43	17	3.48
-80	5.00	3.54	16	5

Application Information

BTL Operation

The APA2069 output stage (power amplifier) has two pairs of operational amplifiers internally, which allows different amplifier configurations.

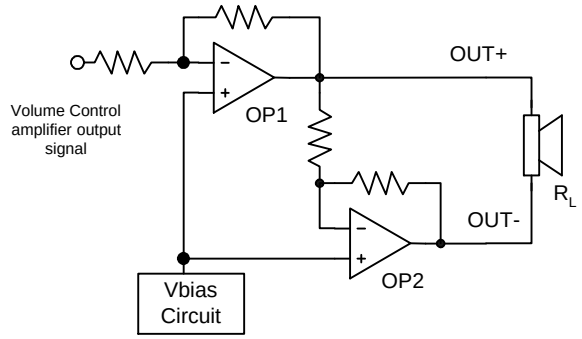


Figure 1: APA2069 Internal Configuration

(each channel)

The power amplifier's OP1 gain is set by internal unity-gain and input audio signal comes from internal volume control amplifier. While the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration is commonly referred to the bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus, doubles the output swing for aspecified supply voltage.

When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA2069, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, it's not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation

To consider the single-supply SE configuration shown in the Application Circuit, a coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).The rules described still hold with the addition of the following relationship:

$$\frac{1}{C_B \times 150k\Omega} \leq \frac{1}{R_i C_i} << \frac{1}{R_L C_C} \qquad (1)$$

Output SE/$\overline{\text{BTL}}$ Operation

The best cost saving feature of APA2069 is that it can be switched easily between BTL and SE modes. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA2069, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

· When SE/$\overline{\text{BTL}}$ keeps low, the OP2 turns on and the APA2069 is in the BTL mode.

· When SE/$\overline{\text{BTL}}$ keeps high, the OP2 is in a high output impedance state, which configures the APA2069 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in the SE mode.

The Control of the SE/$\overline{\text{BTL}}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in the Application Circuit.

Application Information (Cont.)

Output SE/$\overline{BTL}$ Operation (Cont.)

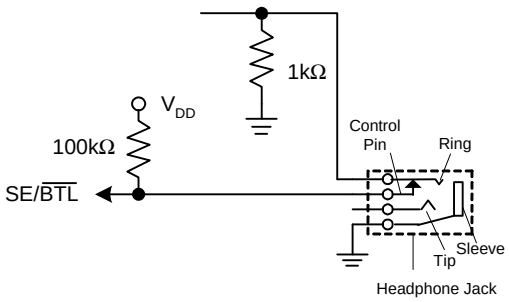


Figure 2: SE/$\overline{BTL}$ Input Selection by Readphone Plug

In Figure 2, input SE/$\overline{BTL}$ operates as below :
When the Readphone plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high and enables the SE mode. When the input goes high, the OUT- amplifier is shutdown which causes the speaker to mute. The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack. When there is no headphone plugged into the system, the contact pin of the headphone jack is connnected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{BTL}$ pin, enabling the BTL function.

Volume Control Function

The APA2069 has an internal stereo volume control whose setting is the function of the DC voltage applied to the VOLUME input pin. The APA2069 volume control consists of 32 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps, controlled by the DC voltage, are from 20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in the table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the volume control graph.

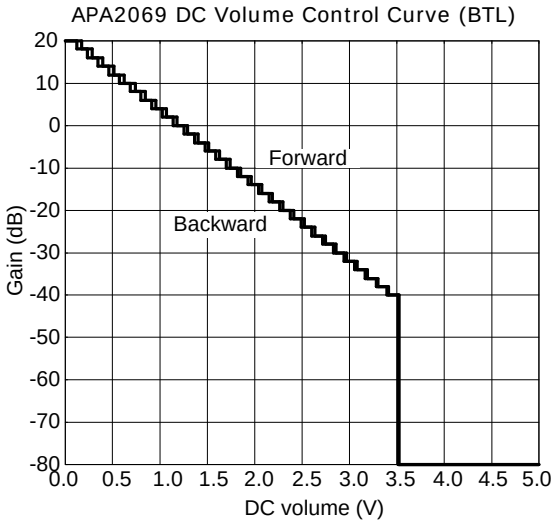


Figure 3: Gain Setting vs. DC Volume Pin Voltage

For the highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gain levels are 2dB/step from 20dB to -40dB in the BTL mode, and the last step at -80dB as mute mode.

Input Resistance, R_i

The gain for each audio input of the APA2069 is set by the internal resistors (R_i and R_F) of volume control amplifier in inverting configuration.

$$\text{SE Gain} = A_V = -\frac{R_F}{R_i} \qquad (2)$$

$$\text{BTL Gain} = -2 \times \frac{R_F}{R_i} \qquad (3)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. For varying gain settings, the APA2069 generates each input resistance on the figure 4. The input resistance will affect the low frequency performance of audio signal. The minmum input resistance is 25kΩ when gain setting is 20dB and the resistance will ramp up when close loop gain below 20dB. The input resistance has wide variation (+/-10%) caused by process variation.

Application Information (Cont.)

Input Resistance, R_i (Cont.)

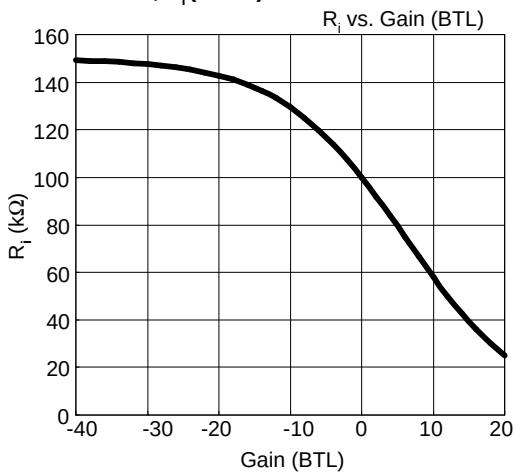


Figure 4: Input resistance vs. Gain setting

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i (25kΩ) form a high-pass filter with the corner frequency determined in the following equation :

$$F_C(highpass) = \frac{1}{2\pi \times 25k\Omega \times C_i} \quad (4)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_i is 25kΩ and the specification calls for a flat bass response down to 50Hz. Equation is reconfigured as below :

$$C_i = \frac{1}{2\pi \times 25k\Omega \times F_C} \quad (5)$$

When the input resistance variation is considered, the value of C_i is 0.13μF, a value in the range 0.22μF to 1.0μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_F, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at V_{DD}/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

A power amplifier, proper supply bypassing, is critical for low noise performance and high power supply rejection. The capacitor location on the BYPASS pin should be as close to the device as possible. The effect of a larger supply bypass capacitor is to improve PSRR due to increased half-supply stability. Two critical criteria of bypass capacitor (C_B): 1st, it depends upon desired PSRR requirements and click-and-pop performance; 2nd, the leakage current of C_B will induce the voltage drop of V_{BYPASS} (voltage of BYPASS pin), and if the V_{BYPASS} is less than 0.49V_{DD}, APA2069 will enter mute condition. The value of V_{BYPASS} can be calculated as below:

$$V_{BYPASS} = 0.5V_{DD} - I_{Leakage} \times 150k\Omega \quad (6)$$

Where

$I_{Leakage}$ =Leakage current of C_B

Therefore, it is recommended that C_B leakage current should be no more then 0.4μA for properly work of APA2069.

To avoid the start-up pop noise, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{(C_B \times 150k\Omega)} << \frac{1}{C_i \times 150k\Omega} \quad (7)$$

The capacitor is fed from a 150kΩ resistor inside of the amplifier and the 150kΩ is the maximum input resistance of (R_i+R_F). Bypass capacitor, C_B, values of 2.2μF to 10μF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance.

The bypass capacitance also affects the start up time. It is determined in the following equation:

$$T_{start\ up} = 5X(C_B \times 150k\Omega) \quad (8)$$

Application Information (Cont.)

Output Coupling Capacitor, C_O

In the typical single-supply SE configuration, an output coupling capacitor (C_O) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation:

$$F_C(\text{highpass}) = \frac{1}{2\pi R_L C_O} \quad (9)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantage, from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_O are required to pass low frequencies into the load.

Power Supply Decoupling, C_S

The APA2069 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device V_{DD} lead works the best. For filtering lower-frequency noise signals, it is recommended to place a large aluminum electrolytic capacitor of 10µF or greater near the audio power amplifier

Optimizing Depop Circuitry

Circuitry has been included in the APA2069 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the clicks and pops.

The value of C_i will also affect turn-on pops (Refer to Effective Bypass Capacitance). The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time. In a SE configuration, the output coupling capacitor, C_O, is of particular concern.

This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_O, the time constant can be relatively large. To reduce transients in the SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current. In most cases, choosing a small value of C_i in the range of 0.33µF to 1µF, C_B being equal to 4.7µF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain, therefore, it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the APA2069 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the $\overline{\text{SHUTDOWN}}$ pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between the ground and the supply V_{DD} to provide maximum device performance.

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, I_{DD}<1µA. APA2069 is in the shutdown mode. Under normal operation, $\overline{\text{SHUTDOWN}}$ pin pull to high level to keep the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changing.

Application Information (Cont.)

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (10)$$

Where

$$P_O = \frac{V_{orms} \times V_{orms}}{R_L} = \frac{(V_P \times V_P)}{2R_L}$$

$$V_{orms} = \frac{V_P}{\sqrt{2}} \quad (11)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (12)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \frac{(\frac{V_P \times V_P}{2R_L})}{(V_{DD} \times \frac{2V_P}{\pi R_L})} = \frac{\pi V_P}{4V_{DD}} \quad (13)$$

Table 1 calculates efficiencies for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than the dissipation in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

P_O (W)	Efficiency (%)	I_{DD} (A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD+N to increase.

Table 1. Efficiency vs. Output Power in 5-V/8Ω BTL Systems

Power Dissipation

Whether the power amplifier is operated in BTL or SE mode, power dissipation is the major concern. Equation14 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode} : P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (14)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode} : P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (15)$$

Since the APA2069 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depend on the mode of operation. Even with this substantial increase in power dissipation, the APA2069 does not require extra heatsink. The power dissipation from equation14, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation16:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (16)$$

For DIP16-A package with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Application Information (Cont.)

Power Dissipation (Cont.)

Since the maximum junction temperature ($T_{J,MAX}$) of APA2069 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation16.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs are per channel values, therefore, the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMAX}), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2069 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs.

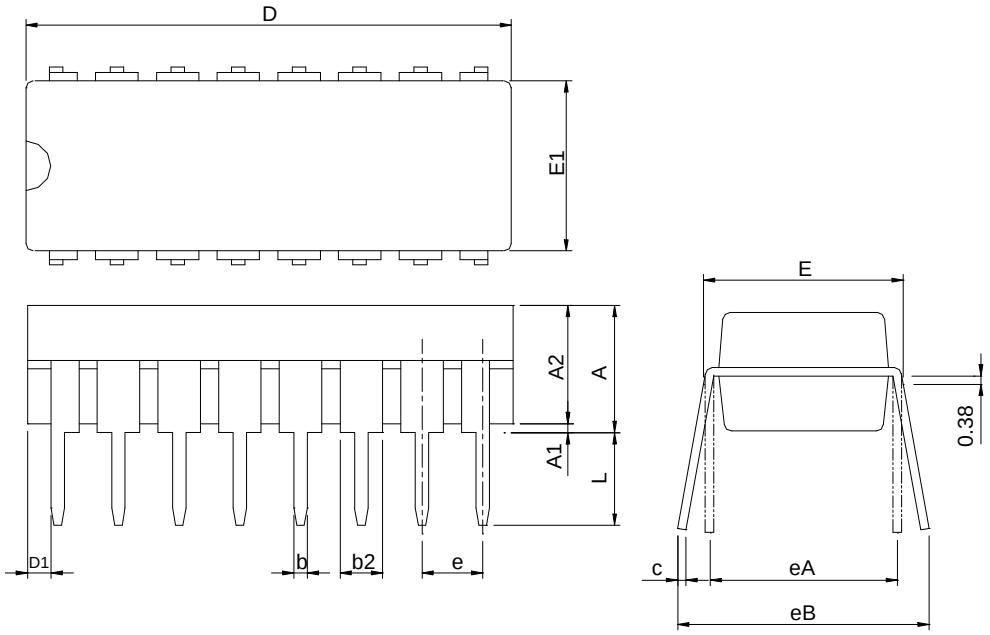
$$T_{AMax} = T_{JMax} - \theta_{JA} P_D \quad (16)$$

150 - 45(0.8*2) = 78°C

The APA2069 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Package Information

DIP-16

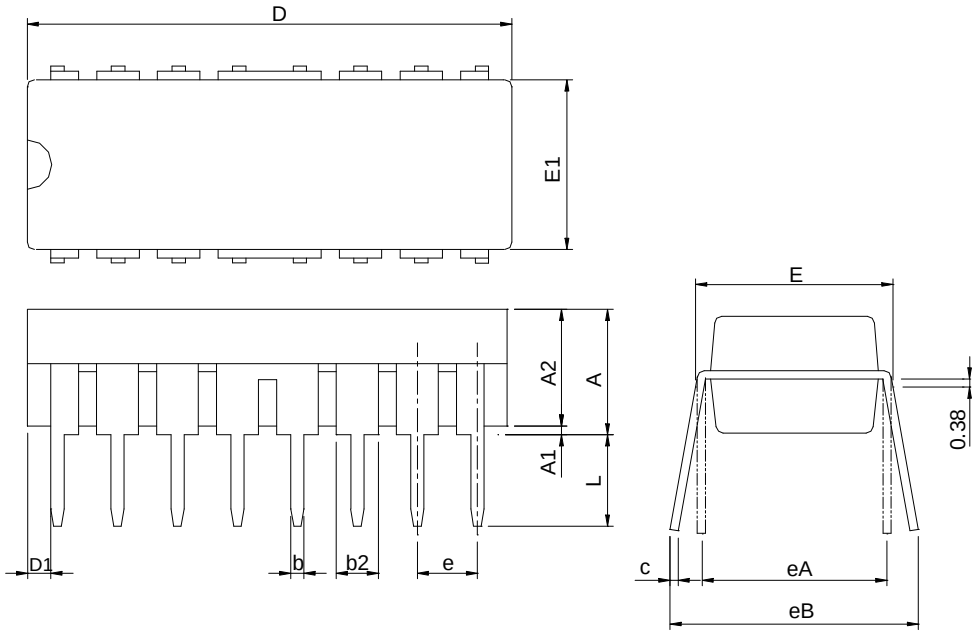


SYMBOL	DIP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	18.6	20.31	0.732	0.800
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note : 1. Followed from JEDEC MS-001AB
2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Package Information

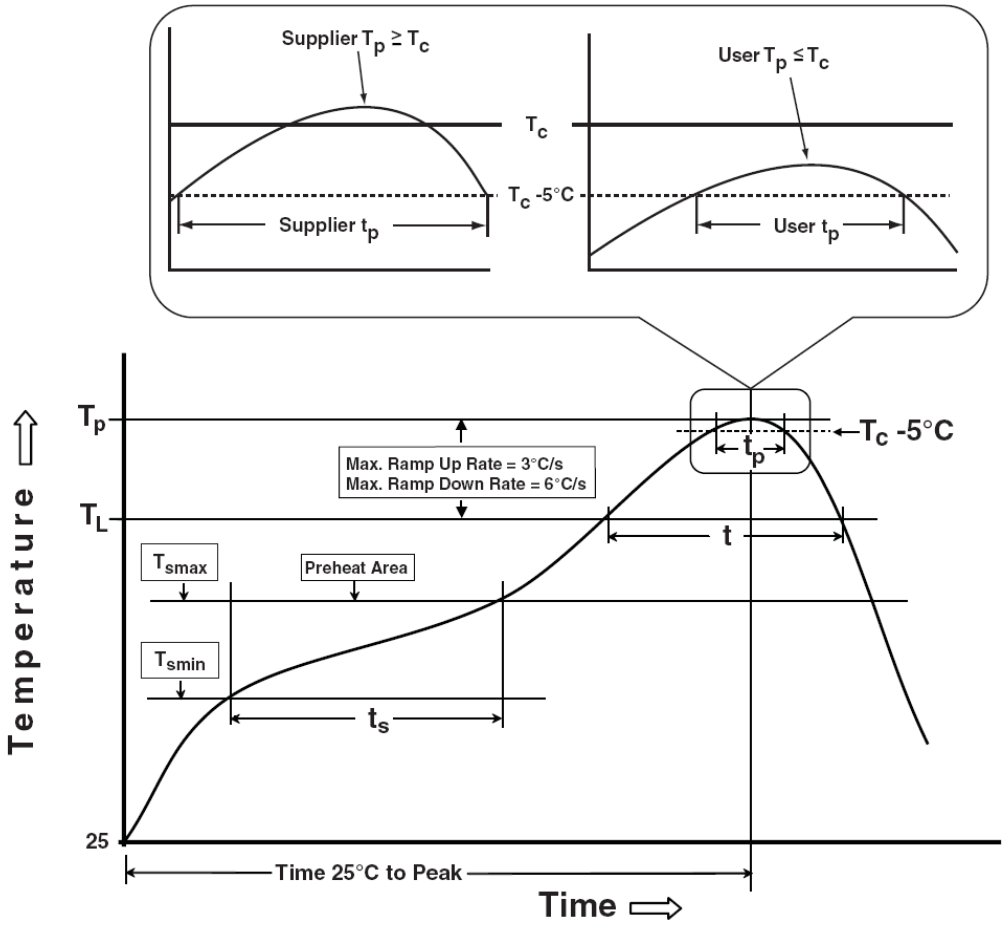
DIP-16A



SYMBOL	DIP-16A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	18.6	20.31	0.732	0.800
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note : 1. Followed from JEDEC MS-001AB
2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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