

2.8W Stereo Class-D Audio Power Amplifier (with DC Volume Control, AGC Function)

Features

- **Operating Voltage: 3.3V-5.5V**
- **High Efficiency 85% at $P_o=2.8W$, 4W Speaker, $V_{DD}=5V$**
- **Filter-Free Class-D Amplifier**
- **Low Shutdown Current**
– $I_{DD}=1mA$ at $V_{DD}=5V$
- **64 Steps Volume Adjustable from -80dB to +20dB by DC Voltage with Hysteresis**
- **AGC (Non-Clip) Function**
- **Output Power at THD+N=1%**
– 2.3W at $V_{DD}=5V$, $R_L=4W$
– 1.3W at $V_{DD}=5V$, $R_L=8W$
Output Power at THD+N=10%
– 2.8W at $V_{DD}=5V$, $R_L=4W$
– 1.6W at $V_{DD}=5V$, $R_L=8W$
- **Less External Components Required**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Power Enhanced Packages SSOP-24, SOP-18, SSOP-24P & QFN4x4-20A**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- LCD TVs
- DVD Player
- Active Speakers

General Description

The APA2605 is a stereo, high efficiency, filter-free Class-D audio amplifier available in SOP-18, SSOP-24, SSOP-24P, and QFN4x4-20A packages.

The APA2605 provides the precise DC volume control, the gain range is from -80dB ($V_{VOLUME}=0V$) to +20dB ($V_{VOLUME}=5V$) with 64 steps precise control. It's easy to get the suitable amplifier's gain with the 64 steps gain setting. The filter-free architecture eliminates the output filters compared to the traditional Class-D audio amplifier, and reduces the external component counts and the components high, it could save the PCB space, system cost, simplifies the design and the power loss at filter.

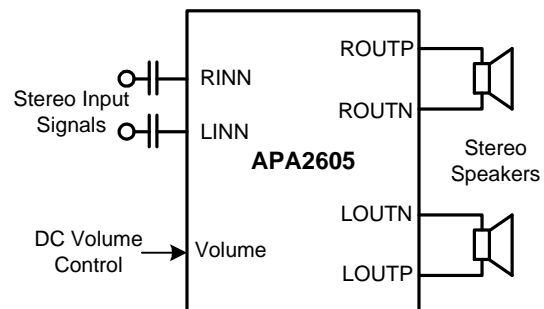
APA2605 provides an AGC (Non-Clip) function, and this function can low down the dynamic range for large input signal. APA2605 can provide from 20dB to -80dB with 64 steps gain decrease for non-clipping function, and this function can avoid output signal clipping.

The APA2605 also integrates the de-pop circuitry that reduces the pops and click noise during power on/off or shutdown enable process.

The APA2605 has build-in over-current and thermal protection that prevent the chip being destroyed by short-circuit or over-temperature situation.

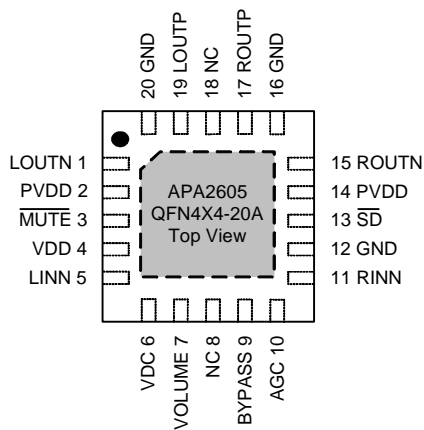
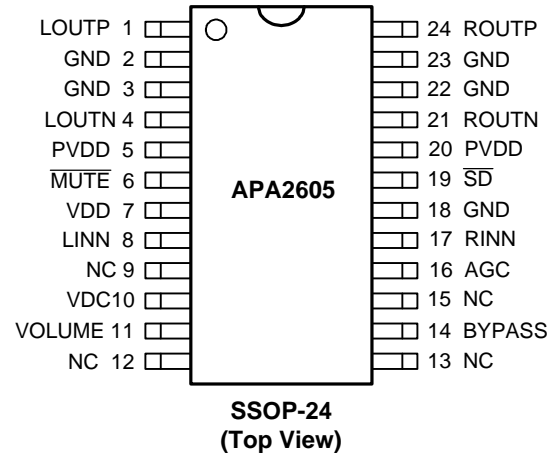
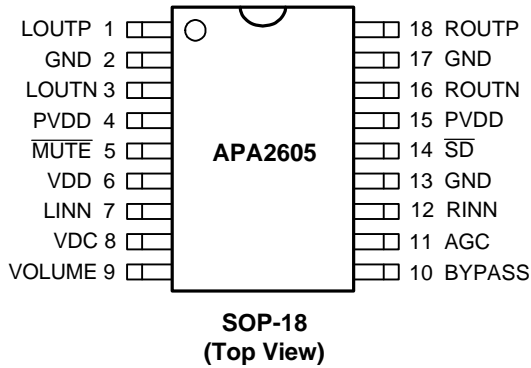
APA2605 is capable of driving 2.8W at 5V into 4Ω speaker. The efficiency can archive 85% at $R_L=4Ω$ when $P_o=2.8W$ at $V_{DD}=5V$.


Simplified Application Circuit

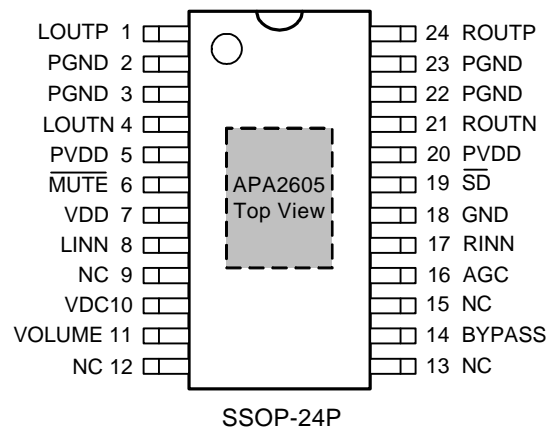


ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

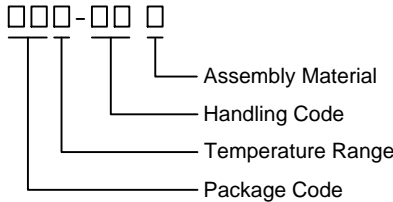




Pin Configuration



 = Thermal Pad (connected the Thermal Pad to GND plane for better dissipation)



Ordering and Marking Information

<p>APA2605</p>  <p> □□□ - □□ □ ———— Assembly Material ———— Handling Code ———— Temperature Range ———— Package Code </p>	<p>Package Code N : SSOP-24 NA : SSOP-24P K : SOP-18 QA : QFN4x4-20A Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APA2605 N:</p>	 <p>XXXXX - Date Code</p>
<p>APA2605 NA:</p>	 <p>XXXXX - Date Code</p>
<p>APA2605 K:</p>	 <p>XXXXX - Date Code</p>
<p>APA2605 QA:</p>	 <p>XXXXX - Date Code</p>

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage (VDD, PVDD, VDC to GND)	-0.3 to 6.5	V
	Input Voltage (LINN, RINN to GND)	-0.3 to V _{DD} +0.3	
	Input Voltage (\overline{SD} , \overline{MUTE} , AGC, VDC, VOLUME and BYPASS to GND)	-0.3 to V _{DD} +0.3	
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to +150	
T _{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	
P _D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit	
θ _{JA}	Thermal Resistance -Junction to Ambient ^(Note 2)	QFN4x4-20A	45	°C/W
		SSOP-24	96	
		SOP-18	70	
		SSOP-24P	45	
θ _{JC}	Thermal Resistance -Junction to Case ^(Note 3)	QFN4x4-20A	7	°C/W
		SSOP-24	18	
		SOP-18	16	
		SSOP-24P	11	

Note 2: Please refer to "Layout Recommendation", the GND PIN on the central of the IC should connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: The case temperature is measured at the center of the GND PIN on the underside of the SSOP-24, SOP-18 and QFN 4x4-20A packages.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit	
V _{DD}	Supply Voltage	3.3 ~ 5.5	V	
V _{IH}	High Level Threshold Voltage	\overline{SD} , \overline{MUTE}		2 ~ V _{DD}
V _{IL}	Low Level Threshold Voltage	\overline{SD} , \overline{MUTE}		0 ~ 0.8
V _{ICM}	Common Mode Input Voltage			1 ~ V _{DD} -1
T _A	Ambient Temperature Range		-40 ~ 85	°C
T _J	Junction Temperature Range		-40 ~ 125	
R _L	Speaker Resistance		3.5 ~	Ω

Electrical Characteristics

$V_{DD}=5V$, $V_{GND}=0V$, $T_A=25^{\circ}C$, Gain=20dB (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2605			Unit	
			Min.	Typ.	Max.		
$V_{DD}=5V$, $V_{GND}=0V$, $T_A=25^{\circ}C$, GAIN=20dB							
V_{BYPASS}	Bypass Pin Voltage		0.49x V_{DD}	0.5x V_{DD}	0.51x V_{DD}	V	
I_{DD}	Supply Current	$V_{MUTE}=0V$, $V_{SD}=5V$, No Load	-	5	13	mA	
I_{SD}	Shutdown Current	$V_{MUTE}=0V$, $V_{SD}=0V$, No Load	-	-	1	μA	
I_i	Input Current	\overline{SD} , MUTE, VOLUME	-	-	1		
F_{OSC}	Oscillator Frequency	($V_{DD}=3.3\text{--}5.5V$, $T_A=-40\text{--}85^{\circ}C$)	400	500	600	kHz	
$R_{i(min)}$	Minimum Input Resistance	Gain=20dB	36	43	50	k Ω	
$R_{DS(on)}$	Static Drain-Source On-State Resistance	Power MOSFET (P+N)	$V_{DD}=5.5V$, $I_L=0.8A$	-	690	-	m Ω
			$V_{DD}=4.5V$, $I_L=0.6A$	-	720	-	
			$V_{DD}=3.6V$, $I_L=0.4A$	-	760	-	
$T_{START-UP}$	Start-Up Time from Shutdown	Bypass Capacitor, $C_1=2.2\mu F$	-	1.2	-	s	
$V_{DD}=5V$, $T_A=25^{\circ}C$, GAIN=6dB							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=4\Omega$	-	2.3	-	W
			$R_L=8\Omega$	-	1.3	-	
		THD+N=10% $f_{in}=1kHz$	$R_L=4\Omega$	-	2.8	-	
			$R_L=8\Omega$	-	1.6	-	
η	Efficiency	$R_L=4\Omega$, $P_O=2.8W$	80	85	-	%	
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=4\Omega$, $P_O=1.6W$	-	0.1	0.3	%
			$R_L=8\Omega$, $P_O=0.8W$	-	0.08	0.2	
Crosstalk	Channel Separation	$P_O=0.2W$, $R_L=4\Omega$, $f_{in}=1kHz$	-	-100	-60	dB	
PSRR	Power Supply Rejection Ratio	$R_L=4\Omega$, Input AC-Ground	$f_{in}=100Hz$	-	-60		-50
			$f_{in}=1kHz$	-	-70		-60
SNR	Signal to Noise Ratio	With A-Weighting Filter $V_O=1V_{rms}$, $R_L=8\Omega$	-80	-85	-		
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz$, $R_L=8\Omega$, $V_{IN}=1V_{rms}$	-	-100	-80	dB	
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz$, $R_L=8\Omega$, $V_{IN}=1V_{rms}$	-	-120	-90		
V_n	Output Noise	With A-Weighting Filter (Gain = 20dB)	-	80	100	μV_{rms}	
V_{OS}	Output Offset Voltage	$R_L=4\Omega$ (Gain=20dB)	-	20	30	mV	
$V_{DD}=3.6V$, $T_A=25^{\circ}C$, GAIN=6dB							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=4\Omega$	1.0	1.1	-	W
			$R_L=8\Omega$	0.6	0.65	-	
		THD+N=10% $f_{in}=1kHz$	$R_L=4\Omega$	-	1.4	-	
			$R_L=8\Omega$	-	0.85	-	
η	Efficiency	$R_L=4\Omega$, $P_O=1.4W$	78	83	-	%	

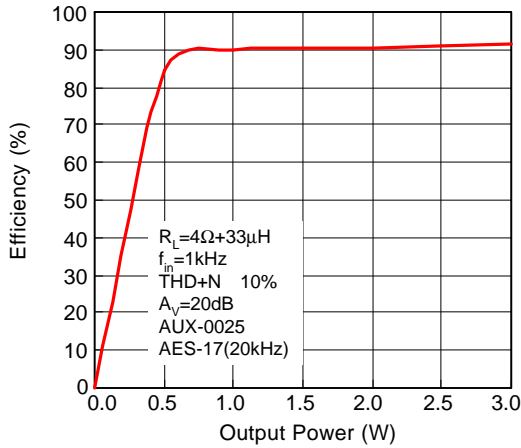
Electrical Characteristics (Cont.)

$V_{DD}=5V$, $V_{GND}=0V$, $T_A=25^{\circ}C$, Gain=20dB (unless otherwise noted)

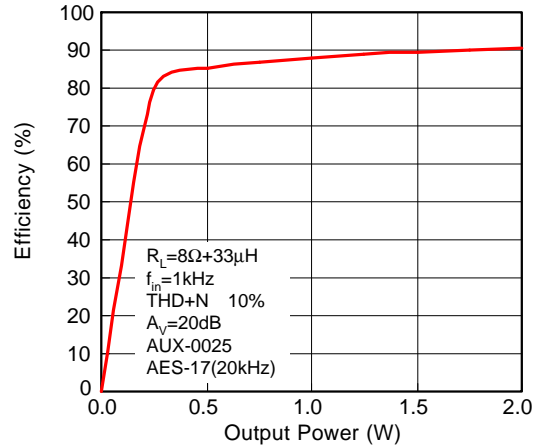
Symbol	Parameter	Test Conditions	APA2605			Unit	
			Min.	Typ.	Max.		
$V_{DD}=3.6V$, $T_A=25^{\circ}C$, GAIN=6dB (CONT.)							
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=4\Omega$, $P_O=0.8W$	-	0.2	0.4	%
			$R_L=8\Omega$, $P_O=0.5W$	-	0.1	0.3	
Crosstalk	Channel Separation	$P_O=0.1W$, $R_L=4\Omega$, $f_{in}=1kHz$	-	-100	-60	dB	
PSRR	Power Supply Rejection Ratio	$R_L=4\Omega$, Input AC-Ground	$f_{in}=100Hz$	-	-60		-50
			$f_{in}=1kHz$	-	-70		-60
SNR	Signal to Noise Ratio	With A-Weighting Filter $V_O=1V_{rms}$, $R_L=8\Omega$	-80	-85	-		
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz$, $R_L=8\Omega$, $V_{IN}=1V_{rms}$	-	-100	-80		
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz$, $R_L=8\Omega$, $V_{IN}=1V_{rms}$	-	-120	-90		
V_n	Output Noise	With A-Weighting Filter (Gain=20dB)	-	80	-	μV_{rms}	
V_{OS}	Output Offset Voltage	$R_L=4\Omega$ (Gain=20dB)	-	20	30	mV	

Typical Operating Characteristics

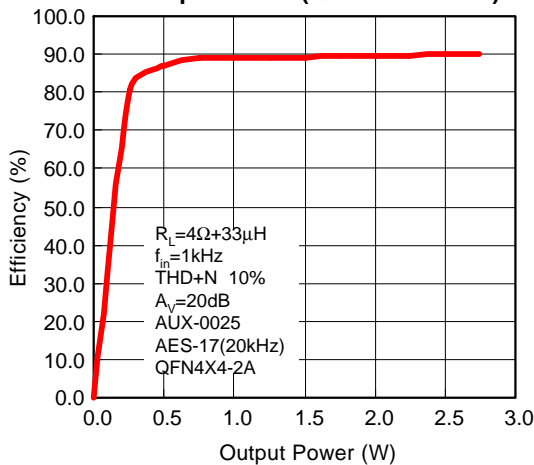
Efficiency vs. Output Power (4W)



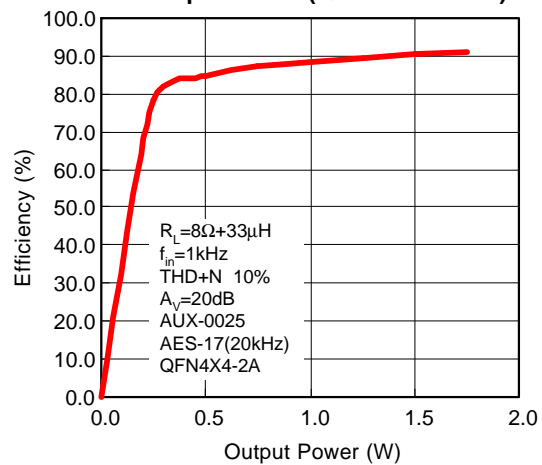
Efficiency vs. Output Power (8W)



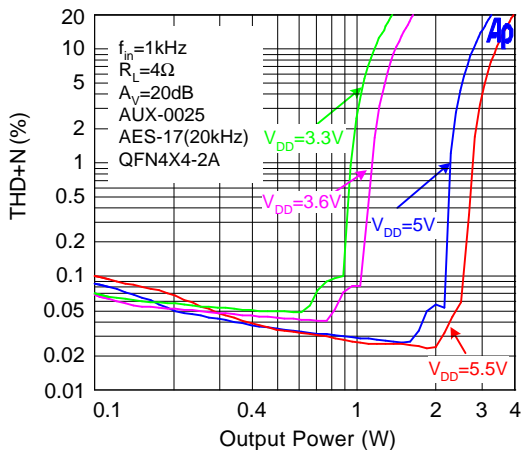
Efficiency vs. Output Power (QFN4X4-20A 4W)



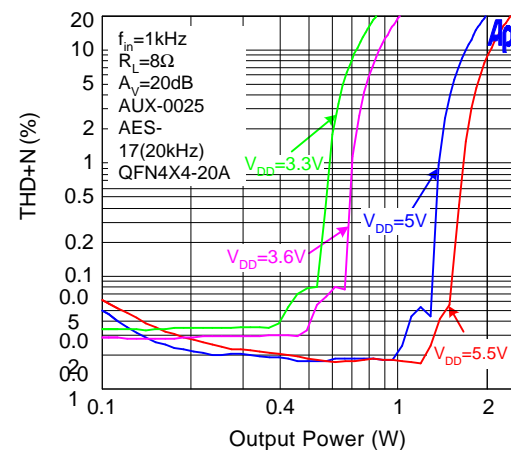
Efficiency vs. Output Power (QFN4X4-20A 8W)



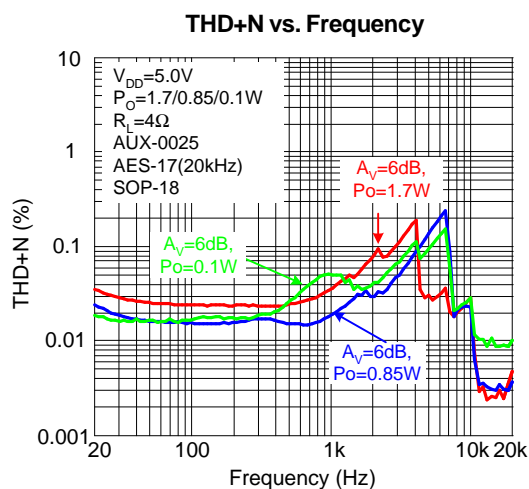
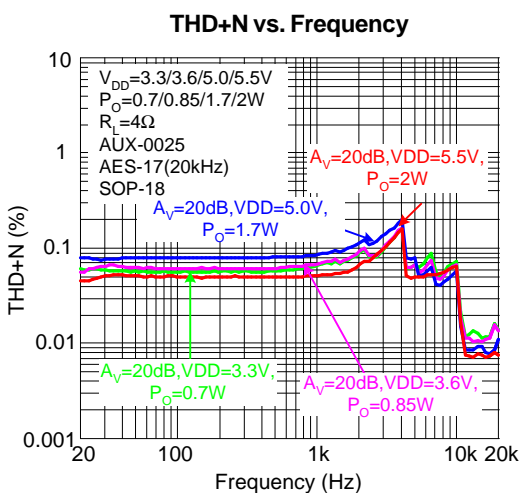
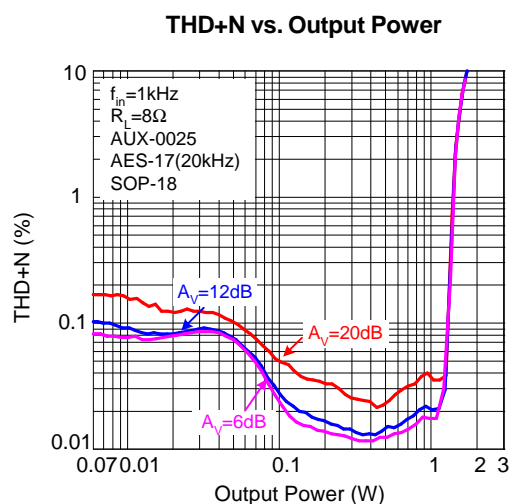
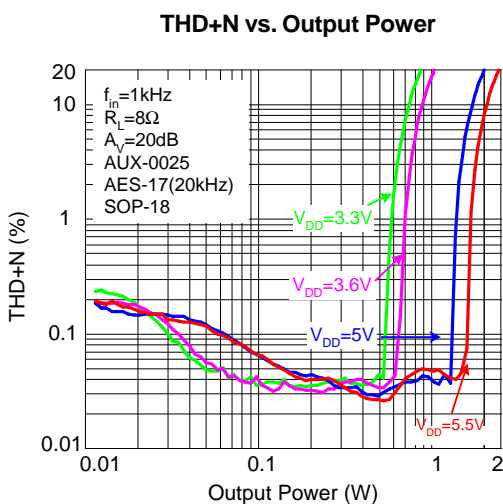
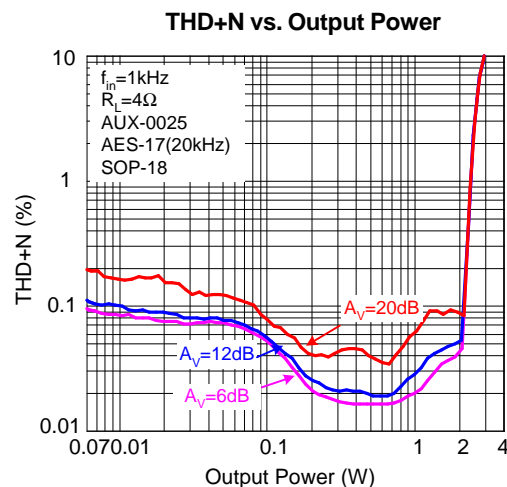
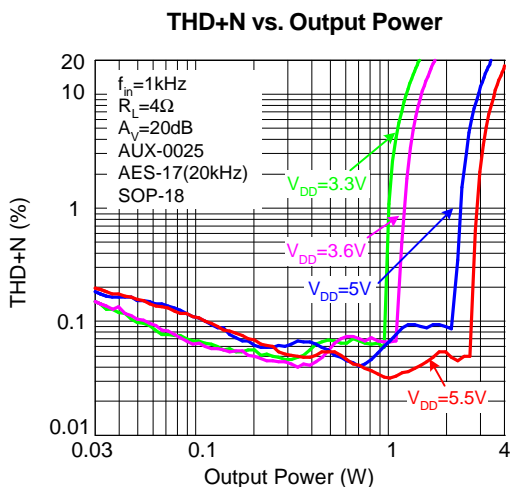
THD+N vs. Output Power



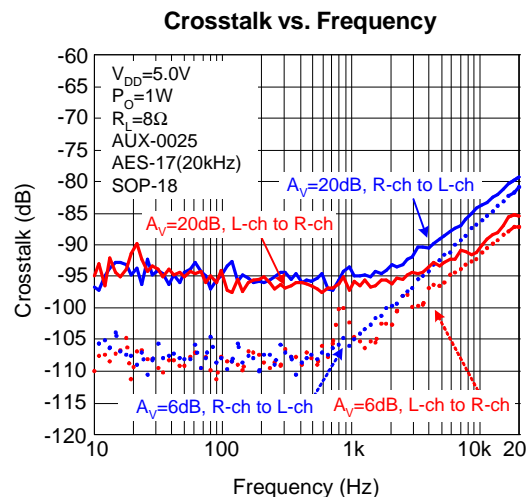
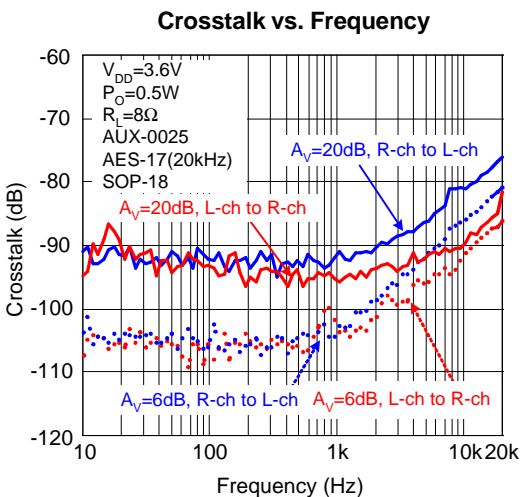
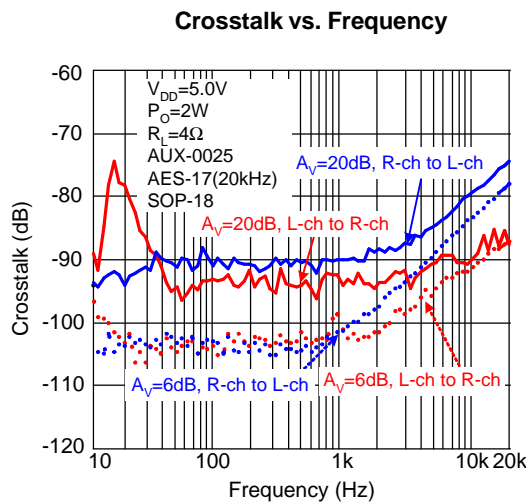
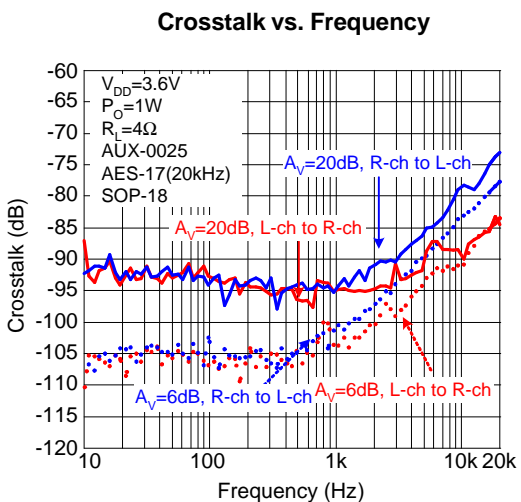
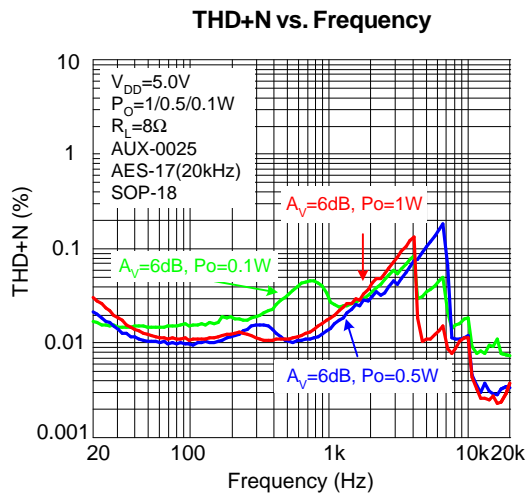
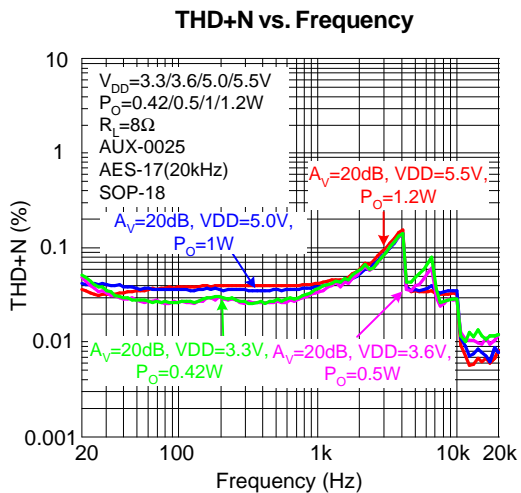
THD+N vs. Output Power



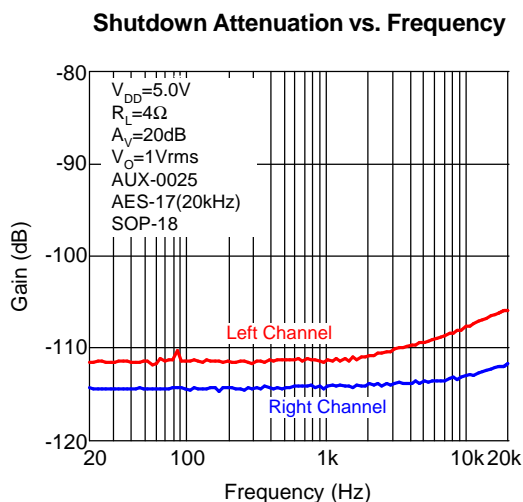
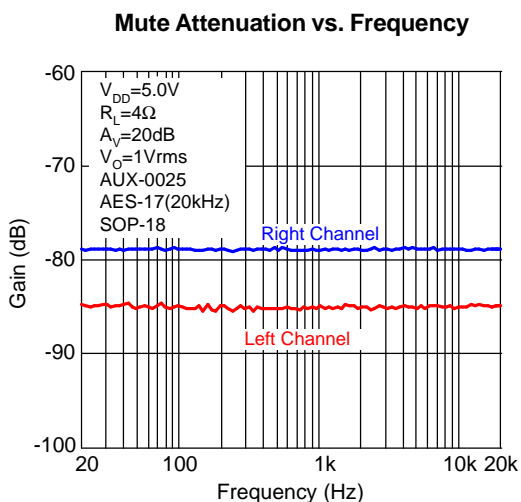
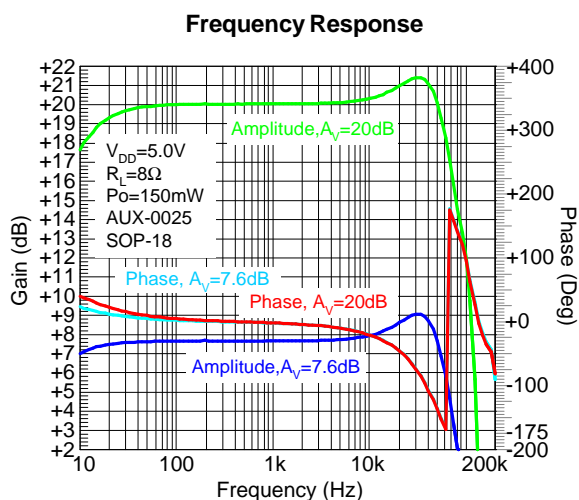
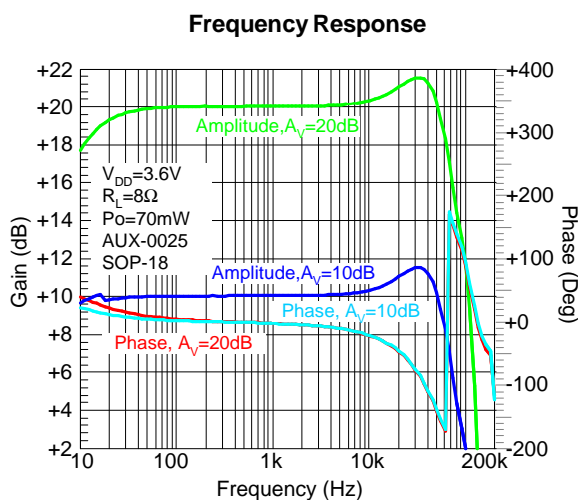
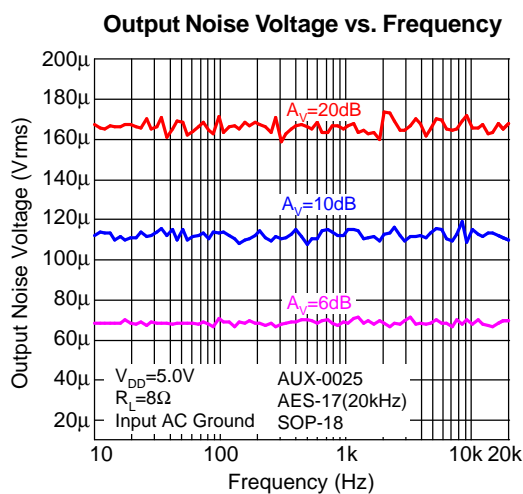
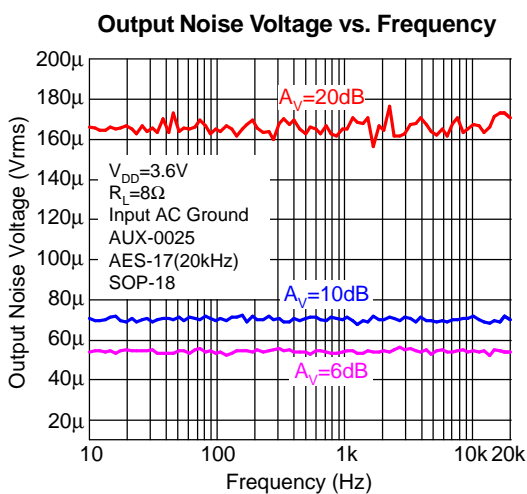
Typical Operating Characteristics (Cont.)



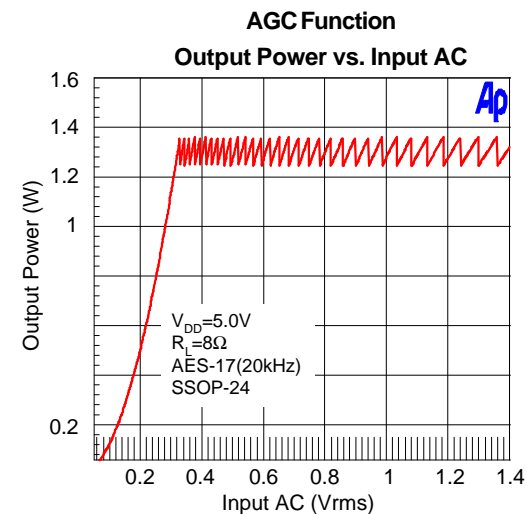
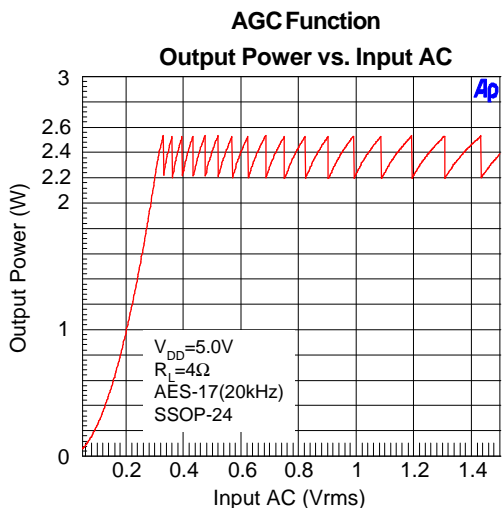
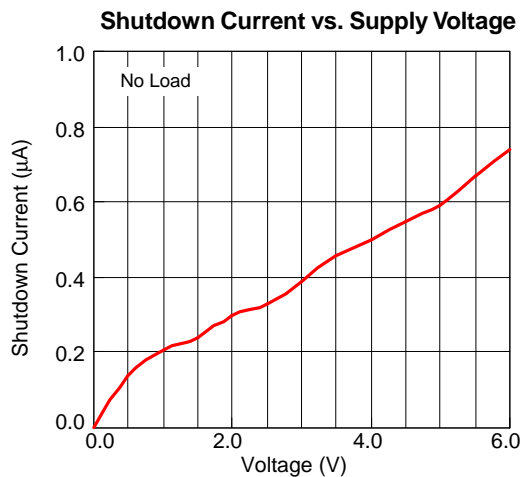
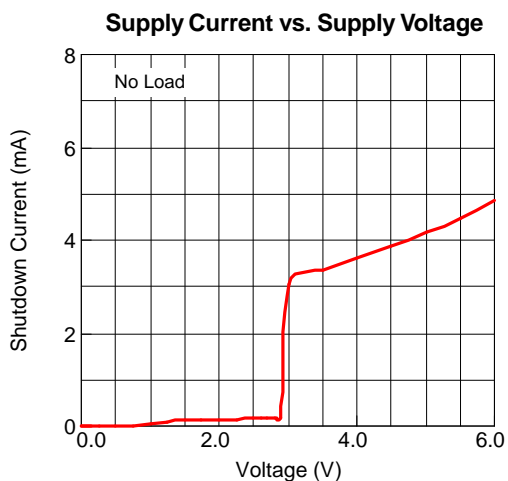
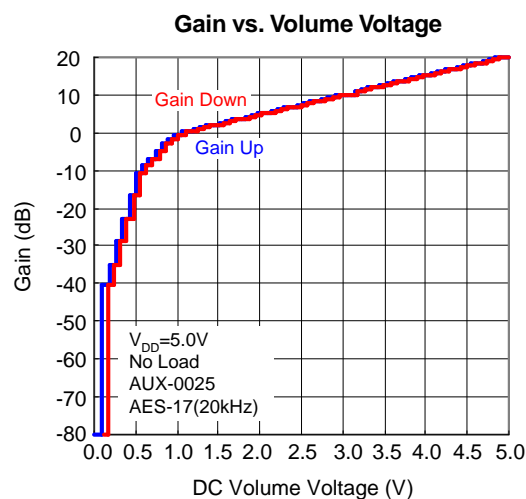
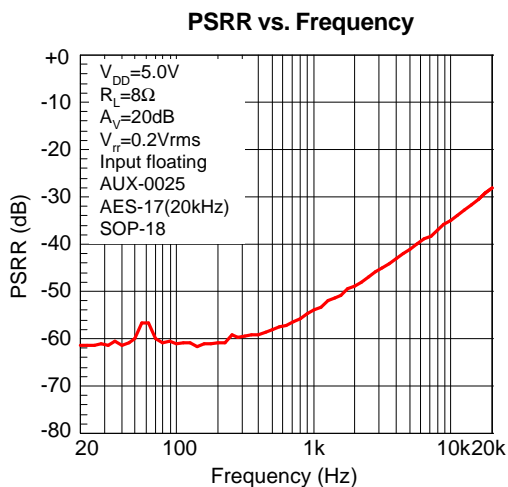
Typical Operating Characteristics (Cont.)



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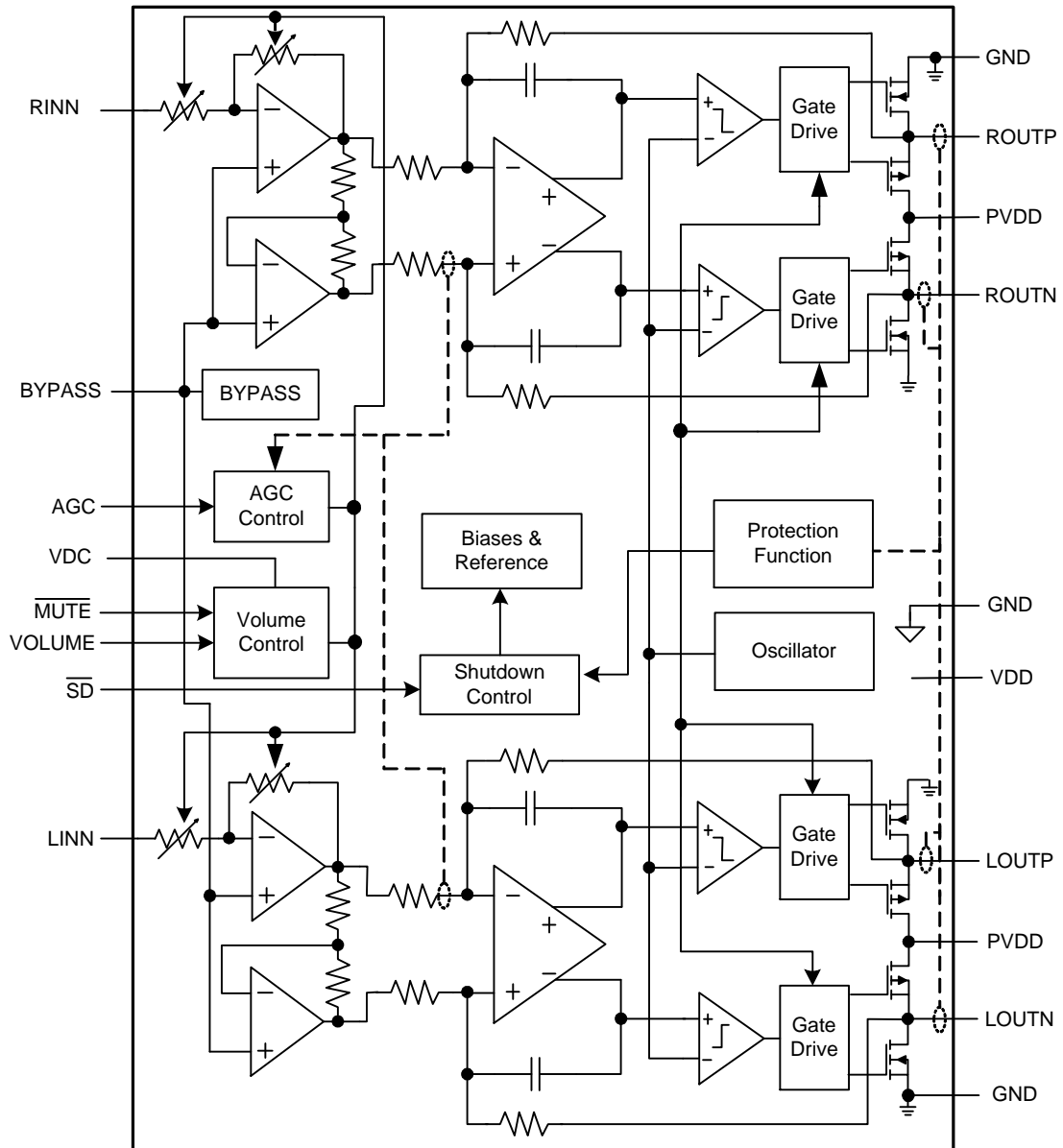
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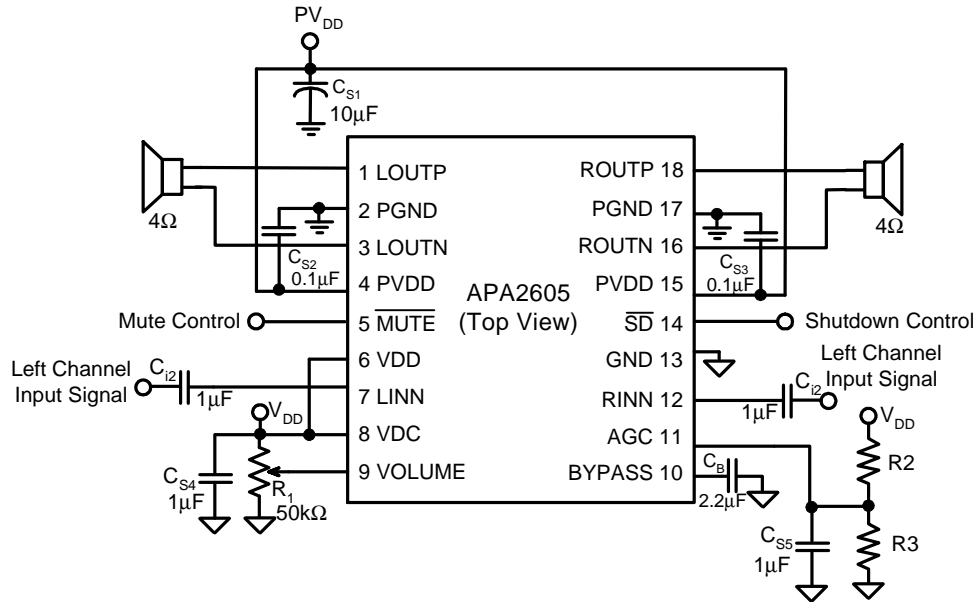
Pin Description

PIN			NAME	I/O/P	FUNCTION
NO.					
SSOP-24	SOP-18	QFN4x4-20A			
1	1	19	LOUTP	O	Positive output of left channel power amplifier.
4	3	1	LOUTN	O	Negative output of left channel power amplifier.
5,20	4,15	2,14	PVDD	P	Power amplifier's power supply.
6	5	3	MUTE	I	Mute control signal input. Place entire IC in mute mode when held low.
7	6	4	VDD	P	Control and bias block's power supply.
8	7	5	LINN	I	Negative input of left channel power amplifier.
9,12,13,15	-	8,18	NC	-	No connection.
10	8	6	VDC	P	Volume control block's power supply.
11	9	7	VOLUME	I	Internal gain setting input.
14	10	9	BYPASS	P	Bias voltage for power amplifiers.
16	11	10	AGC	I	Maximum output power setting input. When held high disable AGC function.
17	12	11	RINN	I	Negative input of right channel power amplifier.
2,3,18,22,23	2,13,17	12,16,20	GND	P	Control and bias block's ground.
19	14	13	SD	I	Shutdown mode control input. Place entire IC in shutdown mode when held low.
21	16	15	ROUTN	O	Negative output of right channel power amplifier.
24	18	17	ROUTP	O	Positive output of right channel power amplifier.

Block Diagram



Typical Application Circuit



VDD=5V

RL (W)	R2 (kW)	R3 (kW)	Po (W)	V _{AGC} (V)
4	30.1	12.0	2.19	1.425
	26.7	12.0	1.71	1.550
8	30.9	12.0	1.15	1.400

Note 4 :The resistance must use 1%.

DC Volume Control Table

Step	Gain	Low (%)	High (%)	Recom (%)	Low (5V)	High (5V)	Recom (5V)
1	20.0	97.7	100.0	100.0	4.885	5.000	5.00
2	19.6	96.2	96.6	96.4	4.808	4.830	4.82
3	19.2	94.6	95.1	94.8	4.731	4.753	4.74
4	18.8	93.1	93.5	93.3	4.653	4.675	4.66
5	18.4	91.5	92.0	91.7	4.576	4.598	4.59
6	18.0	90.0	90.4	90.2	4.499	4.521	4.51
7	17.6	88.4	88.9	88.6	4.421	4.443	4.43
8	17.2	86.9	87.3	87.1	4.344	4.366	4.36
9	16.8	85.3	85.8	85.6	4.267	4.289	4.28
10	16.4	83.8	84.2	84.0	4.189	4.211	4.20
11	16.0	82.2	82.7	82.5	4.112	4.134	4.12
12	15.6	80.7	81.1	80.9	4.035	4.057	4.05
13	15.2	79.1	79.6	79.4	3.957	3.980	3.97
14	14.8	77.6	78.0	77.8	3.880	3.902	3.89
15	14.4	76.1	76.5	76.3	3.803	3.825	3.81
16	14.0	74.5	75.0	74.7	3.725	3.748	3.74
17	13.6	73.0	73.4	73.2	3.648	3.670	3.66
18	13.2	71.4	71.9	71.6	3.571	3.593	3.58
19	12.8	69.9	70.3	70.1	3.493	3.516	3.50
20	12.4	68.3	68.8	68.5	3.416	3.438	3.43
21	12.0	66.8	67.2	67.0	3.339	3.361	3.35
22	11.6	65.2	65.7	65.5	3.261	3.284	3.27
23	11.2	63.7	64.1	63.9	3.184	3.207	3.20
24	10.8	62.1	62.6	62.4	3.107	3.129	3.12
25	10.4	60.6	61.0	60.8	3.029	3.052	3.04
26	10.0	59.0	59.5	59.3	2.952	2.975	2.96
27	9.6	57.5	57.9	57.7	2.875	2.897	2.89
28	9.2	55.9	56.4	56.2	2.797	2.820	2.81
29	8.8	54.4	54.9	54.6	2.720	2.743	2.73
30	8.4	52.9	53.3	53.1	2.643	2.665	2.65
31	8.0	51.3	51.8	51.5	2.565	2.588	2.58
32	7.6	49.8	50.2	50.0	2.488	2.511	2.50
33	7.2	48.2	48.7	48.4	2.411	2.433	2.42
34	6.8	46.7	47.1	46.9	2.333	2.356	2.34
35	6.4	45.1	45.6	45.3	2.256	2.279	2.27
36	6.0	43.6	44.0	43.8	2.179	2.202	2.19
37	5.6	42.0	42.5	42.3	2.101	2.124	2.11
38	5.2	40.5	40.9	40.7	2.024	2.047	2.04

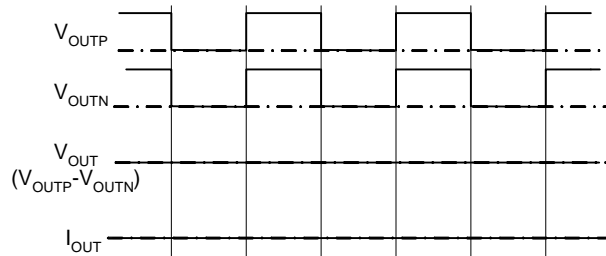
DC Volume Control Table (Cont.)

Step	Gain	Low (%)	High (%)	Recom (%)	Low (5V)	High (5V)	Recom (5V)
39	4.8	38.9	39.4	39.2	1.947	1.970	1.96
40	4.4	37.4	37.8	37.6	1.869	1.892	1.88
41	4.0	35.8	36.3	36.1	1.792	1.815	1.80
42	3.6	34.3	34.8	34.5	1.715	1.738	1.73
43	3.2	32.7	33.2	33.0	1.637	1.660	1.65
44	2.8	31.2	31.7	31.4	1.560	1.583	1.57
45	2.4	29.6	30.1	29.9	1.482	1.506	1.49
46	2.0	28.1	28.6	28.3	1.405	1.429	1.42
47	1.6	26.6	27.0	26.8	1.328	1.351	1.34
48	1.2	25.0	25.5	25.2	1.250	1.274	1.26
49	0.8	23.5	23.9	23.7	1.173	1.197	1.18
50	0.4	21.9	22.4	22.2	1.096	1.119	1.11
51	0.0	20.4	20.8	20.6	1.018	1.042	1.03
52	-1.0	18.8	19.3	19.1	0.941	0.965	0.95
53	-2.0	17.3	17.7	17.5	0.864	0.887	0.88
54	-3.0	15.7	16.2	16.0	0.786	0.810	0.80
55	-5.0	14.2	14.7	14.4	0.709	0.733	0.72
56	-7.0	12.6	13.1	12.9	0.632	0.655	0.64
57	-9.0	11.1	11.6	11.3	0.554	0.578	0.57
58	-11.0	9.5	10.0	9.8	0.477	0.501	0.49
59	-17.0	8.0	8.5	8.2	0.400	0.424	0.41
60	-23.0	6.4	6.9	6.7	0.322	0.346	0.33
61	-29.0	4.9	5.4	5.1	0.245	0.269	0.26
62	-35.0	3.4	3.8	3.6	0.168	0.192	0.18
63	-41.0	1.8	2.3	2.0	0.090	0.114	0.10
64	-80.0	0.0	3.8	0.0	0.000	0.192	0.00

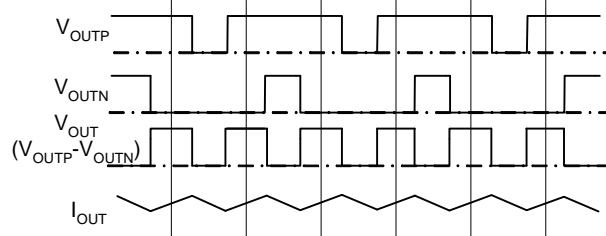
Function Description

Class-D Operation

Output = 0V



Output > 0V



Output < 0V

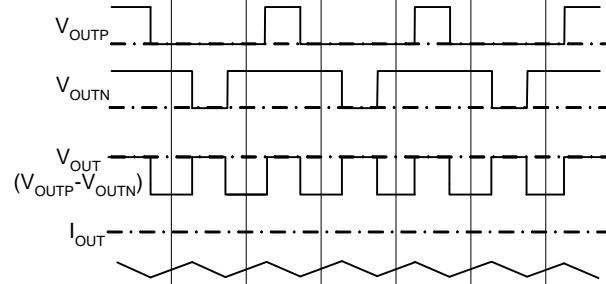


Figure 1. The APA2605 Output Waveform (Voltage & Current)

The APA2605 power amplifier modulation scheme is shown in figure 1; the outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output $> 0V$, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when Output $< 0V$, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load, and reduces the I^2R losses in the load that improve the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Bypass Voltage

The bypass voltage is equal to $V_{DD}/2$, this voltage is for bias the internal preamplifier stages. The external capacitor for this reference (C_B) is a critical component and serves several important functions.

DC Volume Control Function

The APA2605 has an internal stereo volume control whose setting is the function of the DC voltage applied to the VOLUME input pin. The APA2605 volume control consists of 64 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps controlled by the DC voltage, are from +20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in the table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the "DC Volume Control Graph."

For the highest accuracy, the voltage shown in the "recommended voltage" column of the table is used to select a desired gain. This recommended voltage is exactly half-way between the two nearest transitions. The gains level have are 0.4dB/step from 20dB to 0dB; 1dB/step from 0dB to -3dB; 2dB/step from -3dB to -11dB and 6dB/step from -11dB to -41dB and the last step at -80dB as mute mode.

AGC (Non-Clipping) Function

The APA2605 provides the 64 steps non-clipping Control, and the range is from 20dB to -80dB. When the output reaches the maximum power setting value, the internal Programmable Gain Amplifier (PGA) will decrease the gain for prevent the output waveform clipping. This feature prevents speaker damage from occurring clipping. Using the AGC pin to set the non-clipping function and limit the output power.

Function Description (Cont.)

Table 1: AGC Setting Threshold v.s Output Power

AGC Function	Output Power
VDD~0.45VDD	Disable AGC Function
0.45VDD~0.27VDD	$P_O = \frac{8 \times 0.95 \left(\frac{1}{2} V_{DD} - V_{AGC} \right)^2}{RL}$
0.27VDD~GND (AGC Floating)	(Max Output Power 4Ω) Po=2.513W (Max Output Power 8Ω) Po=1.26W

Shutdown Operation

In order to reduce power consumption while not in use, the APA2605 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the SD pin for APA2605. The trigger point between a logic high and logic low level is typically 0.65V. It is the best to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the \overline{SD} pin to a low level, the amplifier enters a low-consumption-current state, I_{DD} for APA2605 is in shutdown mode. On normal operating, APA2605's \overline{SD} pin should pull to a high level to keep the IC out of the shutdown mode. The \overline{SD} pin should be tied to a definite voltage to avoid unwanted state changes.

Over-Current Protection

The APA2605 monitors the output current, and when the current exceeds the current-limit threshold, the APA2605 turn-off the output stage to prevent the output device from damages in over-current or short-circuit condition. The IC will turn-on the output buffer after 1ms, but if the over-current or short-circuits condition is still remain, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has be removed.

Thermal Protection

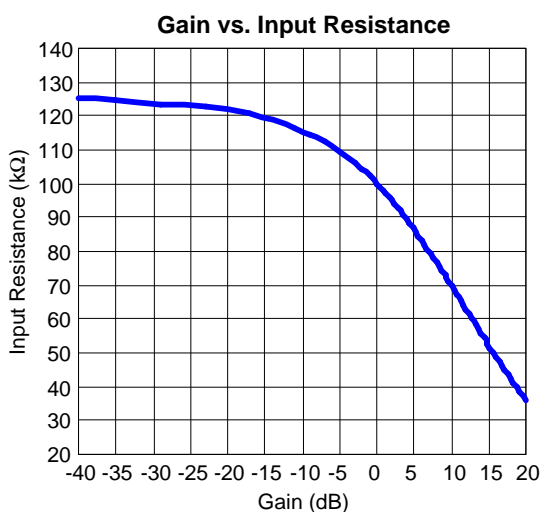
The over-temperature circuit limits the junction temperature of the APA2605. When the junction temperature exceeds $T_J=+150^{\circ}C$, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature going down to about $125^{\circ}C$. The thermal protection is designed with a $25^{\circ}C$ hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Application Information

Square Wave into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jumping out of the air gap and defacing the voice coil. However, this depends on the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 500kHz switching frequency, this is not issued for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor, R_i



For achieving the 64 steps gain setting, it varies the input resistance network (R_i & R_f) of amplifier. The input resistor's range from smallest to maximum is about six times. Therefore, the input high-pass filter's low cutoff frequency will change for six times from low to high. The cutoff frequency can be calculated by equation 1.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is $36k\Omega$ (minimum) and the specification calls for a flat bass response down to 50Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is $0.08\mu\text{F}$, so a value in the range of $0.01\mu\text{F}$ to $0.022\mu\text{F}$ would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network ($R_i + R_f, C_i$) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' inputs are held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The bypass capacitance affects the start-up time. It is determined in the following equation:

$$T_{\text{START-UP}} = 0.5(\text{sec}/\mu\text{F}) \times C_B + 0.2(\text{sec}) \quad (3)$$

The capacitor location on the bypass pin should be as close to the device as possible. The effect of a larger half bypass capacitor is improved PSRR due to increased half-supply stability. The selection of bypass capacitors, especially C_B , is thus dependent upon desired PSRR requirements, click and pop performance. To avoid the start-up pop noise occurred, choose C_i which is not larger than C_B .

Application Information (Cont.)

Ferrite Bead Selection

If the traces from APA2605 to speaker are short, the ferrite bead filters can reduce the high frequency radiated to meet the FCC & CE required.

A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output Low-Pass Filter

If the traces from APA2605 to speaker are short, it doesn't require output filter for FCC & CE standard.

A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite shows choosing high impedance in high frequency.

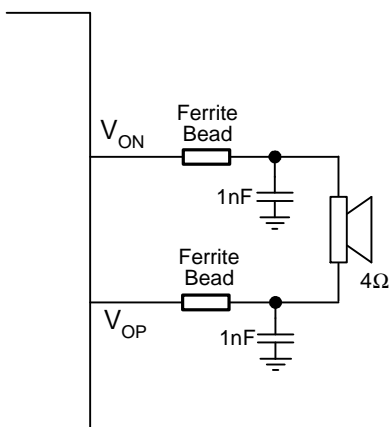


Figure 2. Ferrite Bead Output Filter

Figure 3 and 4 are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace from amplifier to speaker is too long and needs to eliminate the radiated emission or EMI.

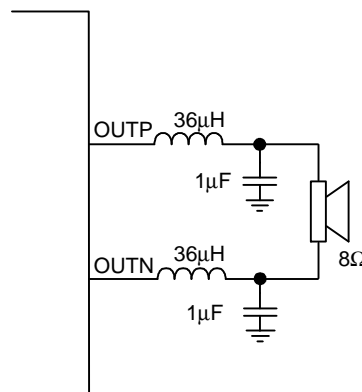


Figure 3. LC Output Filter for 8Ω Speaker

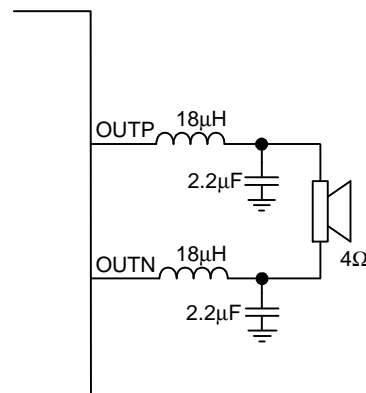


Figure 4. LC Output Filter for 4Ω Speaker

Figure 3 and 4's low pass filter cut-off frequency are 25kHz (F_c).

$$f_{C(\text{lowpass})} = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

Power-Supply Decoupling Capacitor, C_s

The APA2605 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

Application Information (Cont.)

Power-Supply Decoupling Capacitor, C_s (Cont.)

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically $0.1\mu\text{F}$ placed as close as possible to the device VDD pin for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of $10\mu\text{F}$ or greater placed near the audio power amplifier is recommended.

Layout Recommendation

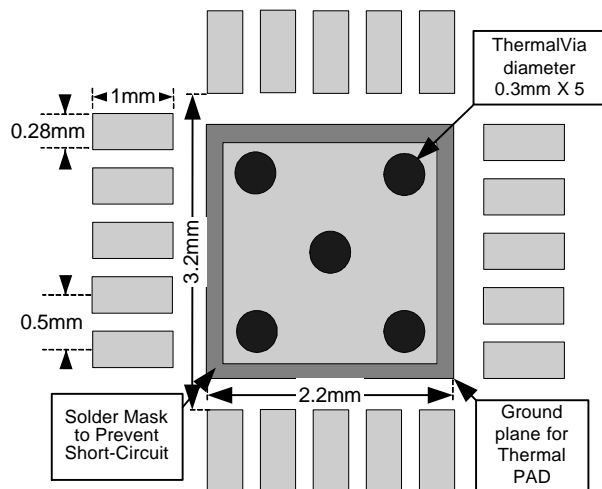
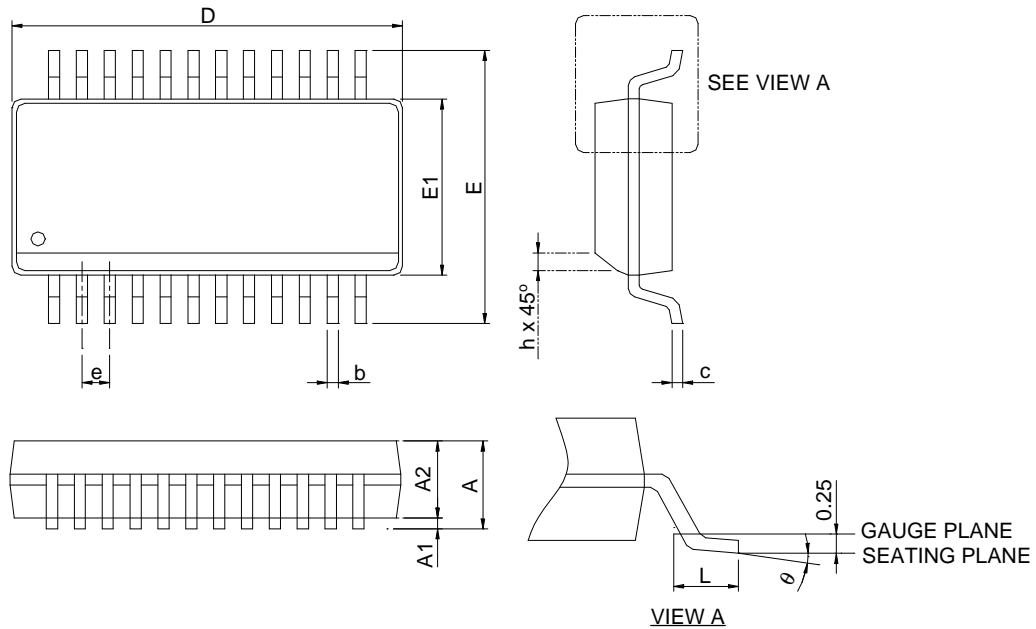


Figure 5. QFN4x4-20A Land Pattern Recommendation

1. All components should be placed close to the APA2605. For example, the input capacitor (C_i) should be close to APA2605's input pins to avoid causing noise coupling to APA2605's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2605's power pin to decouple the power rail noise.
2. The output traces should be short, wide ($>50\text{mil}$), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The QFN4X4-20A Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short-circuit) except the Thermal PAD area.

Package Information

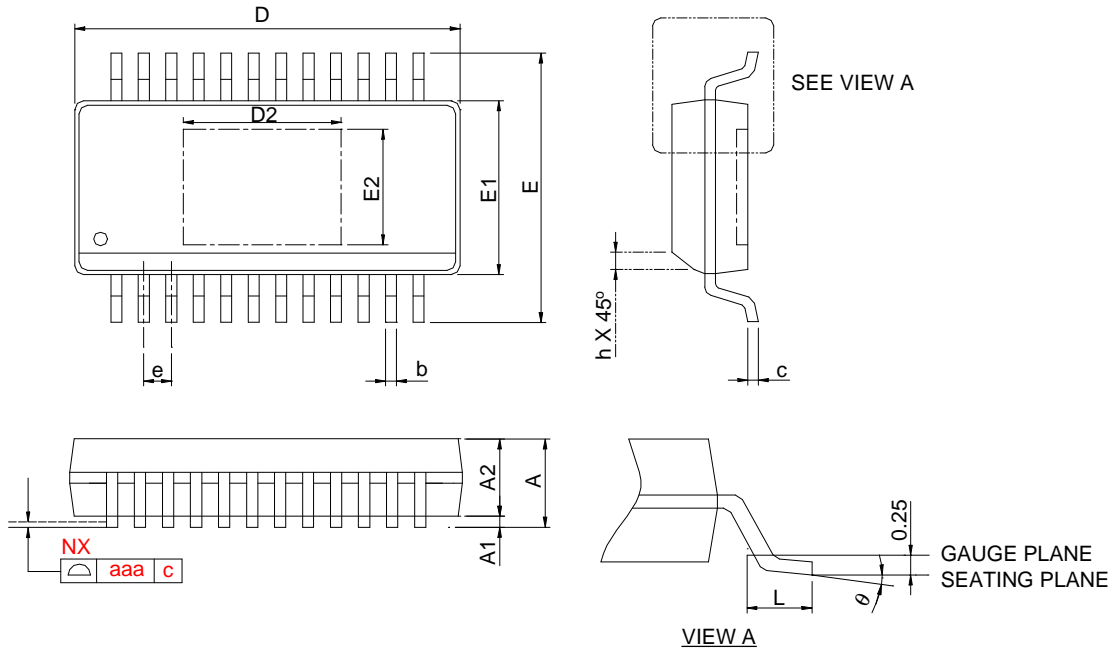
SSOP-24



SYMBOL	SSOP-24 (150mil)			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	8.56	8.76	0.337	0.345
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.158
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0°	8°	0°	8°

Package Information

SSOP-24P

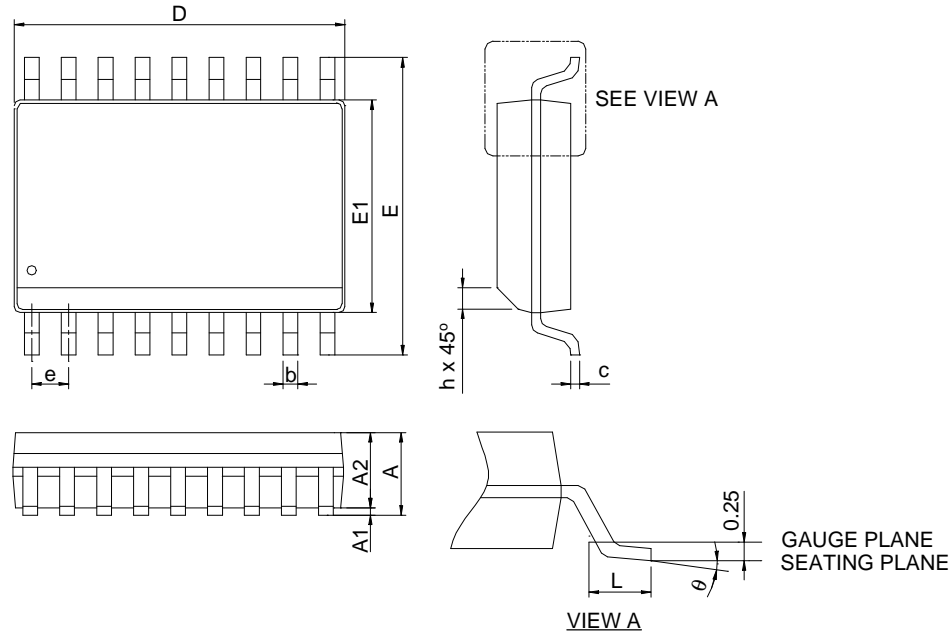


DIMENSIONS	SSOP-24P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	8.56	8.76	0.337	0.345
D2	3.20	4.00	0.126	0.158
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.158
E2	2.00	2.80	0.079	0.110
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0°	8°	0°	8°
aaa	0.10		0.004	

- Note : 1. Reference to JEDEC MO-137 AE.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

SOP-18

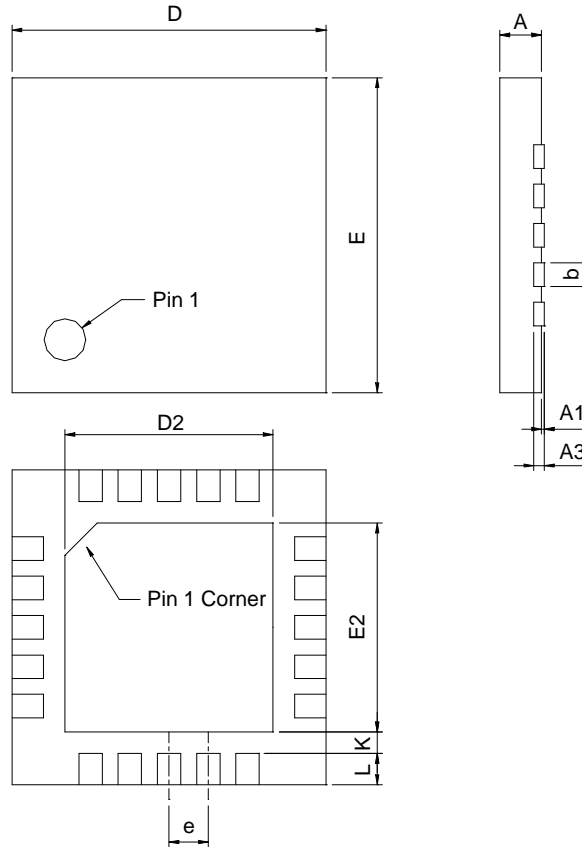


SYMBOL	SOP-18 (300mil)			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		2.65		0.104
A1	0.10	0.30	0.004	0.012
A2	2.05		0.081	
b	0.31	0.51	0.012	0.020
c	0.20	0.33	0.008	0.013
D	11.35	11.75	0.447	0.463
E	10.10	10.50	0.398	0.413
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
h	0.25	0.75	0.010	0.030
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note : 1. Followed from JEDEC MS-013 AB.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

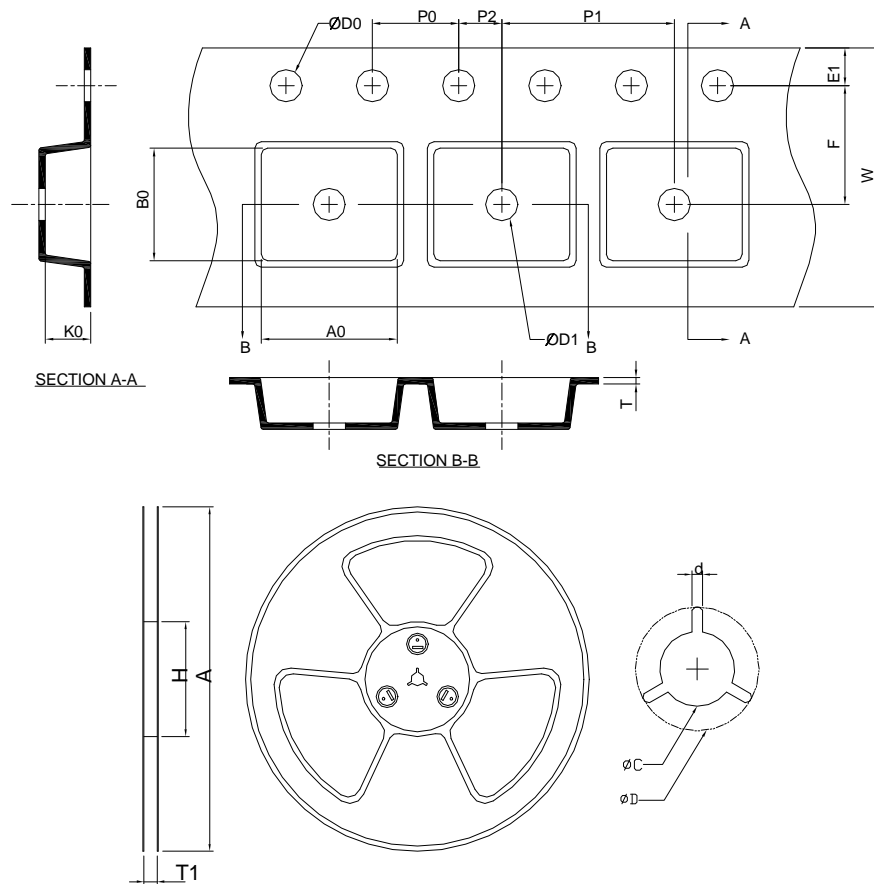
QFN4x4-20A



SYMBOL	QFN4x4-20A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.00	2.50	0.079	0.098
E	3.90	4.10	0.154	0.161
E2	2.00	2.50	0.079	0.098
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 VGGD-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SSOP-24	330±2.00	50MIN	24.40+2.00 -0.00	13.0+0.50 -0.20	1.5MIN	20.2MIN	24.0 ±0.30	1.75 ±0.10	11.5 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	12.0 ±0.10	2.0 ±0.10	5+0.10 -0.00	1.5MIN	0.60+0.00 -0.40	8.50 ±0.10	13.50 ±0.10	2.60 ±0.10
Application	A	H	T1	C	d	D	W	E1	F
SSOP-24P	330.0 ±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0 ±0.30	1.75 ±0.10	7.50 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	9.00 ±0.20	2.10 ±0.20
Application	A	H	T1	C	d	D	W	E1	F
SOP-18	330.0 ±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0 ±0.30	1.75 ±0.10	7.5 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	10.9 ±0.20	10.70 ±0.20	3.1 ±0.20

(mm)

Carrier Tape & Reel Dimensions (Cont.)

Application	A	H	T1	C	d	D	W	E1	F
QFN4x4-20A	330.0 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30 ±0.20	4.30 ±0.20	1.30 ±0.20

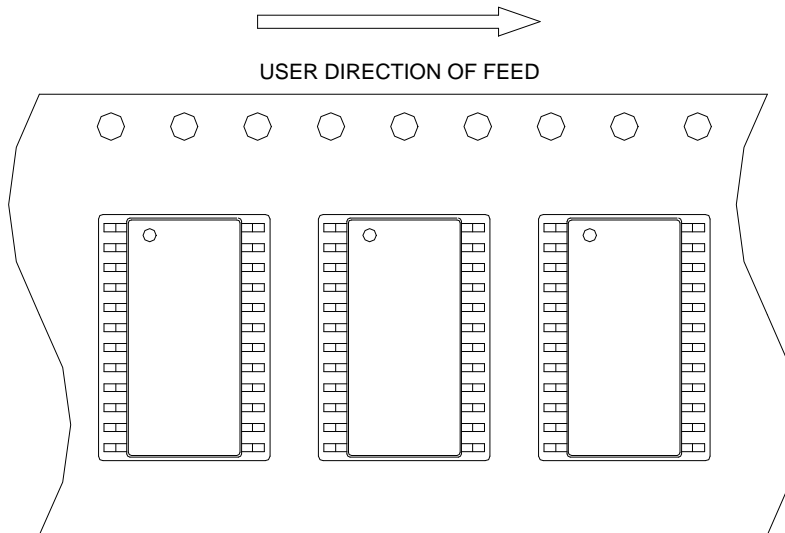
(mm)

Devices Per Unit

Package Type	Unit	Quantity
QFN4x4-20A	Tape & Reel	3000
SSOP-24(P)	Tape & Reel	2500
SOP-18	Tape & Reel	1000

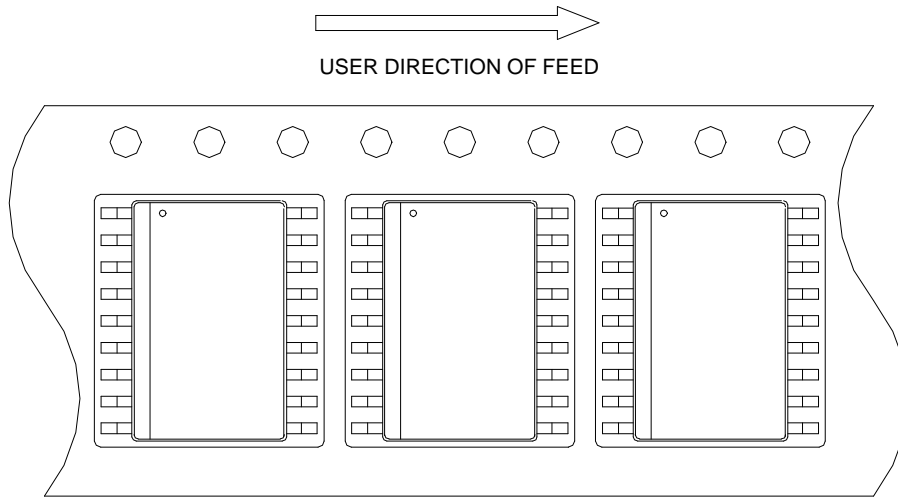
Taping Direction Information

SSOP-24(P)

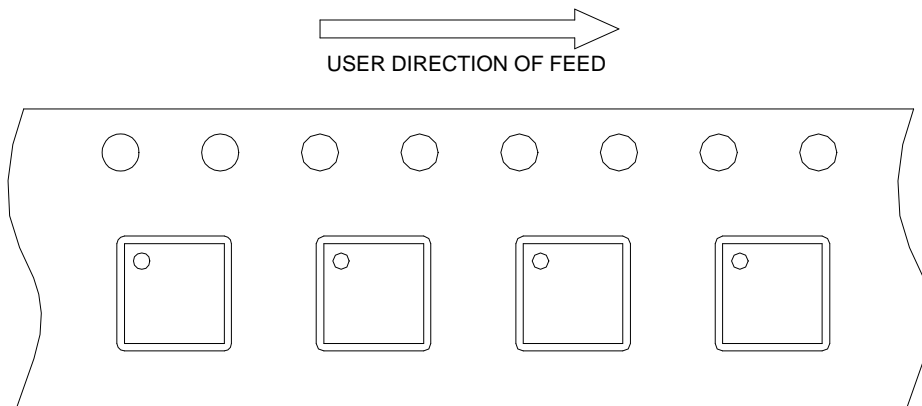


Taping Direction Information (Cont.)

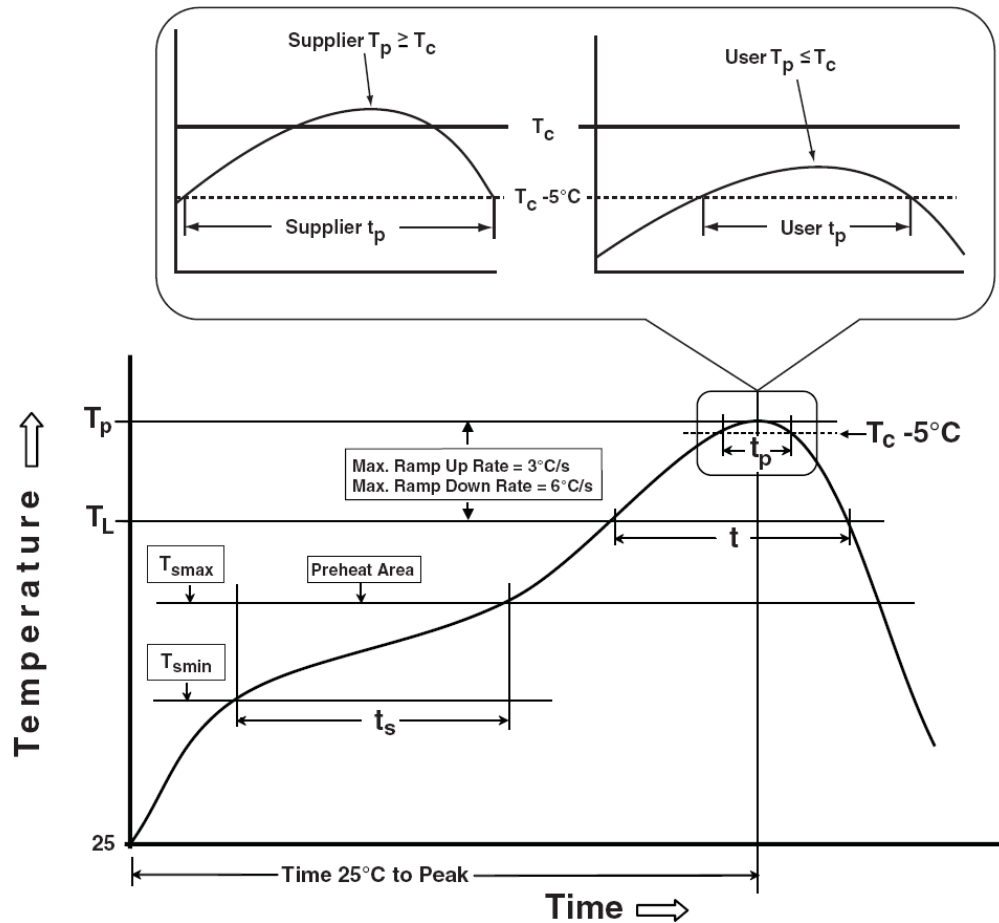
SOP-18



QFN4x4-20A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_l)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T _j =125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

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