Stereo Digital Class-D Amplifier

Features

- **Operating Voltage: 8V-20V for PVDD and AVDD - 3.0V~3.6V for DVDD**
- **High Efficiency Class-D Operation Eliminate the Need of Heatsinks**
- **Digital Serial Audio Input (Stereo Output)**
- **I²C Control Interface**
- **Sampling Rate can Support from 32kHz to 192kHz**
- **Separated Volume Control from 24dB to Mute**
- **Soft Mute (50% Duty Cycle)**
- **Programmable Dynamic Range Compression**
  - **– Power Limiter**
  - **– Speaker Protection**
- **Shutdown and Mute Function**
- **Soft Start and Soft Mute**
- **Slew Rate limiter**
- **Thermal and Over-Current Protections with Auto Recovery**
- **Space Saving Package QFN4x4-28A and TSSOP-28P**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD TV**

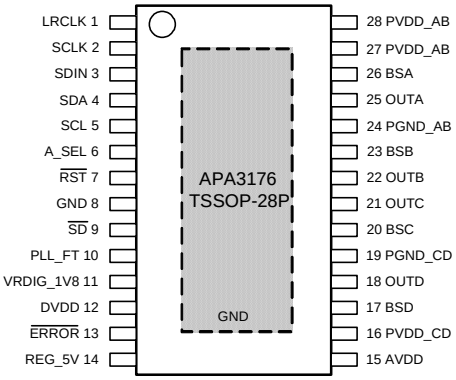
General Description

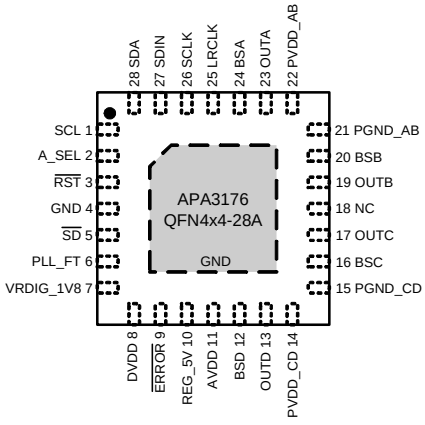
The APA3176 is a digital input, stereo, high efficiency, Class-D audio amplifier and is available in QFN4x4-28A and TSSOP-28P pins packages.

The APA3176 accepts the digital serial audio data and using the digital audio processor to convert the audio data becomes the stereo Class-D output speaker amplifier. This provides the seamless integration between the codec and the speaker amplifier.

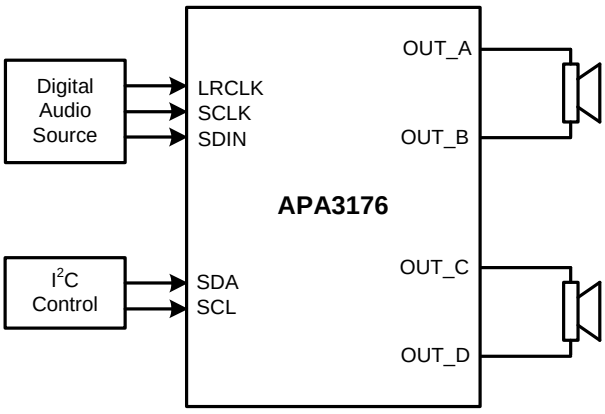
The APA3176 is a slave device receiving clocks from external source, and the Class-D's PWM switching frequency is 352.8kHz for the sampling rate 44.1kHz or 384 kHz for sampling 48kHz, depend on the input signal's sampling rate.

Pin Configuration





Simplified Application Circuit



Ordering and Marking Information

APA3176 □□-□□□ Assembly Material Handling Code Temperature Range Package Code		Package Code R: TSSOP-28P QA: QFN4x4-28A Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3176 R:		XXXXX - Date Code
APA3176 QA:		XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{PVDD}	Supply voltage (PVDD_X to PGND_XX)		-0.3 to 24	V
V_{AVDD}	Supply voltage (AVDD to AVSS)		-0.3 to 24	
V_{DVDD}	Supply voltage (DVDD to DVSS)		-0.3 to 3.6	
	Input Voltage (AVSS, DVSS, AGND to PGND_XX)		-0.3 to 0.3	
V_{OUTX}	Output Voltage (OUT_X to PGND_XX)	<400ns pulse width	-2 to 26	
		>400ns pulse width	-0.3 to 24	
V_{BSX}	Output Voltage (BS_X to OUT_X)		-0.3 to 6	
V_{BSX}	Output Voltage (BS_X to PGND_XX)	<400ns pulse width	-2 to 30	
		>400ns pulse width	-0.3 to 25	
Input Voltage	/SD,/RST, LRCLK, SCLK, SDIN, SDA, SCL to DVSS		-0.3 to DVDD+2.5	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
T_{SDR}	Soldering Temperature Range, 10 seconds		260	°C
P_D	Power Dissipation		Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note2)		°C/W
	TSSOP-28P	45	
	QFN4x4-28A	50	
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3)		°C/W
	TSSOP-28P	8	
	QFN4x4-28A	7	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of QFN4x4-28A and TSSOP-28P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the QFN4x4-28A and TSSOP-28P package.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{PVDD}	Supply voltage (PVDD to PGND)		8	20	V
V_{AVDD}	Supply voltage (AVDD to AGND)		8	20	V
V_{DVDD}	Supply voltage (DVDD to DGND)		3	3.6	V
V_{IH}	High Level Threshold	/SD, /RST, A_SEL,LRCLK, SCLK, SDIN, SDA, SCL to AGND	1.6	3.6	V
V_{IL}	Low Level Threshold	/SD, /RST, A_SEL,LRCLK, SCLK, SDIN, SDA, SCL to AGND	0	0.8	V
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	°C
R_L	Speaker Resistance	PVDD>15V	5	16	Ω
		PVDD≦15V	3.2	16	
L_O	Output Low Pass Filter Inductance		10	47	µH
	Minimum output inductance under short-circuit condition, Rated Current Based on 6A		10	-	

PWM Operating Conditions

Symbol	Parameter	Test Conditions	Value	Unit
f_S	Output Sample Rate	32 kHz Data Rate ±2%	256	kHz
		44.1k/88.2k/176.4 kHz Data Rate ±2%	352.8	
		48k/96k/192 kHz Data Rate ±2%	384	

PLL Input Parameters and External Filter Components

Symbol	Parameter	Test Conditions	APA3176			Unit
			Min.	Typ.	Max.	
	External PLL Filter Capacitor C1	SMD 0603 Y5V	-	47	-	nF
	External PLL Filter Capacitor C2	SMD 0603 Y5V	-	4.7	-	
	External PLL Filter Resistor R		-	470	-	Ω

Electrical Characteristics

DC CHARACTERISTICS

T_A=25°C, PV_{DD}=AV_{DD}=16V, DV_{DD}=3.3V, R_L=8Ω, BTL BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3176			Unit
			Min	Typ	Max	
I_{DD}	3.3V Supply Current (DVDD)	Normal Mode (No load),3.3V	-	10	20	mA
I_{PVDD}	Full Bridge Stage Supply Current	Normal Mode (No load),16V	-	18	35	mA
I_{SD}	PVDD	16V,T_A=-40~85°C	-	-	100	μA
	DVDD	3.3V,T_A=-40~85 °C,only /SD=GND, others NC	-	-	1.5	mA
I_I	Input Current	/SD,/RST=GND,PH=200k,	13	-	25	μA
		A_SEL =3.3V,PL=200k,	13	-	25	μA
		SCL,SDA,SDIN,SCLK,LRCLK=GND ,PH=20k	130	-	250	μA
V_{RDIG_1V8}	VRDIG_1V8 Voltage		1.6	1.8	2	V
V_{REG_5V}	REG_5V Voltage		4.5	5	5.5	V
$R_{DS(ON)}$	Drain to source resistance,LS	T_A=25 °C, includes metallization resistance	-	180	200	mΩ
	Drain to source resistance,HS	T_A=25 °C, includes metallization resistance	-	180	200	
OCP	Over Current Tripping Point		-	5	-	A
OVP	Overvoltage Trip Level	rising	21	22	23	V
	Hysteresis		-	1.5	-	V
UVP	Under Voltage Detection	UVP=1111	14.5	15	15.5	V
	UVP_Release	UVP=1111	14.8	15.5	15.8	V
OTW	Thermal Warning Threshold		-	120	-	°C
	Thermal Warning Threshold Hysteresis		-	25	-	
OTP	Thermal Protection Threshold		-	160	-	°C
	Thermal Protection Threshold Hysteresis		-	25	-	
η	Efficiency	PVDD=12V,RL=8Ω,PO=7W	85	88	-	%
R_{OUT}	Internal pull-down resistance at each OUT_X		-	3	-	kΩ
R_ERROR	ERROR pull-low resistance		1.5	-	3	kΩ
I_ERROR	ERROR Leakage Current	VERROR=3.3V	-	-	1	μA

Electrical Characteristics (Cont.)

AC CHARACTERISTICS

T_A=25°C, PV_{DD}=AV_{DD}=16V, DV_{DD}=3.3V, R_L=8Ω, BTL BD Mode, f_S=48kHz (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA3176			Unit
				Min	Typ	Max	
P_O	Output Power	BTL,THD+N=1%,fin=1kHz, RL=8Ω	PVDD=16V	-	13.5	-	W
			PVDD=12V	-	7.5	-	
		BTL,THD+N=1%,fin=1kHz, RL=4Ω	PVDD=8V	-	6.2	-	
			PVDD=12V	-	13.6	-	
		BTL,THD+N=10%,fin=1kHz, RL=8Ω	PVDD=16V	-	16.5	-	
			PVDD=12V	-	9.3	-	
		BTL,THD+N=10%,fin=1kHz, RL=4Ω	PVDD=8V	-	7.7	-	
			PVDD=12V	-	17	-	
THD+N	Total Harmonic Distortion Plus Noise	fin=1kHz,RL=8Ω,PO=1W	PVDD=8V	-	0.04	-	%
			PVDD=16V	-	0.03	-	
Crosstalk	Channel Separation	P_O=0.25W, RL=8Ω, fin=1kHz		-	82	-	dB
V_n	Noise Output Voltage	With A-Weighting Filter (AV=0dB),PVDD=12V		-	30	-	μV
SNR	Signal to Noise Ratio	Maximum output at THD+N<1%, With A-Weighting Filter (AV=0dB)		-	105	-	dB
PSRR		fin=1kHz,Ripple=200mV_{PP}		-	-70	-	dB
Att_{Mute}	Mute Attenuation	fin=1kHz, RL=8Ω, V_O=1Vrms		-	-70	-	dB
$Att_{Shutdown}$	Shutdown Attenuation	fin=1kHz, RL=8Ω, V_O=1Vrms		-	-110	-	dB
DR	Dynamic Range			-	-90	-	dB

Serial Audio Ports Slave Mode

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA3176			Unit
			Min.	Typ.	Max.	
f_{SCLK}	Frequency, SCLK 32xf_S, 48xf_S, 64xf_S	C_L=30pF	1.024	-	12.288	MHz
f_{Setup1}	Setup Time, LRCLK to SCLK Rising Edge		10	-	-	ns
f_{Hold1}	Hold Time, LRCLK to SCLK Rising Edge		10	-	-	
f_{Setup2}	Setup Time, SDIN to SCLK Rising Edge		10	-	-	
f_{Hold2}	Hold Time, SDIN to SCLK Rising Edge		10	-	-	
	LRCLK Frequency		32	48	192	kHz
	LRCLK Duty Cycle		40	50	60	%
	SCLK Duty Cycle		40	50	60	
	SCLK Rising Edges Between LRCLK Riding Edges		32	-	64	SCLK edges
$t_{(edge)}$	LRCLK Clock Edge With Respect To The Falling Edge of SCLK		-1/4	-	1/4	SCLK period
tr/tf (SCLK/LRCLK)	Rise/Fall Time for SCLK/LRCLK		-	-	8	ns

Reset Timing

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to “Recommended Use Model” section on usage of all terminals.

Symbol	Parameter	Test Conditions	APA3176			Unit
			Min.	Typ.	Max.	
$t_{p(/RST)}$	Pulse Duration, RESET Active.	No Load	100	-	-	µs
$t_{d(I2C\_Ready)}$	Time to Enable I^2C		-	-	13.5	ms

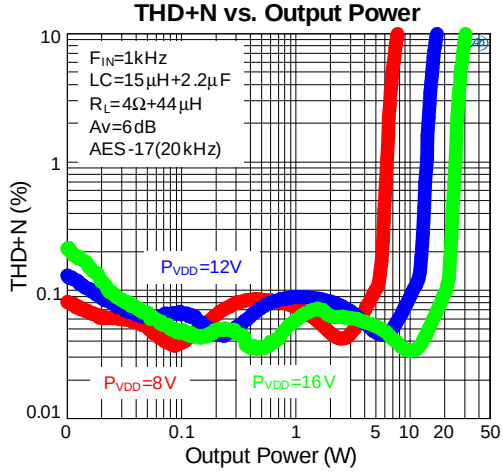
I²C Serial Control Port Operation

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

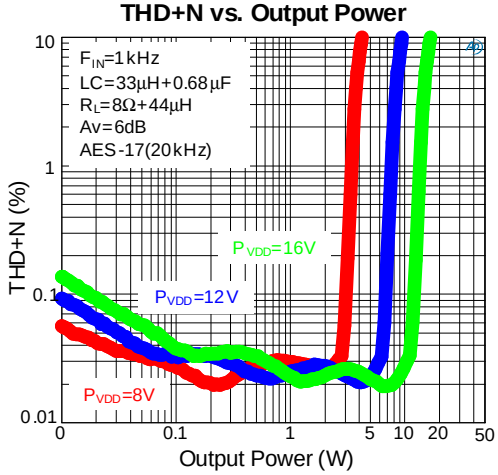
Symbol	Parameter	Test Conditions	APA3176			Unit
			Min.	Typ.	Max.	
f_{SCL}	Frequency, SCL	No Wait States	-	-	400	kHz
$t_{W(H)}$	Pulse Duration, SCL High		0.6	-	-	µs
$t_{W(L)}$	Pulse Duration, SCL Low		1.3	-	-	
t_r	Rise Time, SCL and SDA		-	-	300	ns
tf	Fall Time, SCL and SDA		-	-	300	ns
t_{setup1}	Setup Time, SCL to SDA		100	-	-	ns
t_{hold1}	Hold Time, SCL to SDA		100	-	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition		1.3	-	-	µs
t_{setup2}	Setup Time, SCL to Start Condition		0.6	-	-	
t_{hold2}	Hold Time, Start condition to SCL		0.6	-	-	
t_{setup3}	Setup Time, SCL to Stop Condition		0.6	-	-	
C_L	Load Capacitance for Each Bus Line		-	-	400	pF

Typical Operating Characteristics

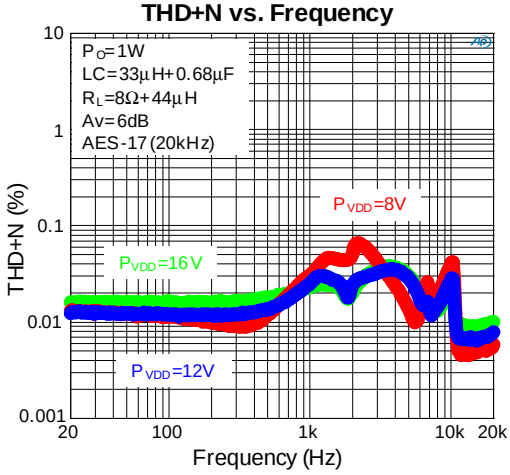
THD+N vs. Output Power



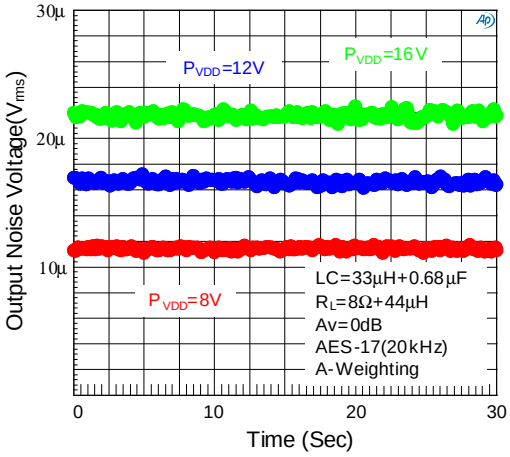
THD+N vs. Output Power



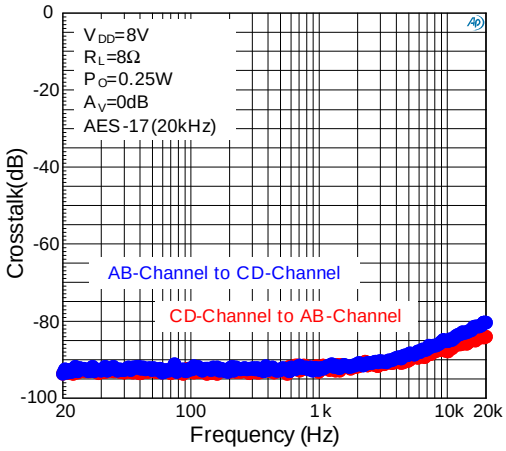
THD+N vs. Frequency



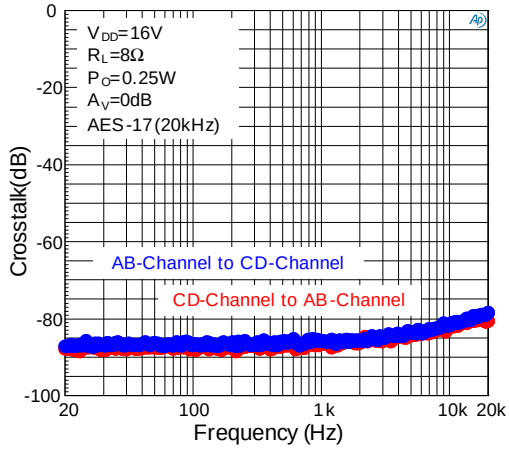
Output Noise Voltage vs. Time



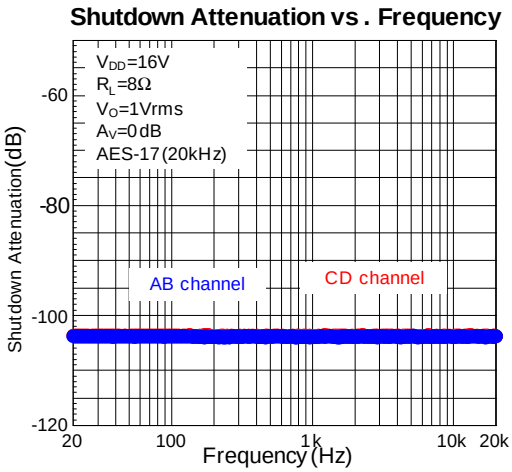
Crosstalk vs. Frequency

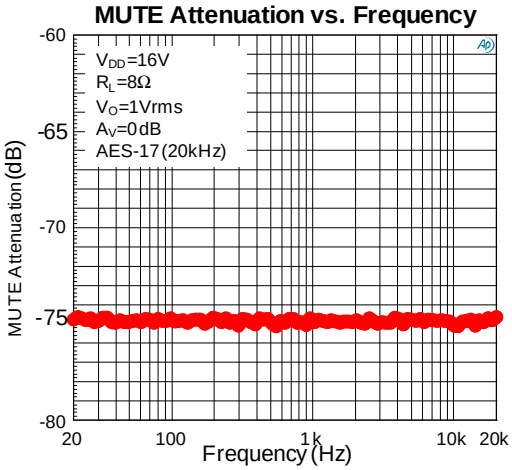


Crosstalk vs. Frequency

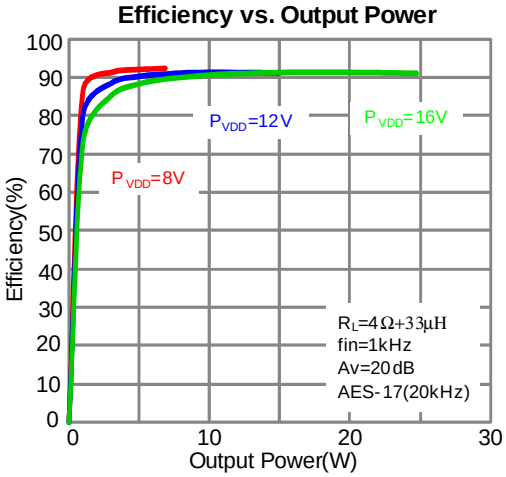


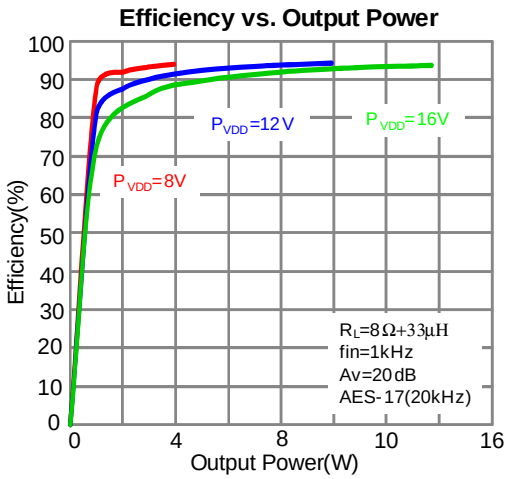
Typical Operating Characteristics (Cont.)





Typical Operating Characteristics (Cont.)

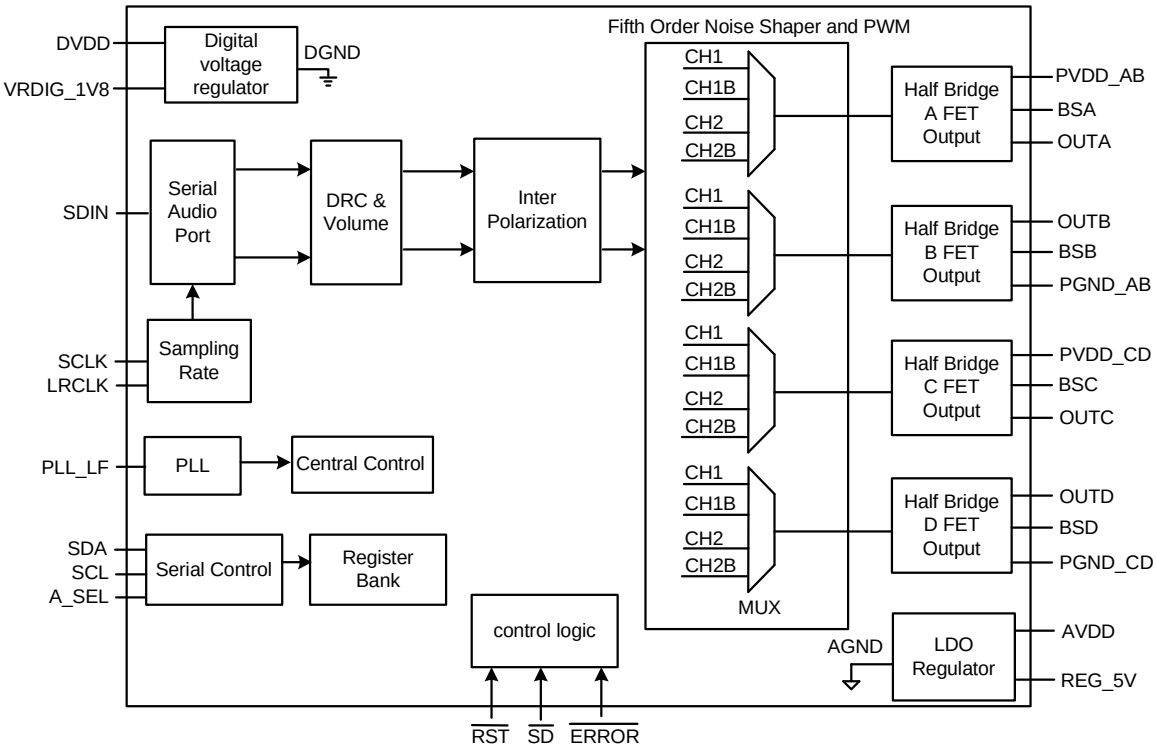




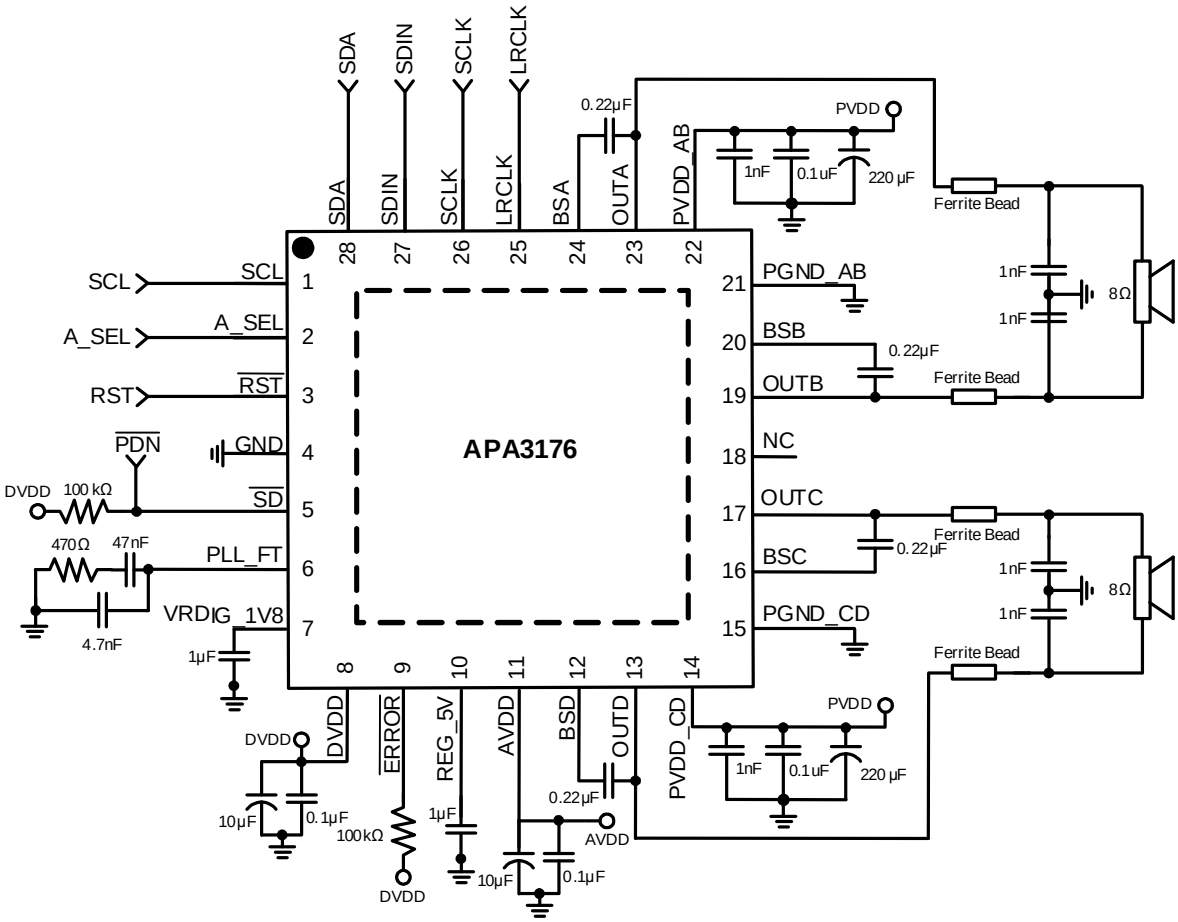
Pin Description

PIN		NAME	I/O/P	FUNCTION
No.				
QFN4x4-28A	TSSOP-28P			
1	5	SCL	I	I2C serial control clock input.
2	6	A_SEL	I/O	Input: device address setting
3	7	/RST	I	Reset control, place a logic low to this pin, will reset the APA3176 to its default condition. It's weak pull-up terminal.
4	8	GND	P	analog ground.
5	9	/SD	I	Shutdown logic input for audio amp (Low=outputs disabled, High=output enabled).
6	10	PLL_FT	O	PLL negative loop filter pin.
7	11	VRDIG_1V8	O/P	Internal regulated 1.8V for digital block's supply, Not for power external device.
8	12	DVDD	P	Digital power supply and connects to 3.3V.
9	13	/ERROR	O	When over temperature (OTW/OTP), over current over voltage and under voltage occur, this pin will be pull low; and it will be reset to high when the fault condition has be remove.
10	14	REG_5V	O/P	Nominal voltage is 5V, only for internal used.
11	15	AVDD	P	Analog power supply.
12	17	BSD	I/O	High side bootstrap supply for half bridge D.
13	18	OUTD	O	Output of half bridge D.
14	16	PVDD_CD	P	Power supply for half bridge CD.
15	19	PGND_CD	P	Power stage's analog ground.
16	20	BSC	I/O	High side bootstrap supply for half bridge C.
17	21	OUTC	O	Output of half bridge C.
18	-	NC	-	Not connected.
19	22	OUTB	O	Output of half bridge B.
20	23	BSB	I/O	High side bootstrap supply for half bridge B.
21	24	PGND_AB	P	Power stage's analog ground.
22	27,28	PVDD_AB	P	Power supply for half bridge AB.
23	25	OUTA	O	Output of half bridge A.
24	26	BSA	I/O	High side bootstrap supply for half bridge A.
25	1	LRCLK	I	Input serial audio data left/right clock. (Sample rate clock), it's weak pull down terminal.
26	2	SCLK	I	Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
27	3	SDIN	I	Serial audio data input.
28	4	SDA	I	I2C serial control data interface input/output.
Exposed Pad	Exposed Pad	GND	P	Ground pin of the circuitry. Connect the exposed pad to the system ground plan with large copper area for dissipating heat into the ambient air.

Block Diagram



Typical Application Circuit



Function Description

Clock And PLL

The APA3176 is a slave device and receives signals from SCLK, and LRCLK. The digital audio processor(DAP) provides all sample rates.The APA3176 checks to verify that SCLK is a particular value of $32f_S$, $48f_S$, or $64f_S$. The DAP only provides a $1xf_S$ LRCLK.The timing relationship of these clocks to SDIN is shown in subsequent sections.

Serial Data Interface

Serial data is an input transmitted to SDIN. The PWM outputs are derived from SDIN. Besides, the APA3176 DAP receives left-justified, right-justified, and I2S serial data formats with 16, 20, or 24 bit.

PWM Section

The APA3176 DAP device uses noise-shaping to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts PCM data from the DAP and outputs two BTL PWM audio output channels.
The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters are included and can be enabled and disabled. The PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

I²C Compatible Serial Control Interface

The APA3176 DAP receives commands from a system controller through an I2C serial control slave interface. The serial control interface supports both normal-speed 100kHz and high-speed 400kHz operations without waiting states. For status registers, the serial control interface provides both single-byte and multi-byte read and write operations; and for the general control registers, they associated with the PWM.

Function Description (Cont.)

Serial Interface Control And Timing

I²S Timing

I²S timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is low; for the right channel, the LRCLK is high. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. When the LRCLK signal changes state, there is a delay of one bit clock from the time which the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

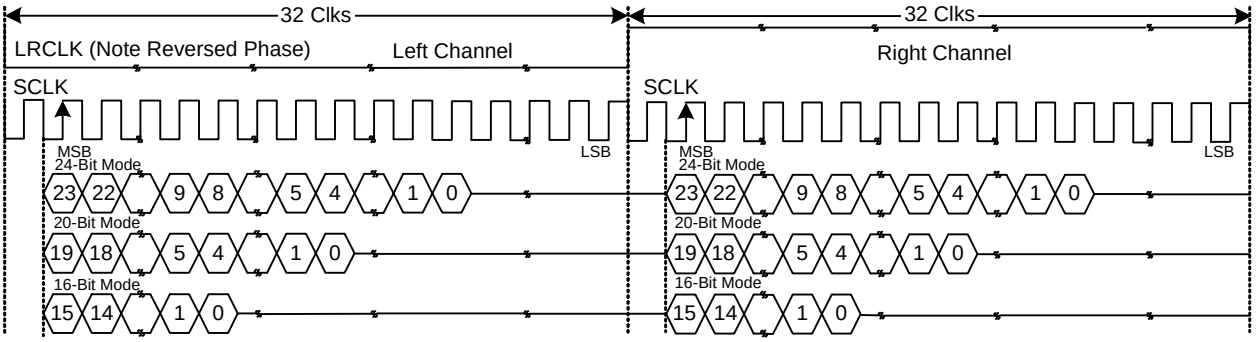


Figure 1. I²S 64 f_S Format

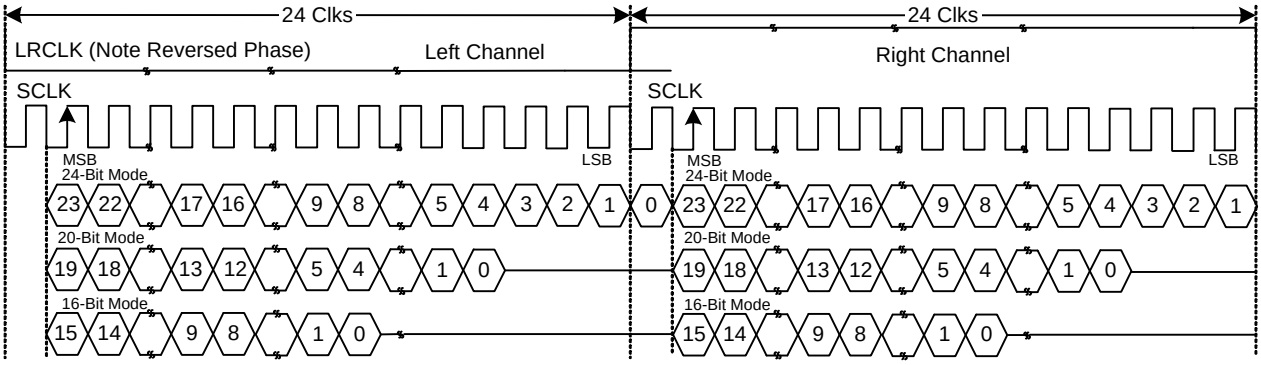


Figure 2. I²S 48 f_S Format

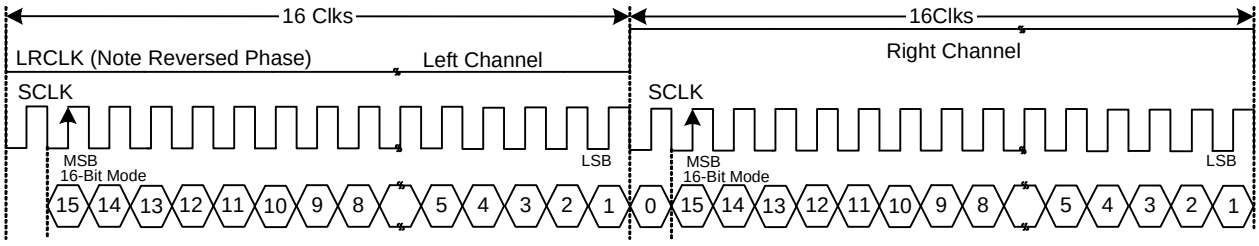


Figure 3. I²S 32 f_S Format

Function Description (Cont.)

Left-Justified

Left-justified (LJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK is low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines when LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

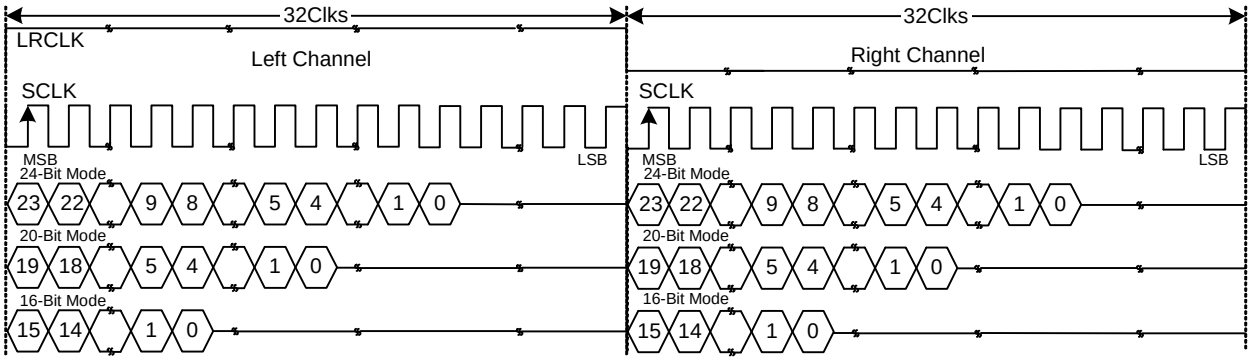


Figure 4. Left-Justified 64 f_S Format

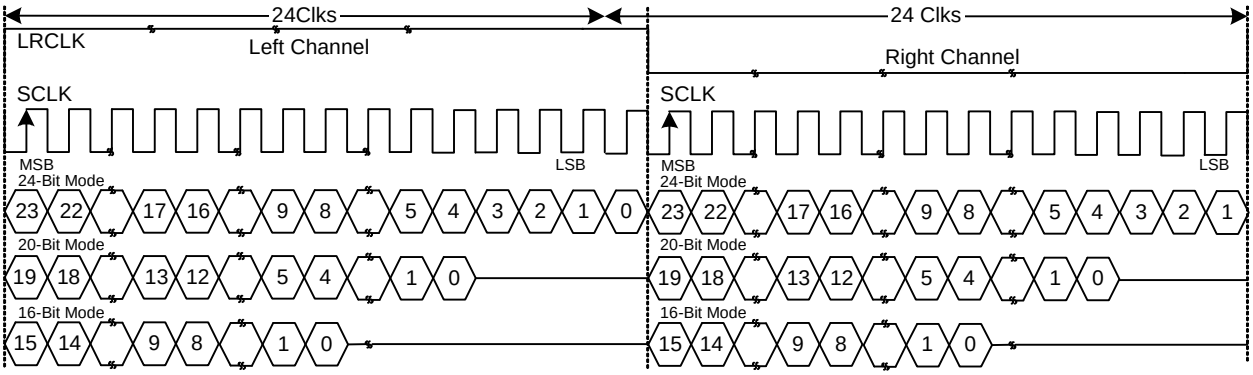


Figure 5. Left-Justified 48 f_S Format

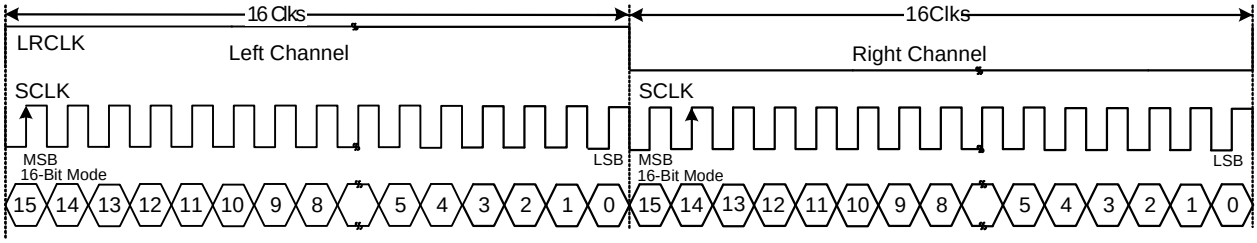


Figure 6. Left-Justified 32 f_S Format

Function Description (Cont.)

Right-Justified

Right-justified (RJ) timing uses LRCLK to define the data for the left channel and the right channel when the data being transmitted. For the left channel, the LRCLK is high; for the right channel, the LRCLK low. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. After LRCLK toggles, for 24bit data, the first bit of data appears on the data 8 bit-clock. In RJ mode, the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

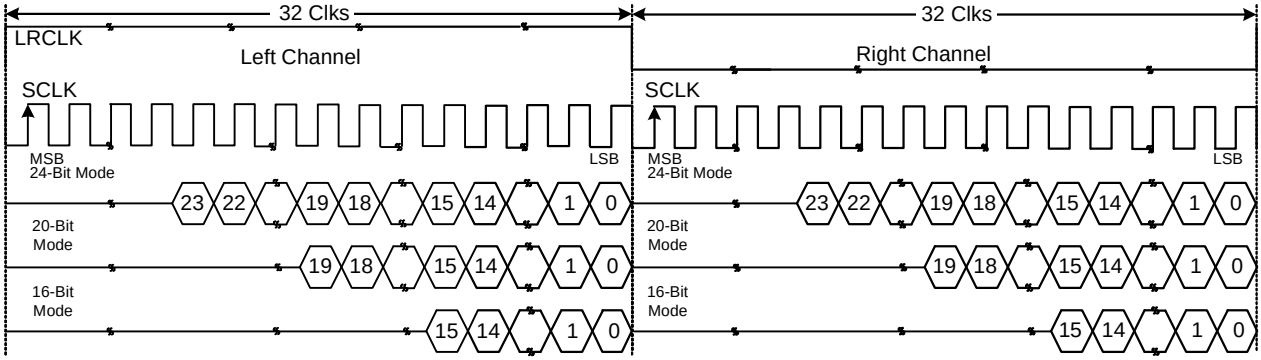


Figure 7. Right-Justified 64 f_S Format

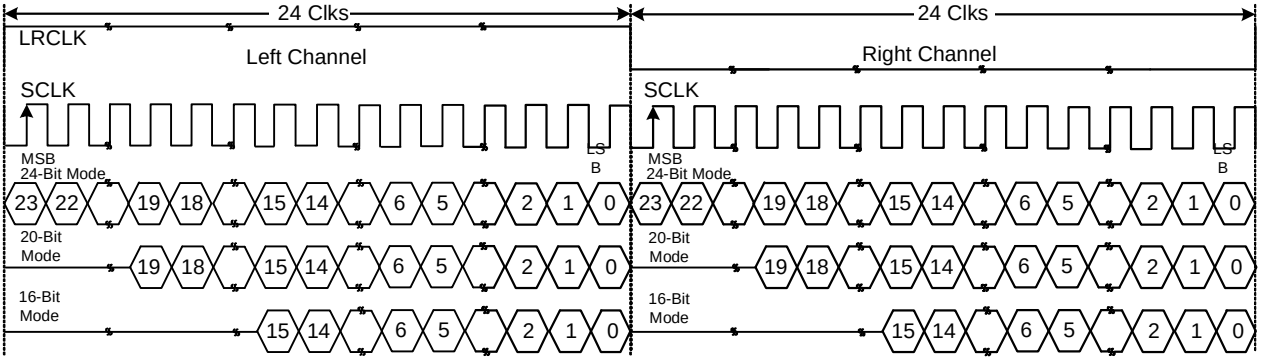


Figure 8. Right-Justified 48 f_S Format

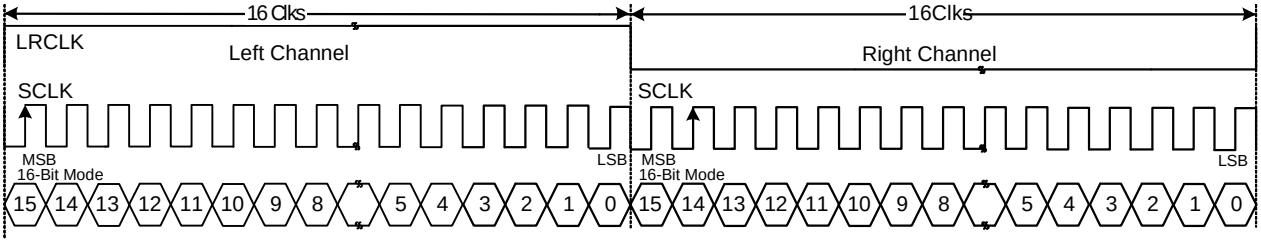


Figure 9. Right-Justified 32 f_S Format

Function Description (Cont.)

I²C Serial Control Interface

The APA3176 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol. Besides, it provides both 100kHz and 400kHz data transfer rates to single and multiple bytes write and read operations. This is a slave only device, and it doesn't support a multi-master bus environment or wait state insertion. The function of the control interface is to read device status and to program the registers of the device. The DAP supports the standard-mode I²C bus operation (100kHz maximum) and the fast I²C bus operation (400kHz maximum). Without I²C wait cycles, the DAP performs I²C operations.

General I²C Operation

The I²C bus uses SDA (data) and SCL (clock) to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. With the most significant bit (MSB) transferred first, the address and data can be transferred in byte (8bit) format. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the SDA when the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock. These conditions are shown in Figure 10. The master generates the 7bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The APA3176 holds SDA low during the acknowledge clock to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

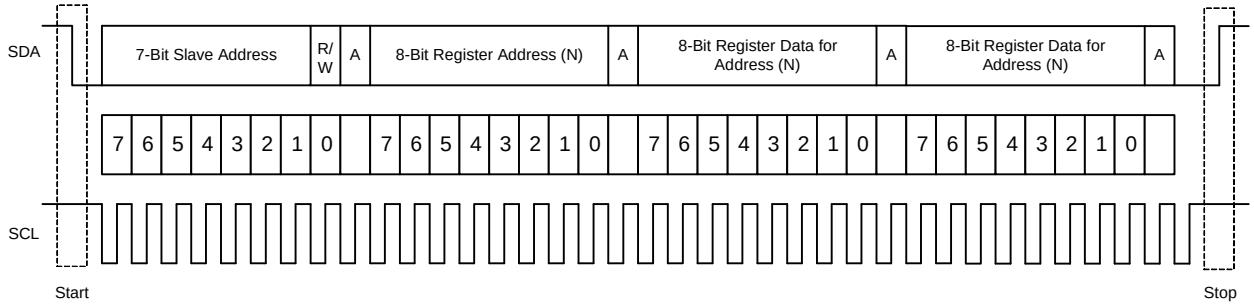


Figure 10. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 10.

Pin A_SEL defines the I²C device address. An external 15kΩ pulldown on this pin gives a device address of 0x34 and a 15kΩ pullup gives a device address of 0x36. The 7-bit address is 0011 010 (0x34) or 0011 011 (0x36).

Function Description (Cont.)

Single- and Multiple-Byte Transfers

The serial control interface supports single-byte and multiple-byte (R/W) operations for sub-addresses 0x00 to 0x1F. During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the sub-address assigned, as long as the master device continues to respond with acknowledges. If a particular sub-address does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific sub-address.

Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APA3176 also supports sequential I²C addressing. For write transactions, if a sub-address is issued and followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APA3176. For I²C sequential write transactions, the sub-addresses then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last sub-address is discarded. However, if all other data written is accepted, only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 11, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. The R/W bit determines the direction of the data transfer. For a write data transfer, the R/W bit will be a 0. After receiving the correct I²C device address and the R/W bit, the DAP responds with an acknowledge bit. And then, the master transmits the address byte or bytes corresponding to the APA3176 internal memory address being accessed. After receiving the address byte, the APA3176 responds with an acknowledge bit again. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APA3176 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

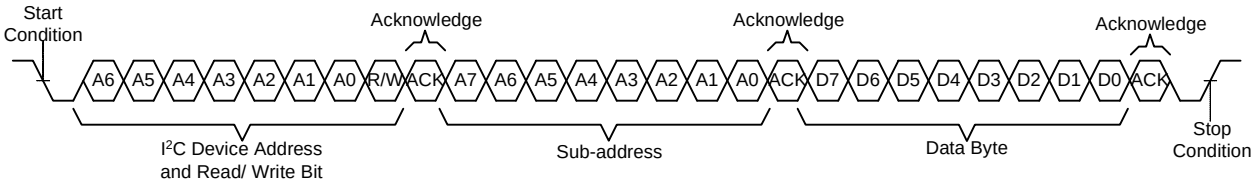


Figure 11. Single-Byte Write Transfer

Function Description (Cont.)

Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 12. After receiving each data byte, the APA3176 responds with an acknowledge bit.

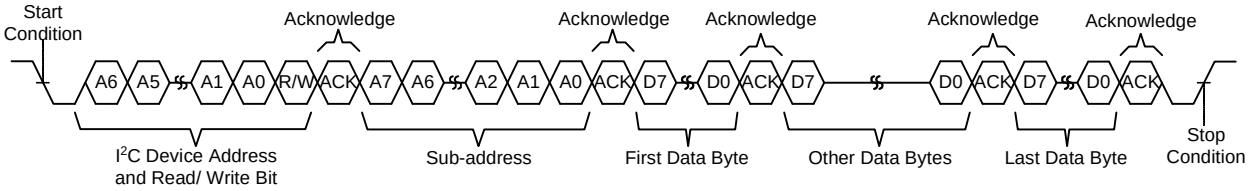


Figure 12. Multiple-Byte Write Transfer

Single-Byte Read

As shown in Figure 13, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the APA3176 address and the read/write bit, APA3176 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APA3176 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the APA3176 again responds with an acknowledge bit. Next, the APA3176 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

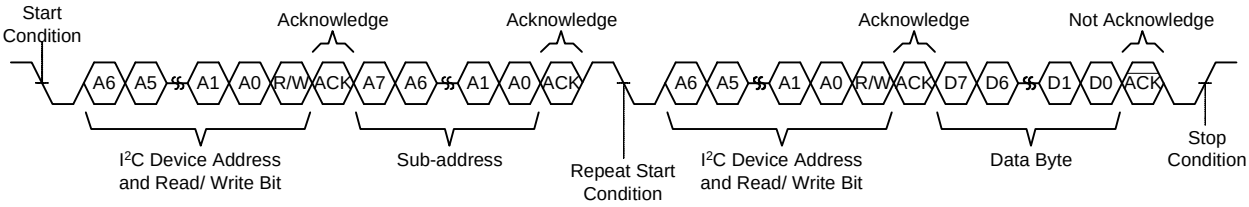


Figure 13. Single-Byte Read Transfer

Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the APA3176 to the master device as shown in Figure 14. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

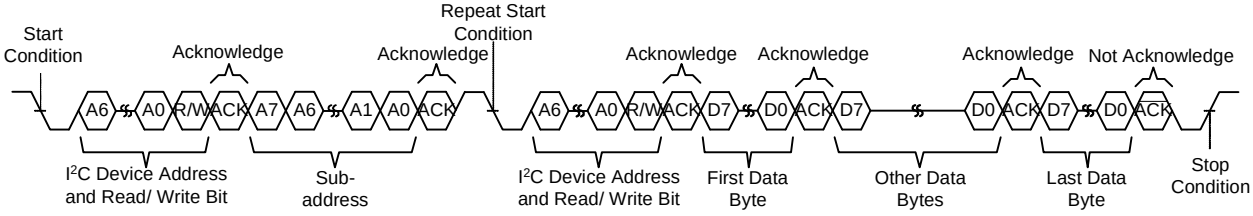


Figure 14. Multiple-Byte Read Transfer

Function Description (Cont.)

Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/ right channels.

The DRC input/output diagram is shown in Figure 15.

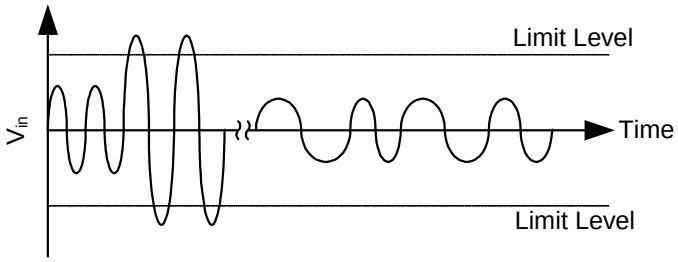


Figure 15. Dynamic Range Control

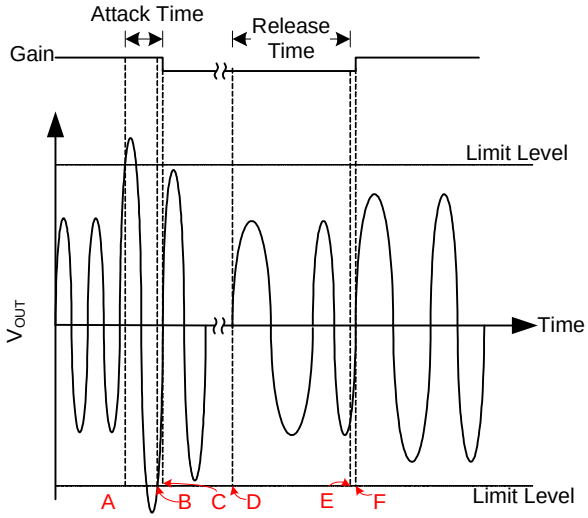


Figure 16. DRC Structure

Function Description (Cont.)

26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 17 .

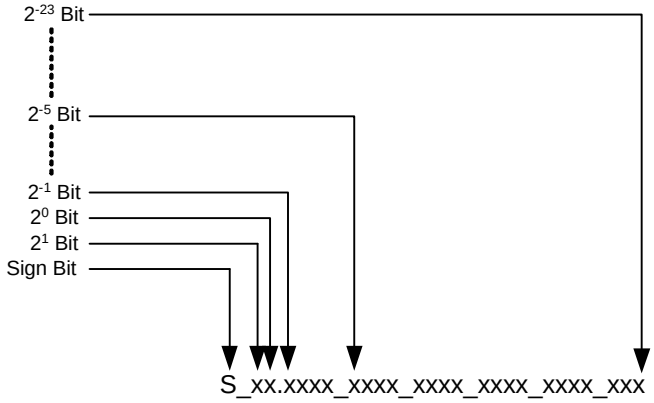


Figure 17. 3.23 Format

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 17. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 18 applied to obtain the magnitude of the negative number.

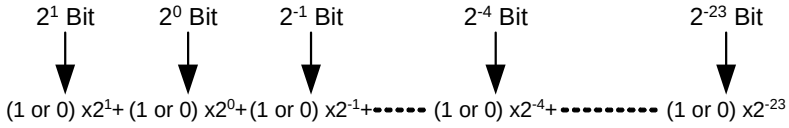


Figure 18. Conversion Weighting Facroes-3.23 Format to Floating Point

Gain coefficients, entered via the I²C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 19.

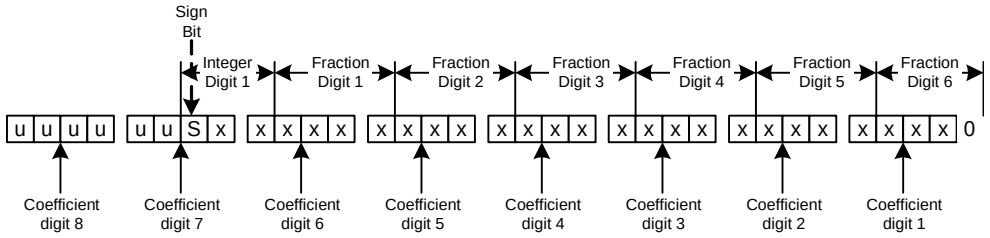


Figure 19. Alignment of 3.23 Coefficient in 32Bit I2C Word

Function Description (Cont.)

Sample calculation for 3.23 format

dB	Linear	Decimal	Hex(3.23 Format)
0	1	8388608	00800000
5	1.7782794	14917288	00E39EA8
-5	0.5623413	4717260	0047FACC
X	L = 10(X/20)	D = 8388608 × L	H = dec2hex (D, 8)

Sample calculation for 9.17 format

dB	Linear	Decimal	Hex(9.17 Format)
0	1	131072	00020000
5	1.7782794	233082.6	00038E7A
-5	0.5623413	73707.2	00011FEB
X	L = 10(X/20)	D = 131072 × L	H = dec2hex (D, 8)

Recommended Use Model

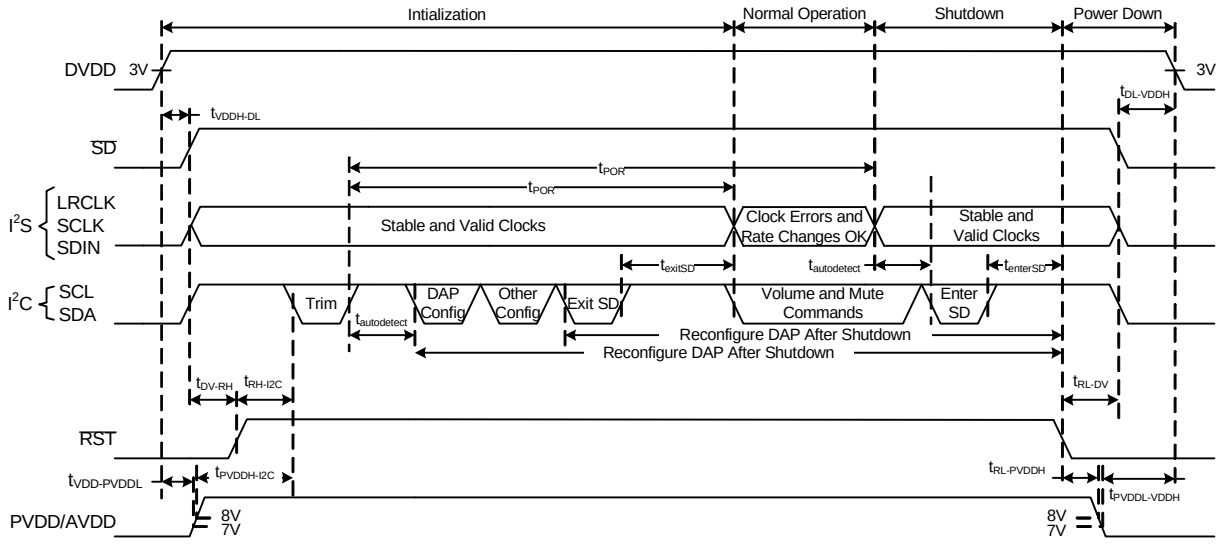


Figure 20. Recommended Command Sequence

Function Description (Cont.)

Parameter	Description	APA3176			Unit
		Min.	Typ.	Max.	
$t_{VDDH-DL}$	Time digital inputs must remain low after DVDD goes above 3V	0	-	-	µs
$t_{DL-VDDH}$	Time digital inputs must be low before DVDD goes below 3V	0	-	-	
$t_{VDD-PVDDL}$	Time PVDD/AVDD remains below 7.5V after DVDD goes above 3V	100	-	-	
$t_{PVDDL-VDDH}$	Time PVDD/AVDD must be below 7.5V before DVDD goes below 3V	0	-	-	
$t_{PVDDH-I2C}$	Time PVDD/AVDD must be above 10V before I²C commands may address device	10	-	-	
$t_{RL-PVDDH}$	Time PVDD/AVDD must remain above 10V after /RST goes low	2	-	-	
t_{RH-I2C}	Time RESET must be high before I²C commands may address device	13.5	-	-	ms
t_{DV-RH}	Time digital inputs must be valid (driven as recommended) before /RST goes high	100	-	-	µs
t_{RL-DV}	Time digital inputs must remain valid (driven as recommended) after /RST goes low	2	-	-	
$t_{autodetect}$	Auto-detect completion wait time (given stable and valid clocks) before issuing further commands	50	-	-	ms
t_{exitSD}	Exit shutdown wait time before issuing further commands to device (t start given by register 0x1A)	1+1.3 x tstart	-	-	
$t_{enterSD}$	Enter shutdown wait time before issuing further commands to device (t stop given by register 0x1A)	1+1.3 x tstop	-	-	
t_{POR}	Power-on-reset wait time after 1st trim following DVDD power-up (tstart given by register 0x1A) (does not apply to trim commands following subsequent resets)	240 + 1.3 x tstart	-	-	
t_{RL-DV}	Time digital inputs must remain valid (driven as recommended) after /RST goes low	2	-	-	µs
$t_{DL-VDDH}$	Time digital inputs must be low before DVDD goes below 3V	0	-	-	
$t_{RL-PVDDH}$	Time PVDD/AVDD must remain above 10V after /RST goes low	2	-	-	
$t_{PVDDL-VDDH}$	Time PVDD/AVDD must be below 7.5V before DVDD goes below 3V	0	-	-	

Recommended Use Model

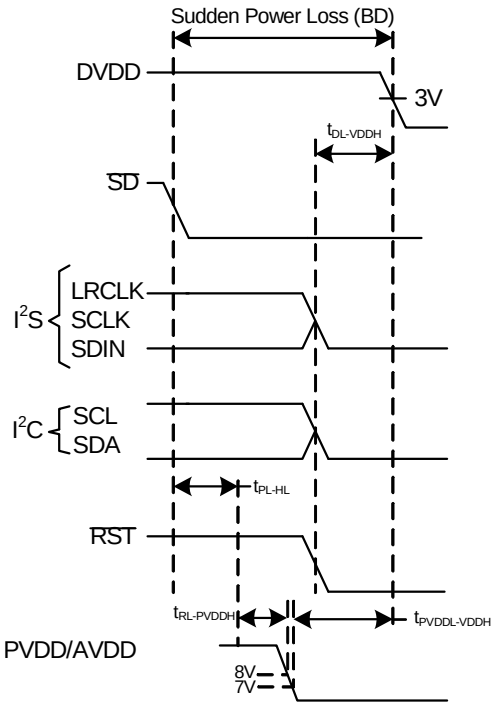


Figure 21. Power Loss Sequence

Function Description (Cont.)

Recommended Use Model (Cont.)

Parameter	Description	APA3176			Unit
		Min.	Typ.	Max.	
t_{RL-DV}	Time digital inputs must remain valid (driven as recommended) after /RST goes low	2	-	-	µs
$t_{DL-VDDH}$	Time digital inputs must be low before DVDD goes below 3V	0	-	-	
$t_{RL-PVDDH}$	Time PVDD/AVDD must remain above 10V after /RST goes low	2	-	-	
$t_{PVDDL-VDDH}$	Time PVDD/AVDD must be below 7.5V before DVDD goes below 3V	0	-	-	

Recommended Command Sequences

The DAP has two groups of commands. One set is for configuration and is intended for use only during initialization. The other set has built-in click and pop protection and may be used during normal operation while audio is streaming. The following supported command sequences illustrate how to initialize, operate, and shutdown the device.

Initialization Sequence

Use the following sequence to power-up and initialize the device:
1.Hold all digital inputs low and ramp up DVDD to at least 3V.
2.Initialize digital inputs and PVDD/AVDD supply as follows:

- Drive /RST=0, /SD=1, and other digital inputs to their desired state while ensuring that all are never more than 2.5V above DVDD. Provide stable and valid I2S clocks (LRCLK, and SCLK). Wait at least 100us, drive /RST=1, and wait at least another 13.5ms.
- Ramp up PVDD/AVDD to at least 7V while ensuring that it remains below 3.5V for at least 100us after /DVDD reaches 3V. Then wait at least another 10µs.

3.Configure the DAP via I^2C (see Users's Guide for typical values)
4.Configure remaining registers
5.Exit shutdown (sequence defined below).

Normal Operation

The following are the only events supported during normal operation:
(a) Writes to master/channel volume registers
(b) Writes to soft mute register
(c) Enter and exit shutdown (sequence defined below)
(d) Clock errors and rate changes
Note: Events (c) and (d) are not supported for 240ms+1.3xt0 0after trim following AVDD/DVDD power up ramp (where Tstart is specified by register 0x1A).

Function Description (Cont.)

Shutdown Sequence

Enter:

1. Ensure I^2S clocks have been stable and valid for at least 50ms.
2. Write 0x40 to register 0x05.
3. Wait at least 1ms+1.3xtstop (where tstop is specified by register 0x1A).
4. Once in shutdown, stable clocks are not required while device remains idle.
5. If desired, reconfigure by ensuring that clocks have been stable and valid for at least 50ms before returning to step 4 of initialization sequence.

Exit:

1. Ensure I2S clocks have been stable and valid for at least 50ms.
2. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240ms after trim following DVDD powerup ramp).
3. Wait at least 1ms+1.3xt_{start} (where tstart is specified by register 0x1A).
4. Proceed with normal operation.

Power-Down Sequence

Use the following sequence to power-down the device and its supplies:

1.If time permits, enter shutdown (sequence defined above); else, in case of sudden power loss, assert /SD=0 and wait at least 2ms.

2.Assert /RST=0.

3.Drive digital inputs low and ramp down PVDD/AVDD supply as follows:

- Drive all digital inputs low after /RST has been low for at least 2μs.
- Ramp down PVDD/AVDD while ensuring that it remains above 8V until /RST has been low for at least 2μs.

4.Ramp down DVDD while ensuring that it remains above 3V until PVDD/AVDD is below 7V and that it is never more than 2.5V below the digital inputs.

Function Description (Cont.)

Table 1. Serial Control Interface Register Summary

Sub Address	Register Name	No. of Bytes	Contents	Initialization Values
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x0C
0x01	Anpec ID register	1	Description shown in subsequent section	0x76
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0x80
0x04	Serial data interface	1	Description shown in subsequent section	0x05
0x05	System control register 2	1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	1	Description shown in subsequent section	0xFF
0x08	Channel 1 volume	1	Description shown in subsequent section	0x30
0x09	Channel 2 volume	1	Description shown in subsequent section	0x30
0x0A	Fine_vol Volume	1	Description shown in subsequent section	0x00
0x0E	Volume Slew configuration	1	Description shown in subsequent section	0x01
0x10	Modulation limit register	1	Description shown in subsequent section	0x00
0x1A	Start/stop period register	1	Description shown in subsequent section	0x0A
0x20	Input Mux	1	Description shown in subsequent section	0x89
0x25	PWM output MUX register	4	Description shown in subsequent section	0x0002 1300
0x45	Hard clipper	4	Description shown in subsequent section	0x017F_FFFF
0x46	DRC control	4	Description shown in subsequent section	0x0000_0000
0xE1	UVP	1	Description shown in subsequent section	0x00

Function Description (Cont.)

CLOCK CONTROL REGISTER (0x00)

The clocks and data rates are automatically determined by the APA3176. The clock control register contains the auto-detected clock status. Bits D3-D2 reflect the sample rate. Bits D1-D0 reflect the BCLK frequency. Bits D7-D4 reflect the reserved.

Table 2. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	-	-	-	-	Reserved
-	-	-	-	0	0	-	-	f_S=32-kHz sample rate
-	-	-	-	0	1	-	-	f_S=88.2/96-kHz sample rate
-	-	-	-	1	0	-	-	f_S=176.4/192-kHz sample rate
-	-	-	-	1	1	-	-	**f_S=44.1/48-kHz sample rate (2) (Default)**
-	-	-	-	-	-	0	0	**BCLK frequnecy=64*fs (2) (Default)**
-	-	-	-	-	-	0	1	BCLK frequnecy=48*fs
-	-	-	-	-	-	1	0	BCLK frequnecy=32*fs
-	-	-	-	-	-	1	1	BCLK frequnecy=64*fs (Reserved)

(1) Reserved registers should not be accessed.
(2) Default values are in bold.

DEVICE ID REGISTER (0x01)

The Anpec ID register contains the ID code for the firmware revision.

Table 3. Anpec ID Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**1**	**1**	**1**	**0**	**1**	**1**	**0**	Identification code

ERROR STATUS REGISTER (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.
Error Definitions:

- SCLK Error:The number of SCLKs per LRCLK is changing.
- LRCLK Error:LRCLK frequency is changing.

Table 4. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	-	-	-	-	-	-	OCP error
-	1	-	-	-	-	-	-	LRCLK error
-	-	1	-	-	-	-	-	SCLK error
-	-	-	1	-	-	-	-	OVP error
-	-	-	-	1	-	-	-	UVP error
-	-	-	-	-	1	-	-	OTP error (sets around 150℃)
-	-	-	-	-	-	1	-	PLL autolock error
-	-	-	-	-	-	-	1	OTW error
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors(Default)**

Default values are in bold.

Function Description (Cont.)

SYSTEM CONTROL REGISTER 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.

If 1, the dc-blocking filter (-3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D6-D0:Reserved

Table 5. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	-	-	-	-	-	-	PWM high-pass (dc blocking) disenabled
1	-	-	-	-	-	-	-	**PWM high-pass (dc blocking) enabled(Default)**
-	0	0	0	0	0	0	0	Reserved

Default values are in bold.

SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 6, the APA3176 supports 9 serial data modes. The default is 24-bit, I²S mode.

Table 6. Serial Data Interface Control Register (0x04) Format

D7	D6	D5	D4	D3	D2	D1	D0	WORD LENGTH	RECEIVE SERIAL DATA INTERFACE FORMAT
0	**0**	**0**	**0**	-	-	-	-		**Reserved(Default)**
-	-	-	-	0	0	0	0	16	Right-justified
-	-	-	-	0	0	0	1	20	Right-justified
-	-	-	-	0	0	1	0	24	Right-justified
-	-	-	-	0	0	1	1	16	I2S
-	-	-	-	0	1	0	0	20	I2S
-	-	-	-	**0**	**1**	**0**	**1**	**24**	**I2S(Default)**
-	-	-	-	0	1	1	0	16	Left-justified
-	-	-	-	0	1	1	1	20	Left-justified
-	-	-	-	1	0	0	0	24	Left-justified
-	-	-	-	1	0	0	1		Reserved
-	-	-	-	1	0	1	0		Reserved
-	-	-	-	1	0	1	1		Reserved
-	-	-	-	1	1	0	0		Reserved
-	-	-	-	1	1	0	1		Reserved
-	-	-	-	1	1	1	0		Reserved
-	-	-	-	1	1	1	1		Reserved

Default values are in bold.

Function Description (Cont.)

SYSTEM CONTROL REGISTER 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down(hard mute). Bits D7,D5-D0 reflect the reserved.

Table 7. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	-	0	0	0	0	0	0	Reserved
-	**1**	-	-	-	-	-	-	**Enter all channel shut down (hard mute) (Default)**
-	0	-	-	-	-	-	-	Exit all channel shut down (Normal operation)

Default values are in bold.

SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 8. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	-	-	**Reserved**
-	-	-	-	-	-	-	**0**	**Soft un-mute channel 1 (Default)**
-	-	-	-	-	-	-	1	Soft mute channel 1
-	-	-	-	-	-	**0**	-	**Soft un-mute channel 2 (Default)**
-	-	-	-	-	-	1	-	Soft mute channel 2

Default values are in bold.

VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A)

Step size is 0.5 dB.

Master volume -0x07 (default is mute)

Channel-1 volume -0x08 (default is 0 dB)

Channel-2 volume -0x09 (default is 0 dB)

Fine volume -0x0A (default is 0 dB)

Table 9. Volume Registers (0x07, 0x08, 0x09)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	24dB
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0dB(Default)**
1	1	1	1	1	1	1	0	-103dB
1	1	1	1	1	1	1	1	MUTE (default for master volume)

Default values are in bold.

Table 10. Volume Registers (0x0A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	-	-	**Reserved**
						0	**0**	**0dB(Default)**
						0	1	0.125dB
						1	0	0.25dB
						1	1	0.375dB

Default values are in bold.

Function Description (Cont.)

VOLUME CONFIGURATION REGISTER (0x0E)

Bits Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the D2-D0: number of steps in a volume ramp.Volume steps occur at a rate that depends on the sample rate of the I^2S data as follows

Sample Rate (KHz)	Approximate Ramp Rate
8/16/32	125 us/step
11.025/22.05/44.1	90.7 us/step
12/24/48	83.3 us/step

Table 11. Volume Control Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	-	-	-	**Reserved**
-	-	-	-	-	0	0	0	Volume slew 512 steps (43ms volume ramp time at 48kHz)
-	-	-	-	-	**0**	**0**	**1**	**Volume slew 1024 steps (85ms volume ramp time at 48kHz) (Default)**
-	-	-	-	-	0	1	0	Volume slew 2048 steps (171ms volume ramp time at 48kHz)
-	-	-	-	-	0	1	1	Volume slew 256 steps (21ms volume ramp time at 48kHz)
-	-	-	-	-	1	0	0	Volume slew 128 steps
-	-	-	-	-	1	0	1	Volume slew 64 steps
-	-	-	-	-	1	1	0	Reserved
-	-	-	-	-	1	1	1	Volume slew 0 steps (Disable)

Default values are in bold.

MODULATION LIMIT REGISTER (0x10)

The modulation limit is the maximum duty cycle of the PWM output waveform.

Table 12. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
0	**0**	**0**	**0**	**0**	-	-	-	**Reserved**
-	-	-	-	-	**0**	**0**	**0**	**99.2%(Default)**
-	-	-	-	-	0	0	1	98.4%
-	-	-	-	-	0	1	0	97.7%
-	-	-	-	-	0	1	1	96.9%
-	-	-	-	-	1	0	0	96.1%
-	-	-	-	-	1	0	1	95.3%
-	-	-	-	-	1	1	0	94.5%
-	-	-	-	-	1	1	1	93.8%

Default values are in bold.

Function Description (Cont.)

START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the /PDN state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I2S clock stability.

Table 13. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	-	-	-	-	-	**Reserved**
-	-	-	0	0	-	-	-	No 50% duty cycle start/stop period
-	-	-	0	1	0	0	0	16.5ms 50% duty cycle start/stop period
-	-	-	0	1	0	0	1	23.9ms 50% duty cycle start/stop period
-	-	-	**0**	**1**	**0**	**1**	**0**	**31.4ms 50% duty cycle start/stop period(Default)**
-	-	-	0	1	0	1	1	40.4ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	0	53.9ms 50% duty cycle start/stop period
-	-	-	0	1	1	0	1	70.3ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	0	94.2ms 50% duty cycle start/stop period
-	-	-	0	1	1	1	1	125.7ms 50% duty cycle start/stop period
-	-	-	1	0	0	0	0	164.6ms 50% duty cycle start/stop period
-	-	-	1	0	0	0	1	239.4ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	0	314.2ms 50% duty cycle start/stop period
-	-	-	1	0	0	1	1	403.9ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	0	538.6ms 50% duty cycle start/stop period
-	-	-	1	0	1	0	1	703.1ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	0	942.5ms 50% duty cycle start/stop period
-	-	-	1	0	1	1	1	1256.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	0	1728.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	0	1	2513.6ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	0	3299.1ms 50% duty cycle start/stop period
-	-	-	1	1	0	1	1	4241.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	0	5655.6ms 50% duty cycle start/stop period
-	-	-	1	1	1	0	1	7383.7ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	0	9897.3ms 50% duty cycle start/stop period
-	-	-	1	1	1	1	1	13196.4ms 50% duty cycle start/stop period

Default values are in bold.

Function Description (Cont.)

INPUT MULTIPLEXER REGISTER (0x20)

This register controls the routing of I2S audio to the internal channels.

Table 14. Input Multiplexer Register (0x20)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	-	-	-	-	-	-	-	**Channel-1 BD Mode(Default)**
-	**0**	**0**	**0**	-	-	-	-	**SDIN-L to channel 1(Default)**
-	0	0	1	-	-	-	-	SDIN-R to channel 1
-	0	1	0	-	-	-	-	(SDIN-L + SDIN-R)/2 to channel 1
-	0	1	1	-	-	-	-	(SDIN-L - SDIN-R) to channel 1
-	1	0	0	-	-	-	-	(SDIN-R - SDIN-L) to channel 1
-	1	0	1	-	-	-	-	Reserved
-	1	1	0	-	-	-	-	Ground (0) to channel 1
-	1	1	1	-	-	-	-	Reserved
-	-	-	-	**1**	-	-	-	**Channel-2 BD mode(Default)**
-	-	-	-	-	0	0	0	SDIN-L to channel 2
-	-	-	-	-	**0**	**0**	**1**	**SDIN-R to channel 2(Default)**
-	-	-	-	-	0	1	0	(SDIN-L + SDIN-R)/2 to channel 2
-	-	-	-	-	0	1	1	(SDIN-L - SDIN-R) to channel 2
-	-	-	-	-	1	0	0	(SDIN-R - SDIN-L) to channel 2
-	-	-	-	-	1	0	1	Reserved
-	-	-	-	-	1	1	0	Ground (0) to channel 2
-	-	-	-	-	1	1	1	Reserved

Default values are in bold.

PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

The address must be written in shut down condition.

The writing address must be matched the application circuit used, otherwise the IC will be damaged.

Bits D21–D20:	Selects which PWM channel is output to OUT_A
Bits D17–D16:	Selects which PWM channel is output to OUT_B
Bits D13–D12:	Selects which PWM channel is output to OUT_C
Bits D09–D08:	Selects which PWM channel is output to OUT_D

Note: that channels are enclosed so that channel 1 = 0x00, channel 2 = 0x01, channel 4 =0x03.

Function Description (Cont.)

Table 15. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	-	-	-	-	-	-	**Reserved(Default)**
-	-	**0**	**0**	-	-	-	-	**Multiplex channel 1 to OUT_A(Default)**
-	-	0	1	-	-	-	-	Multiplex channel 2 to OUT_A
-	-	1	0	-	-	-	-	Multiplex channel 1B to OUT_A
-	-	1	1	-	-	-	-	Multiplex channel 2B to OUT_A
-	-	-	-	**0**	**0**	-	-	**Reserved(Default)**
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_B
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_B
-	-	-	-	-	-	**1**	**0**	**Multiplex channel 1B to OUT_B(Default)**
-	-	-	-	-	-	1	1	Multiplex channel 2B to OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	-	-	-	-	-	-	**Reserved(Default)**
-	-	0	0	-	-	-	-	Multiplex channel 1 to OUT_C
-	-	**0**	**1**	-	-	-	-	**Multiplex channel 2 to OUT_C(Default)**
-	-	1	0	-	-	-	-	Multiplex channel 1B to OUT_C
-	-	1	1	-	-	-	-	Multiplex channel 2B to OUT_C
-	-	-	-	**0**	**0**	-	-	**Reserved(Default)**
-	-	-	-	-	-	0	0	Multiplex channel 1 to OUT_D
-	-	-	-	-	-	0	1	Multiplex channel 2 to OUT_D
-	-	-	-	-	-	1	0	Multiplex channel 1B to OUT_D
-	-	-	-	-	-	**1**	**1**	**Multiplex channel 2B to OUT_D(Default)**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved(Default)**

Default values are in bold.

Function Description (Cont.)

Table 16. Hard Clipper Register (0x45)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**-**	**Reserved**
-	-	-	-	-	-	-	0	Hard clipper disenable
-	-	-	-	-	-	-	**1**	**Hard clipper enable (Default)**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Hard Clipper th (Default)**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Hard Clipper th (Default)**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Hard Clipper th (Default)**

Default values are in bold.

DRC CONTROL (0x46)

Each DRC can be enabled independently using the DRC control register. The DRCs are disabled by default.

Table 17. DRC Control Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	-	**Reserved**
-	-	-	-	-	-	-	**0**	**DRC turned OFF(Default)**
-	-	-	-	-	-	-	1	DRC turned ON

Default values are in bold.

Function Description (Cont.)

UVP (0xE1)

Internal under voltage detection can be used to set output stage into Hi-Z before generating a pop.

Table 18. UVP Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
-	-	-	-	**0**	**0**	**0**	**0**	**Disable(Default)**
-	-	-	-	1	0	0	1	UVP=6.5V,UVP Release=7V
-	-	-	-	1	0	1	0	UVP=7V,UVP Release=7.5V
-	-	-	-	1	0	1	1	UVP=8V,UVP Release=8.5V
-	-	-	-	1	1	0	0	UVP=9V,UVP Release=9.5V
-	-	-	-	1	1	0	1	UVP=10V,UVP Release=10.5V
-	-	-	-	1	1	1	0	UVP=12V,UVP Release=12.5V
-	-	-	-	1	1	1	1	UVP=15V,UVP Release=15.5V

Default values are in bold.

Error Reporting

Any fault resulting in output shutdown is signaled by the ERROR pin going low (see Table 19). A sticky version of this pin is available on register 0X02.

Table 19. /ERROR Output States

Fault Description	Error
0	Over-Current (OC) or Under-Voltage (UVP) or Over-Temperature (OTW/OTP)
1	No faults (normal operation)

Function Description (Cont.)

Over-Current (OC) Protection

APA3176 has the protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the /ERROR pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. Hiccup counter after 31 times, it latched.

Over-Temperature Protection

The APA3176 has over-temperature protection system. If the device junction temperature exceeds 160°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and FAULT being asserted low. The APA3176 recovers automatically once the temperature drops approximately 25°.

Under-Voltage Protection (UVP) and Power-On-Reset (POR)

The UVP and POR circuits of the APA3176 fully protect the device in any power-up/down and brownout situation. While powering up, ensuring that all circuits are fully operational when the AVDD supply voltages reach 7V and DVDD supply voltages reach 3V.
A supply voltage drop below the UVP threshold on AVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and /ERROR being asserted low.

Application Information

Power-Supply Decoupling Capacitor, C_S

The APA3176 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalentseries-resistance (ESR) ceramic capacitor, typically 0. 1µF placed as close as possible to the device AVDD pin and 1µF placed to the PVDD_AB and PVDD_CD leads for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is recommended.

Output Low-Pass Filter

If the traces from APA3176 to speaker are short, it doesn't require output filter for FCC & CE standard. A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The figure 22 is the sample for adding ferrite bead; it shows choosing high impedance in high frequency.

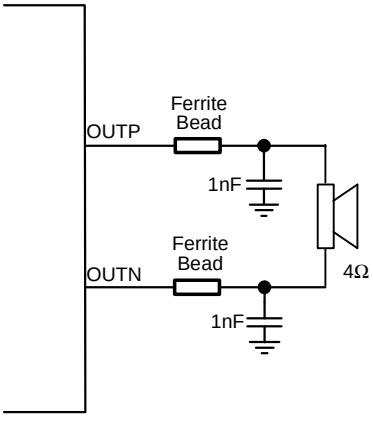


Figure 22. Ferrite Bead Output Filter

Output Low-Pass Filter

Figure 23 and Figure 24 are examples for adding the LC filter (Butterworth), it's recommended for the situation that the trace form amplifier to speaker is too long, and needs to eliminate the radiated emission or EMI.

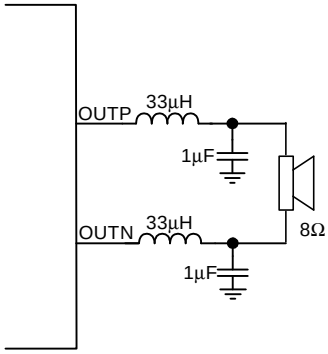


Figure 23. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8Ω

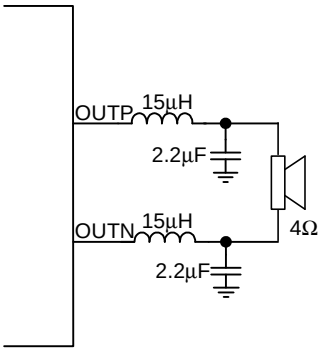


Figure 24. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4Ω

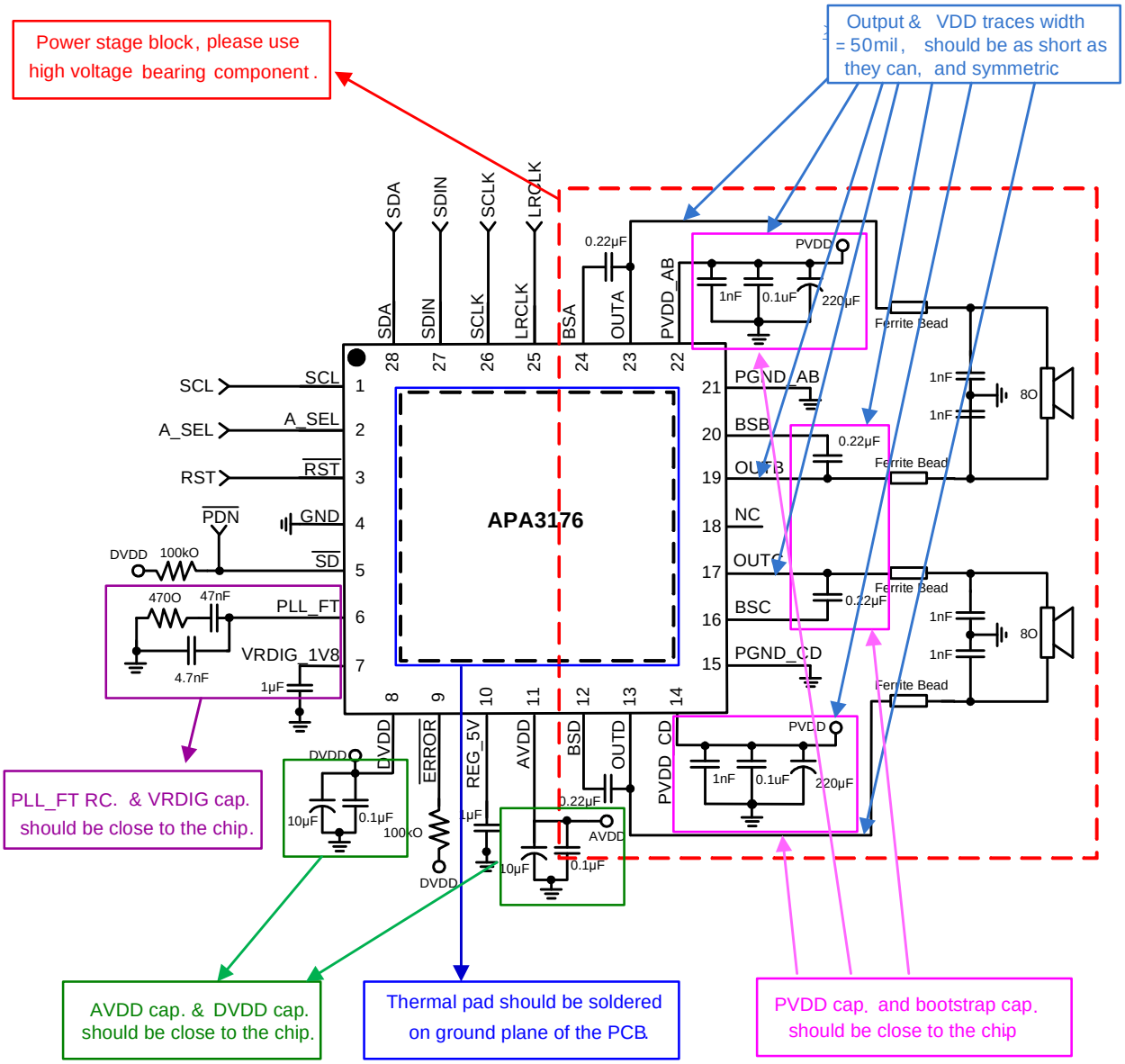
Application Information (Cont.)

BSN and BSP CAPACITORS

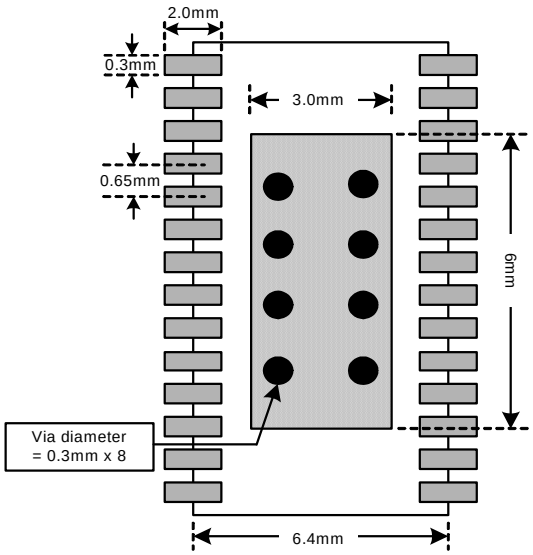
The full H-bridge output stages which use only NMOS transistors require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22µF capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22µF capacitor must be connected from OUTPx to BSPx, and one 0.22µF capacitor must be connected from OUTNx to BSNx. (See the application circuit) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry.

During each high-side switching cycle, the bootstrap capacitors hold the V_{GS} high enough to keep the high-side MOSFETs turned on.

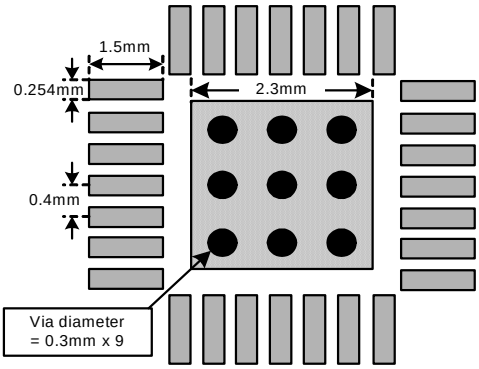
Layout Recommendation



Layout Recommendation (Cont.)

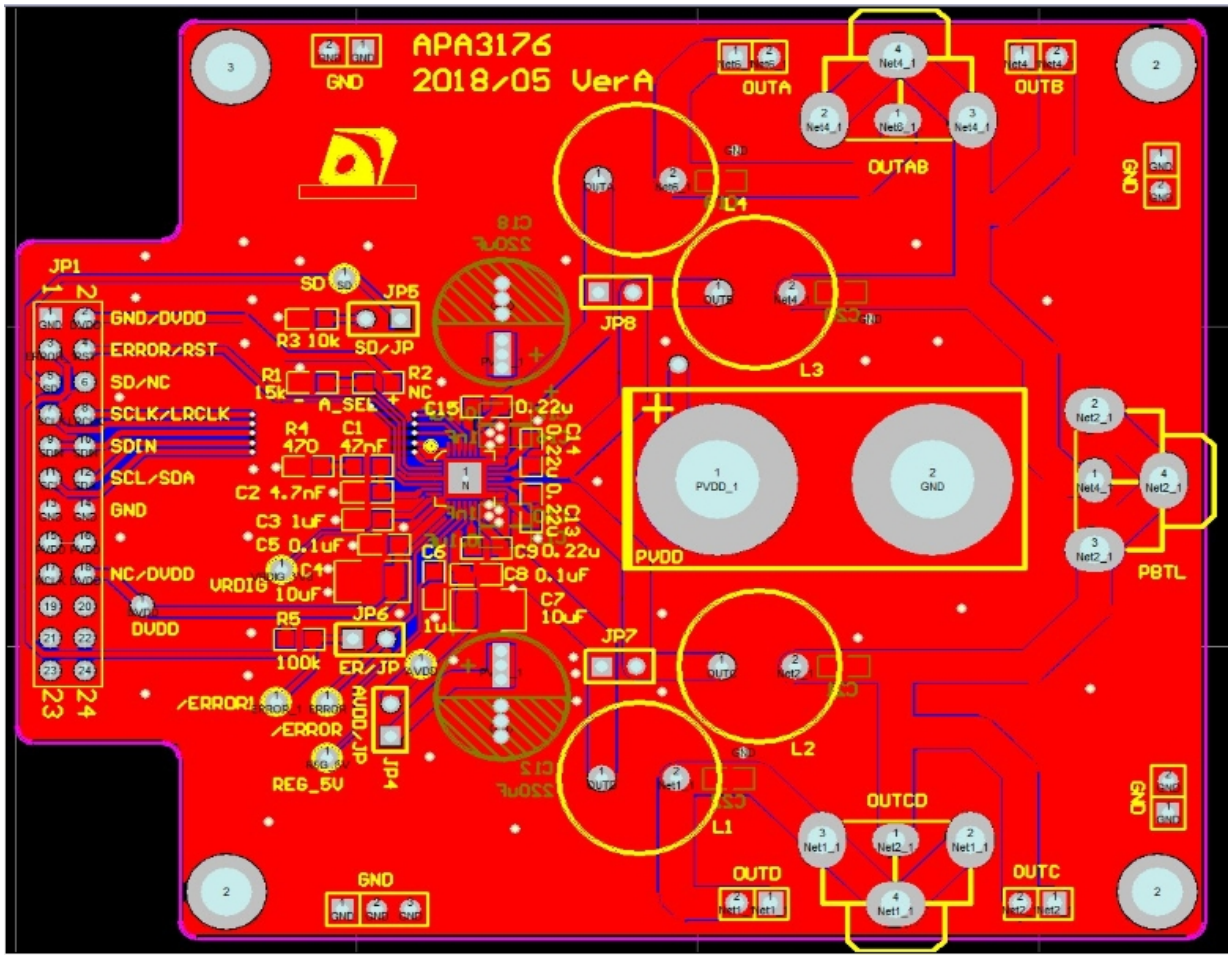


TSSOP-28P Land Pattern Recommendation

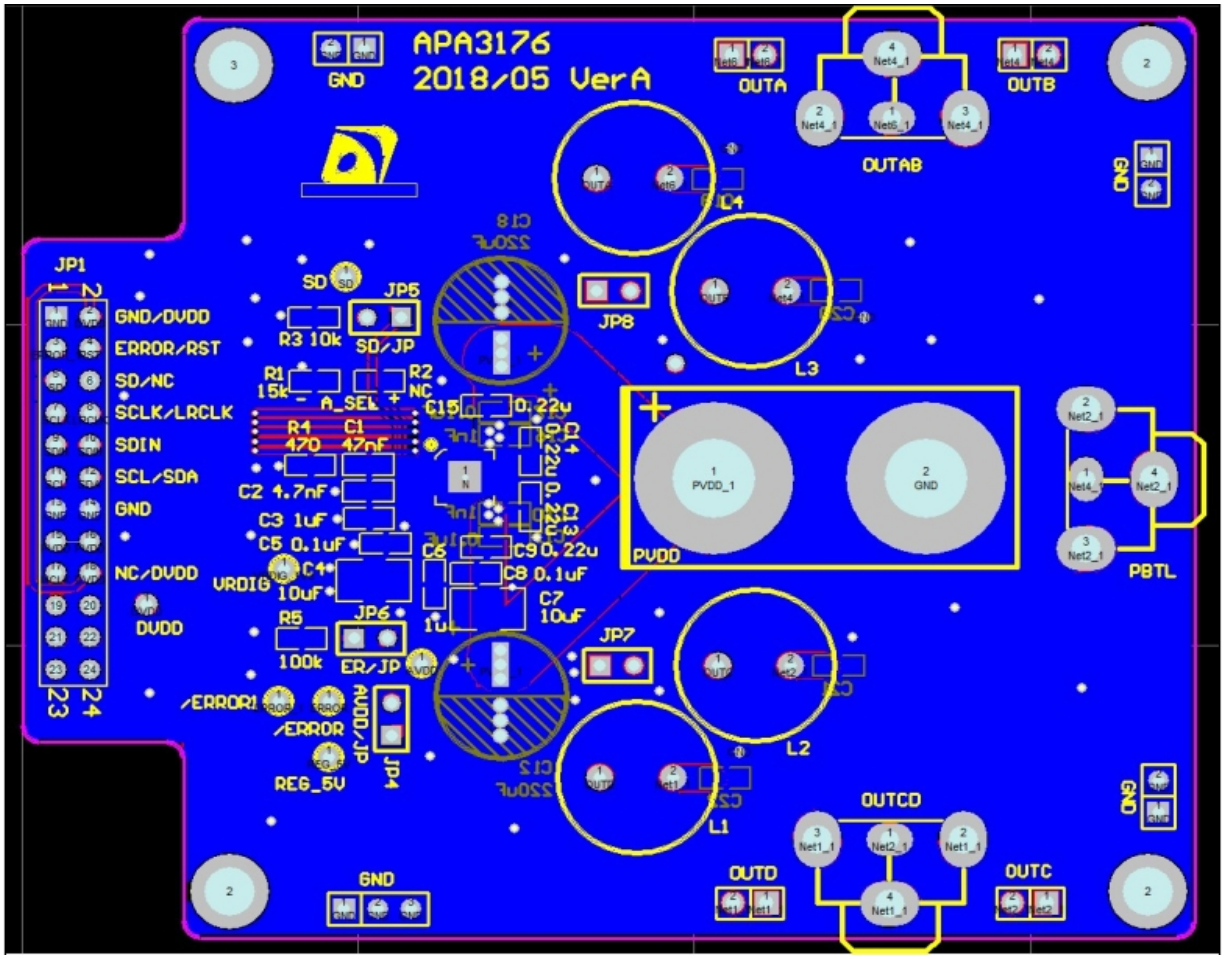


QFN4x4-28A Land Pattern Recommendation

Layout Recommendation (Cont.)

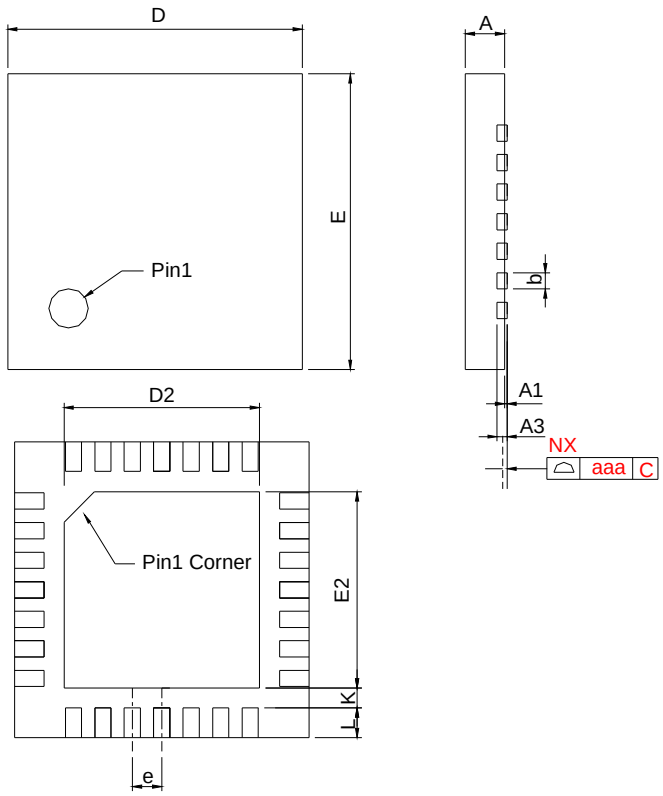


Layout Recommendation (Cont.)



Package Information

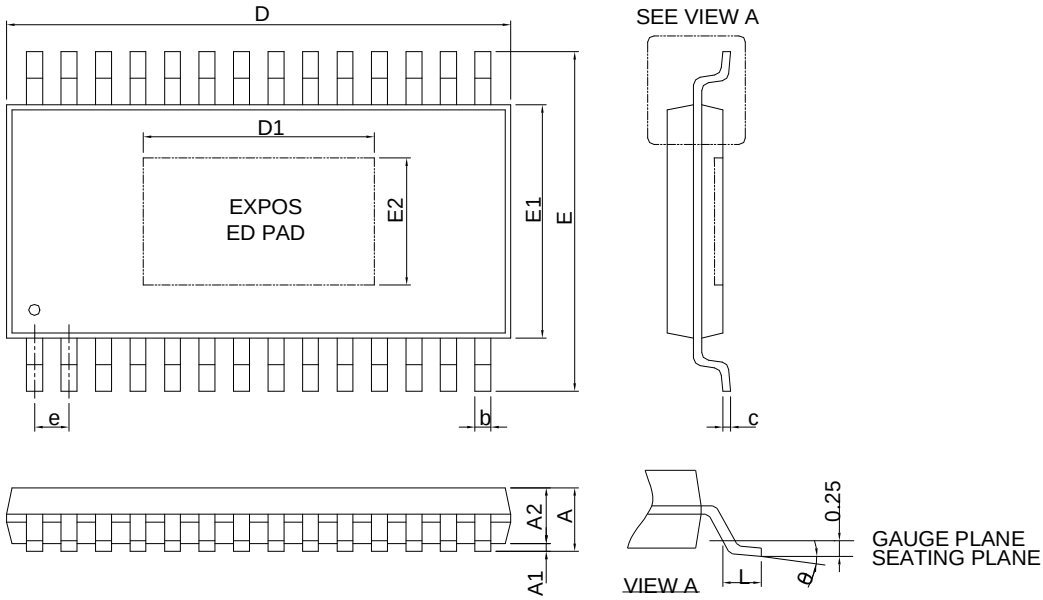
QFN4x4-28A



SYMBOL	QFN4*4-28A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.17	0.27	0.007	0.011
D	3.90	4.10	0.154	0.161
D2	2.10	2.50	0.083	0.098
E	3.90	4.10	0.154	0.161
E2	2.10	2.50	0.083	0.098
e	0.4 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Package Information

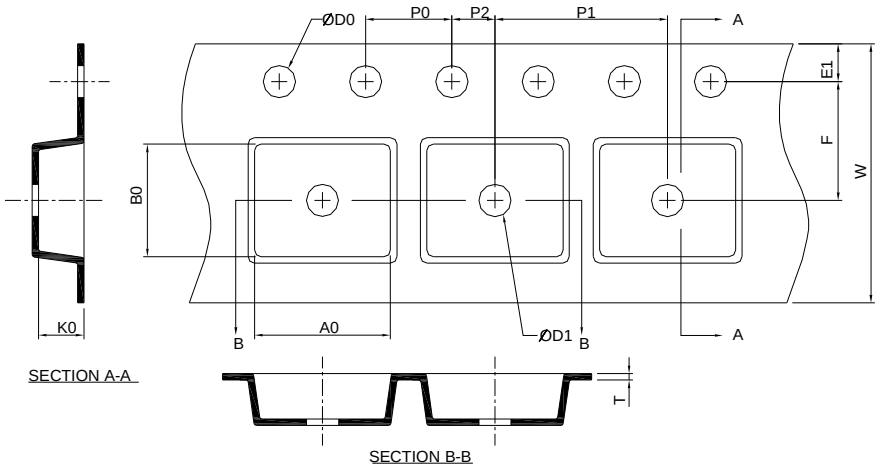
TSSOP-28P

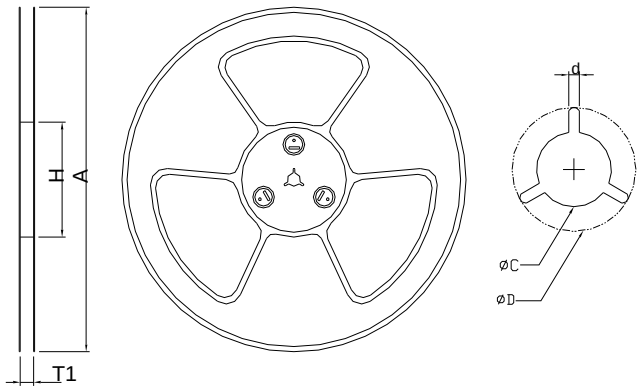


SYMBOL	TSSOP-28P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	9.60	9.80	0.378	0.386
D1	4.50	6.00	0.177	0.236
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC MO-153 AET.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
QFN 4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-28P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	12.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9±0.20	10.20.±0.20	1.50±0.20

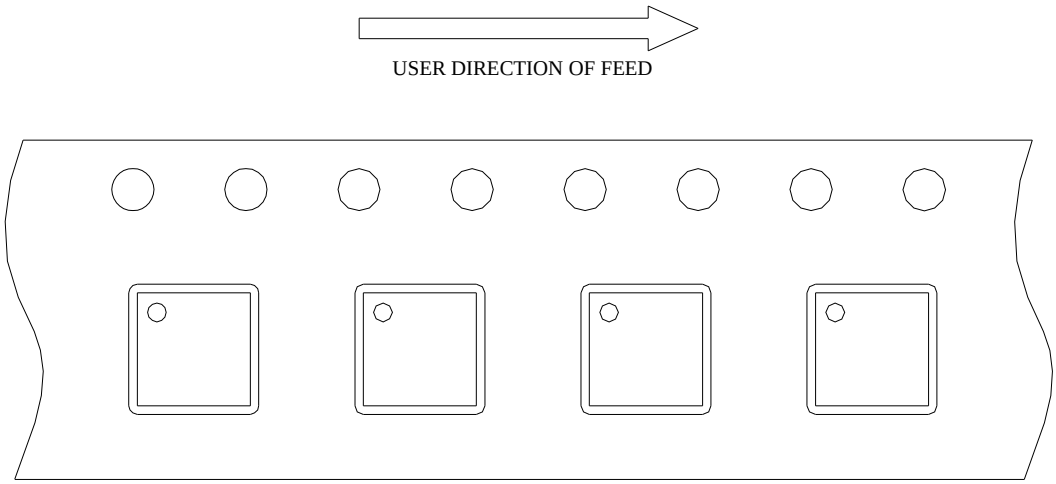
(mm)

Devices Per Unit

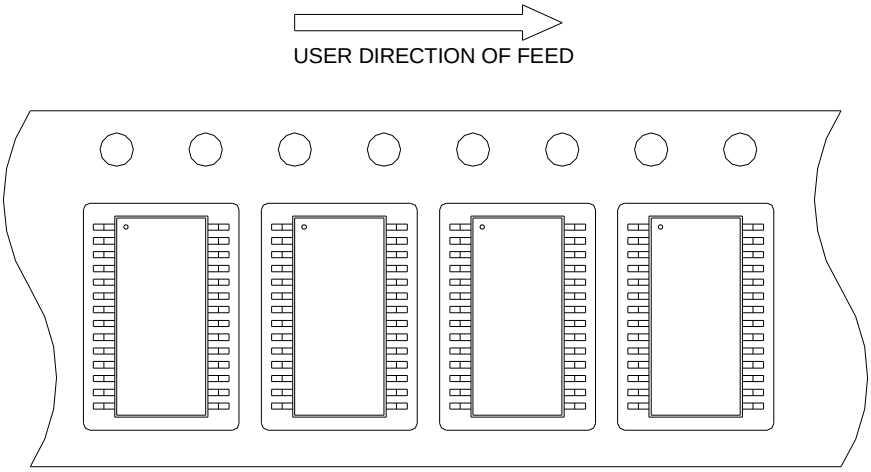
Package Type	Carrier Width	Cover Tape Width	Devices Per Reel
QFN 4x4	12	-	3000
TSSOP-28P	Unit		Quantity
	Tape & Reel		2000

Taping Direction Information

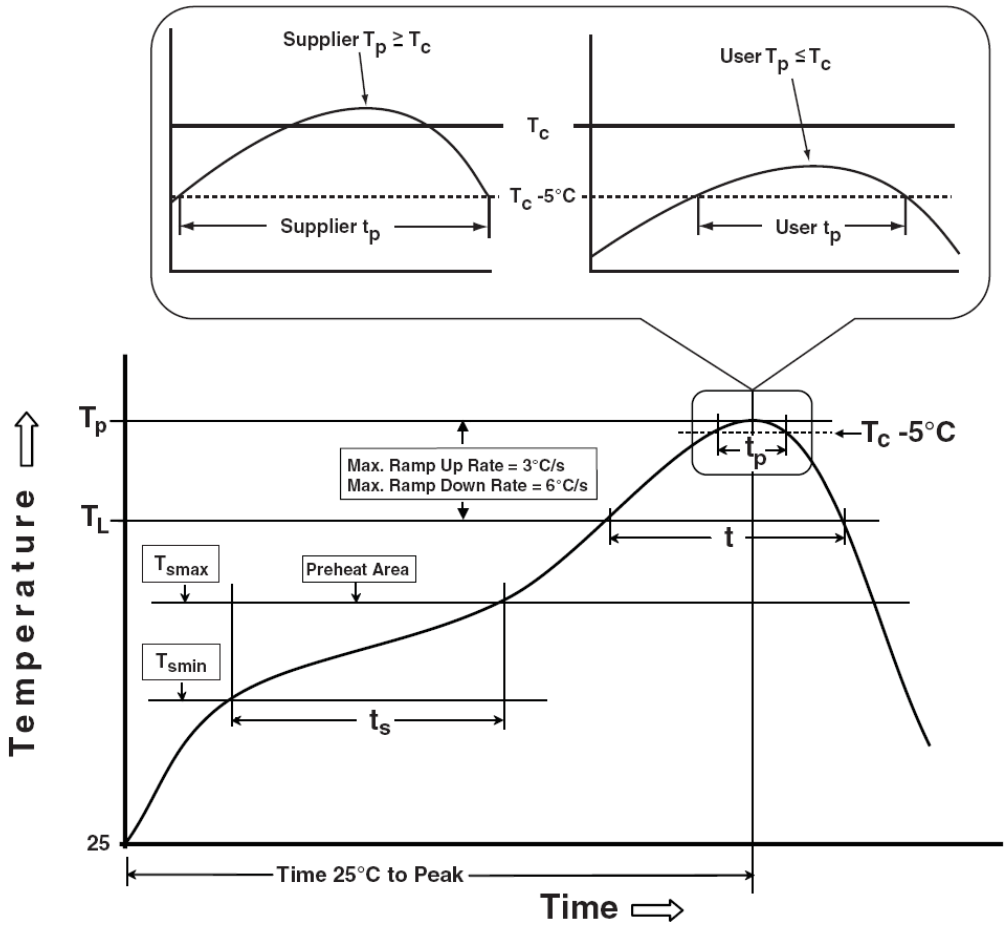
QFN4x4-28A



TSSOP-28P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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