High-Current Overvoltage Protectors with Adjustable OVLO

Features

- **Wide supply voltage range from 3.8V to 28V**
- **Low ON resistance: 50mΩ(typ) at a supply voltage of 5V**
- **Flexible overvoltage-protection trip level**
  - **-Wide adjustable OVLO threshold range from 4V to 20V**
  - **-Preset internal accurate OVLO threshold: 6.8V**
- **Low quiescent current 70μA**
- **Internal 8ms startup debounce**
- **Protection circuitry:**
  - **-Surge Immunity to 100V**
  - **-Overvoltage lockout**
- **Low Capacitance ESD Protection**
- **Available in TDFN3x3-10 Packages**
- **Lead Free Green Devices Available (RoHS Compliant)**

Applications

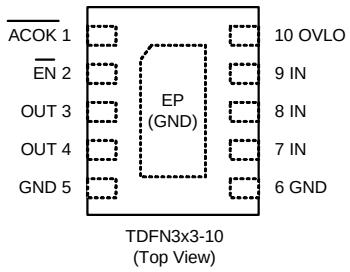
- **Smart Phones**
- **Tablet PCs**
- **Mobile Internet Devices**

General Description

The APL3228 overvoltage protection devices feature a low 50mΩ(typ) RON internal FET and protect low-voltage systems against voltage faults up to +28VDC. An internal clamp also protects the devices from surges up to +100V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

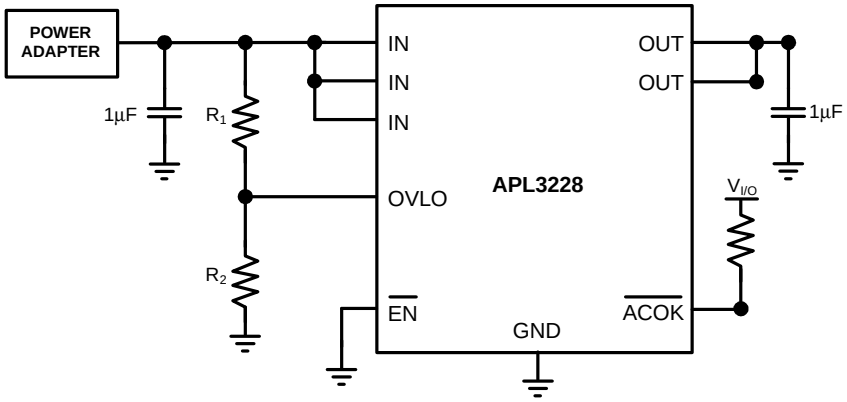
The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the APL3228 automatically choose the accurate internal trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 6.8V. The devices feature an open-drain $\overline{ACOK}$ output indicating a stable supply between minimum supply voltage and V_{OVLO}. The APL3228 are also protected against over current events by an internal thermal shutdown.

Pin Configuration

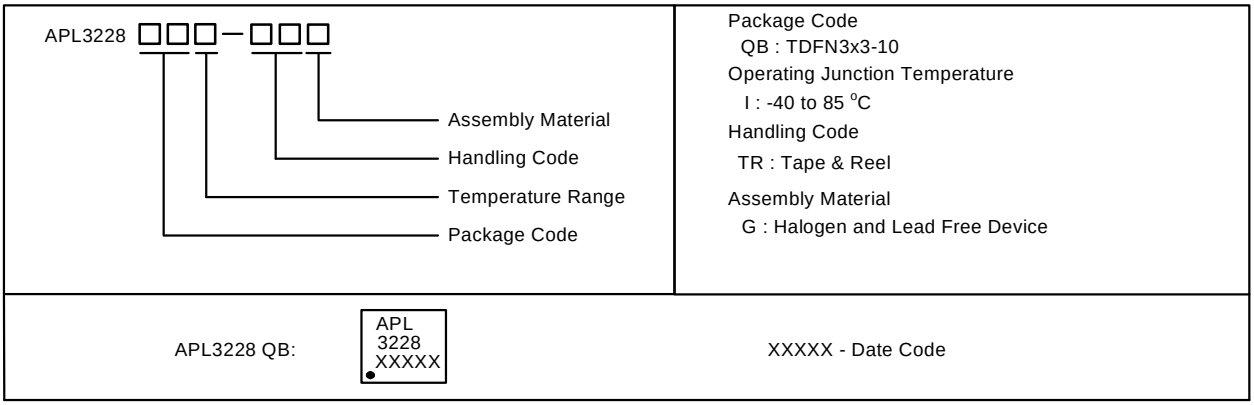


TDFN3x3-10
(Top View)

Simplified Application Circuit



Ordering and Marking Information



Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	IN to GND Voltage	-0.3 ~ 32	V
V_{OUT}	OUT to GND Voltage	-0.3 ~ 32	V
V_{OVLO}	OVLO to GND Voltage	-0.3 ~ 24	V
V_{ACOK}	$\overline{ACOK}$ to GND Voltage	-0.3 ~ 7	V
V_{EN}	$\overline{EN}$ to GND Voltage	-0.3 ~ 7	V
I_{OUT}	OUT Output Current	3.5	A
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in free air (Note 2) TDFN3x3-10	60	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance in free air (Note 3) TDFN3x3-10	8	°C/W

Note 2 :θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TDFN3x3-10 is soldered directly on the PCB.

Note 3: The "Thermal Pad Temperature" is measured on the PCB copper area connected to the thermal pad of package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
IN	IN Input Voltage	3.8 ~ 28	V
I_{OUT}	Output Current	0 ~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4 : Refer th the typical application circuit.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, T_A= -40~85°C· Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3228			Unit
			Min	Typ	Max	
V_{IN}	Input Voltage Range		3.8	-	28	V
V_{IN_CLAMP}	Input Clamp Voltage	I_{IN} = 10mA, T_A = +25ºC	-	31.5	-	V
I_{IN}	Input Supply Current	V_{IN}=5V	-	70	150	µA
I_{SD}	Input Shutdown Current	V_{EN}=5V	-	30	70	µA
I_{IN_Q}	OVLO Supply Current	V_{OVLO} = 3V, V_{IN} = 5V,V_{OUT} = 0V	-	63	120	µA
V_{IN_OVLO}	Internal Overvoltage Trip Level	V_{IN} rising	6.6	6.8	7.0	V
		V_{IN} falling	6.5	6.7	6.9	
	Input OVP Recovery Hysteresis		-	100	-	mV
	Input OVP Propagation Delay		-	-	1	µs
V_{OVLO_TH}	OVLO Set Threshold		1.18	1.22	1.26	V
	Adjustable OVLO Threshold Range		4	-	20	V
V_{OVLO_SELECT}	External OVLO Select Threshold		0.2	-	0.3	V
R_{ON}	Switch On-Resistance	V_{IN} = 5V, I_{OUT} = 1A, T_A = +25ºC	-	50	-	mΩ
I_{OVLO}	OVLO Input Leakage Current	V_{OVLO} = V_{OVLO_TH}	-100	-	100	nA
V_{IN_LEAK}	IN Leakage Voltage by OVLO	V_{OVLO} = 20V, V_{IN} = unconnected,R_{OVLO} = 1MΩ	-	-	0.5	V
	Thermal Shutdown		120	130	140	°C
	Thermal-Shutdown Hysteresis		-	30	-	°C
DIGITAL SIGNALS (ACOK)						
V_{OL}	$\overline{ACOK}$ Output Low Voltage	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA, see the Typical Application Circuit	-	-	0.4	V
V_{ACOK_LEAK}	$\overline{ACOK}$ Leakage Current	$V_{I/O}$ = 3.3V, ACOK deasserted, see the Typical Application Circuit	-1	-	+1	µA
T_{ACOK_DEB}	$\overline{ACOK}$ goes low Debounce Time	VOUT is above 10%VIN	-	2	-	ms
	$\overline{ACOK}$ goes high Debounce Time	VOUT is below 90%VIN	-	2	-	µs
$\overline{EN}$						
$\overline{ENH}$	$\overline{EN}$ Voltage High		1.2	-	-	V
$\overline{ENL}$	$\overline{EN}$ Voltage Low		-	-	0.4	V
$\overline{EN}$_leak	$\overline{EN}$ Leakage Current	$\overline{EN}$=5V	-	10	-	µA

Electrical Characteristics(Cont.)

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, T_A= -40~85°C. Typical values are at T_J=25°C.

Symbol	Parameter	Test Conditions	APL3228			Unit
			Min	Typ	Max	
OCP						
I_{OCP}	OCP Threshold		3.7	4	-	A
$T_{DEB(OCP)}$	OCP Debounce Time		-	80	-	µs
$T_{ON(OCP)}$	OCP Recovery Time		-	40	-	ms
I_{SHORT}	Short circuit Current		-	8	-	A
TIMING CHARACTERISTICS (Figure 1)						
t_{DEB}	Debounce Time	Time from 2.5V < V_{IN} < V_{IN_OVLO} to V_{OUT} = 10% of V_{IN}	-	8	-	ms
t_{SS}	Soft-Start Time	V_{OUT} = 10% of V_{IN} to soft-start off	-	30	-	ms
t_{ON}	Switch Turn-On Time	V_{IN} = 5V, R_L = 100Ω,C_{LOAD} = 100µF, V_{OUT} from 10%,V_{IN} to 90% V_{IN}	-	2	-	ms
t_{OFF}	Switch Turn-Off Time	V_{IN} > V_{OVLO} to V_{OUT} = 80% of V_{IN},R_L = 100Ω, V_{IN} rising at 2V/µs	-	2	-	µs
ESD PROTECTION						
	Human Body Model	All pins	-	±2	-	kV
	IEC 61000-4-2 Contact Discharge	IN pin	-	±8	-	kV
	IEC 61000-4-2 Air Gap Discharge	IN pin	-	±15	-	kV

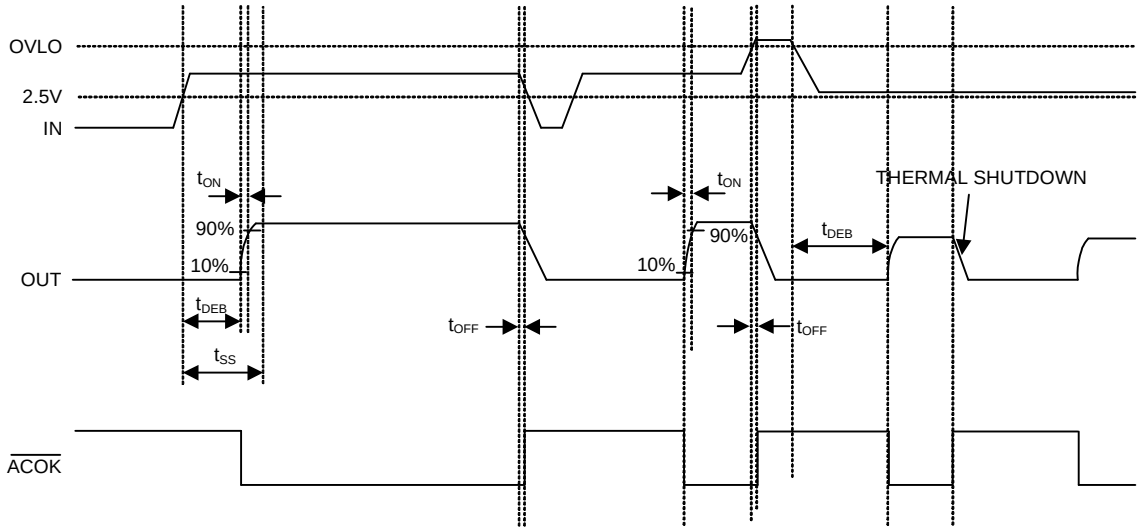
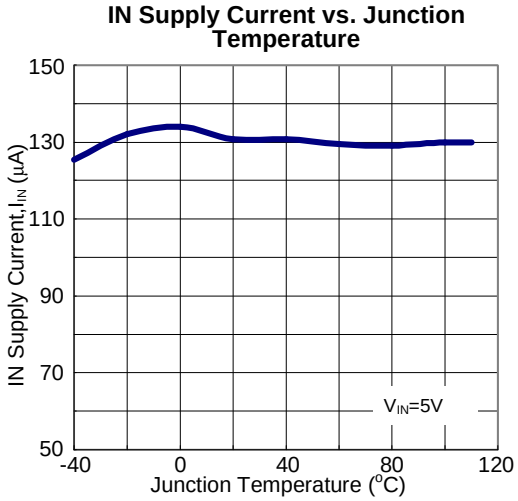
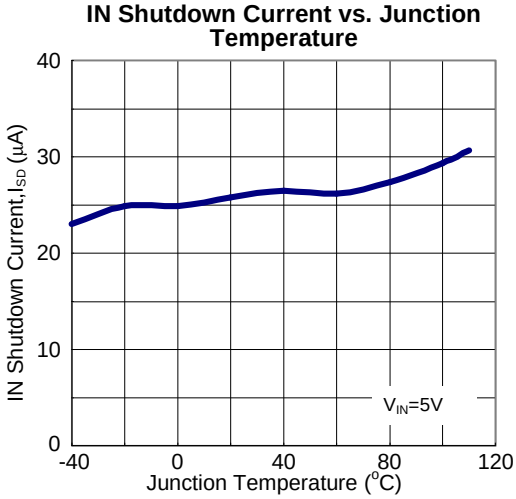
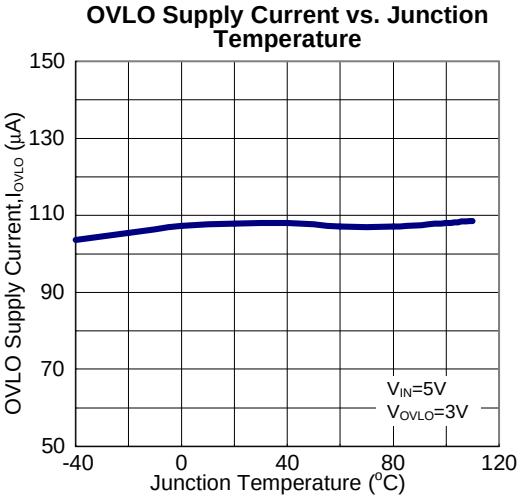


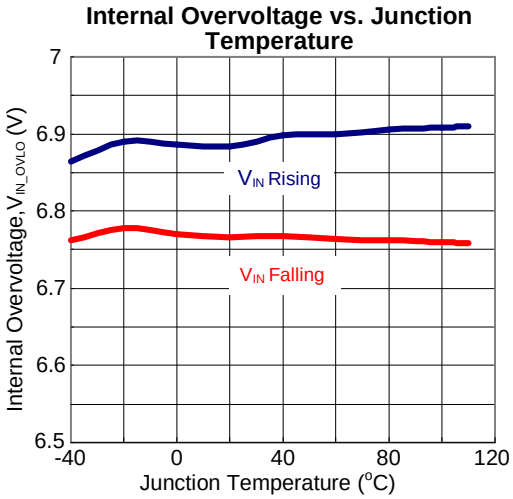
Figure 1. Timing Diagram

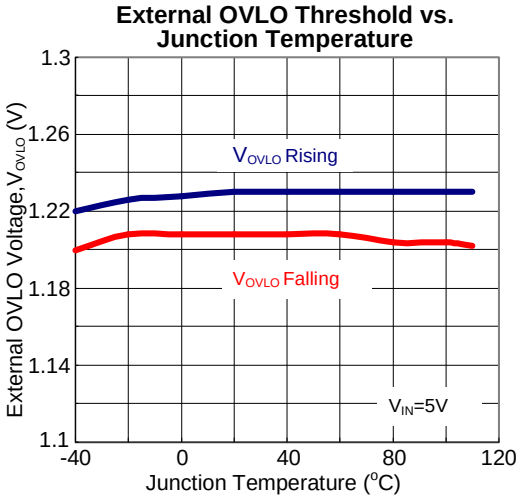
Typical Operating Characteristics





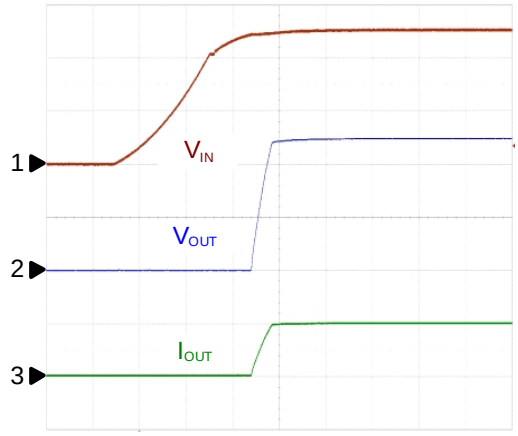






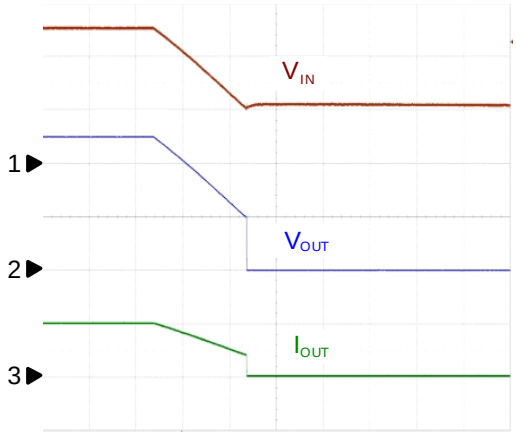
Operating Waveforms

Normal Power On



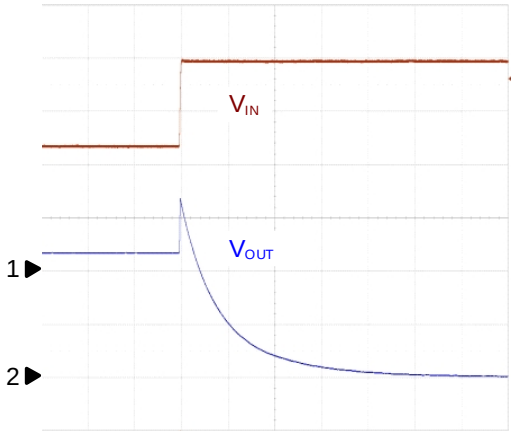
V_{IN}=0 to 5V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=10Ω
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:I_{OUT},0.5A/Div, DC
TIME:5ms/Div

Normal Power Off



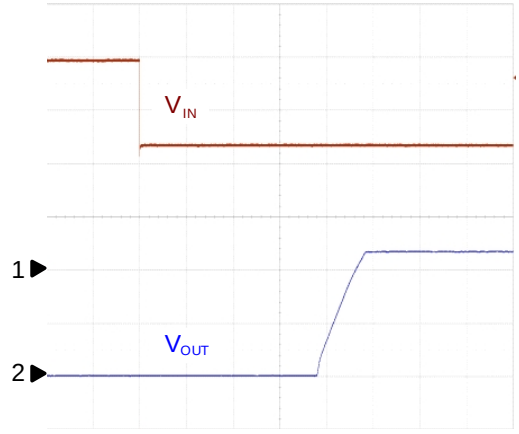
V_{IN}=5 to 0V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=10Ω
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:I_{OUT},0.5A/Div, DC
TIME:5ms/Div

Internal Overvoltage Protection



V_{IN}=5 to 8V
C_{OUT}=1µF,C_{IN}=1µF
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
TIME:1ms/Div

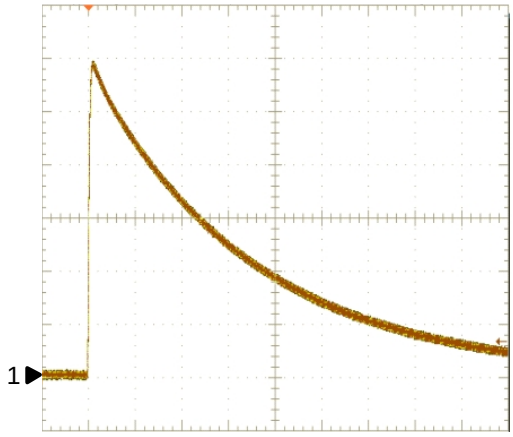
Recovery from Input OVP



V_{IN}=8V to 5V
C_{OUT}=1µF,C_{IN}=1µF
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
TIME:2ms/Div

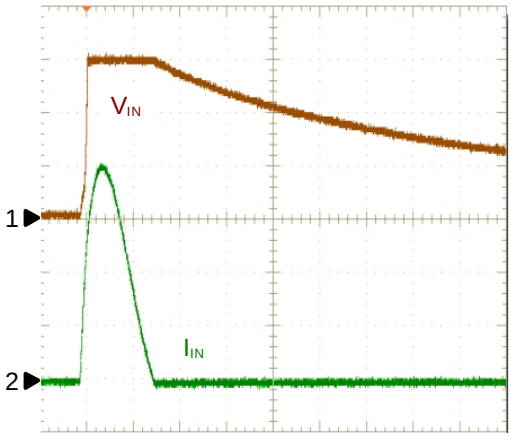
Operating Waveforms (Cont.)

120V Surge Test Waveform



CH1:20V/Div, DC
TIME:20μs/Div

120V Surge Test Waveform

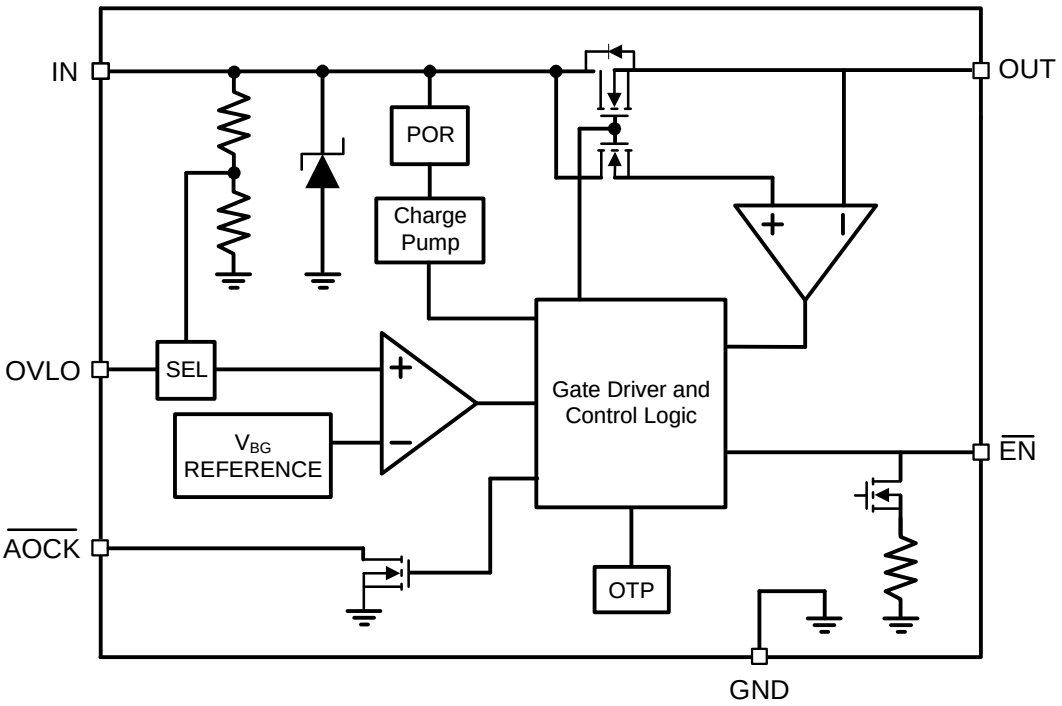


C_{OUT}=1μF,C_{IN}=1μF
CH1:V_{IN},10V/Div, DC
CH2:I_{IN},10A/Div, DC
TIME:20μs/Div

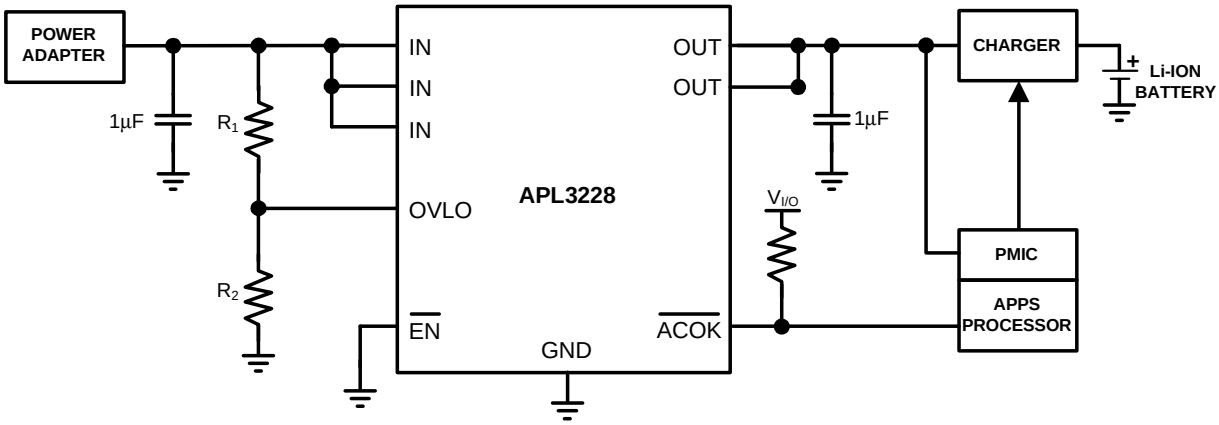
Pin Description

PIN		Function
TDFN3x3-10	NAME	
1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum VIN and VOVLO after debounce. Connect a pullup resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.
2	$\overline{EN}$	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND to a pull down or to a I/O pin. This pin does not have an impact on the fault detection.
10	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.
3,4	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
7,8,9	IN	Voltage Input. Connect IN with a 1uF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.
5,6	GND	Ground. Connect GND pins together for proper operation

Block Diagram



Typical Application Circuit



Function Description

Detailed Description

The APL3228 overvoltage protection devices feature a low on-resistance (RON) internal FET and protect low-voltage systems against voltage faults up to +28VDC. An internal clamp also protects the devices from surges up to +100V. If the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The 8ms debounce time built into the device prevents false turn on of the internal FET during startup.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when $V_{IN} < V_{IN\_OVLO}$ if internal trip thresholds are used and when $V_{OVLO} < V_{OVLO\_TH}$ if external trip thresholds are used. The charge-pump startup, which occurs after a 8ms debounce delay, turns the internal FET on.

Internal Switch

The APL3228 incorporate an internal FET with a 50mΩ (typ) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Overvoltage Lockout (OVLO)

When the V_{IN} voltage rises above V_{OVLO}, the internal FET switch is turned OFF. When the VIN voltage returns below V_{OVLO}, the FET switch is turned on again after the internal delay of. This delay time ensures that the VIN supply has stabilized before turning the switch back on. When the OVP condition is cleared and the FET is completely turned ON.

Thermal-Shutdown Protection

The APL3228 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds +130°C (typ). The device exits thermal shutdown after the junction temperature cools by 30°C (typ).

$\overline{\text{ACOK}}$ Output

An open-drain $\overline{\text{ACOK}}$ output gives the APL3228 the ability to communicate a stable power source to the host system. $\overline{\text{ACOK}}$ is driven low after input voltage is stable between minimum VIN and VOVLO after debounce. Connect a pullup resistor from $\overline{\text{ACOK}}$ to the logic I/O voltage of the host system. $\overline{\text{ACOK}}$ is high impedance after thermal shutdown.

OCP

The output current is monitored by the internal OCP circuit. When the output current reaches the OCP threshold, the device limits the output current at OCP threshold level. If the OCP condition continues for a debounce time, the internal power FET is turned off. After the recovery time, the FET will be turned on again and the output current is monitored again.

Under normal application, when the current reach the current limit level with debounce time 80us, the internal switch turn off. The release condition is after 40ms & T_J< 90°C.

Application Information

IN Bypass Capacitor

For most applications, bypass IN to GND with a 1μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

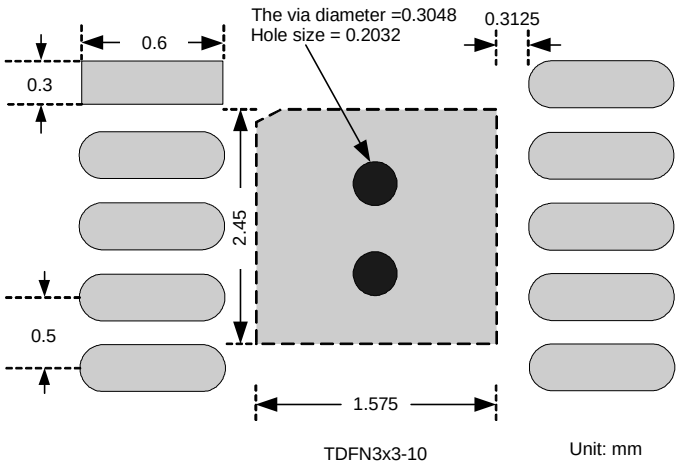
External OVLO Adjustment Functionality

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.
If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor divider. R1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_THRESH}, and R1 are known,R2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left(1 + \frac{R1}{R2}\right)$$

This external resistor-divider is completely independent from the internal resistor-divider.

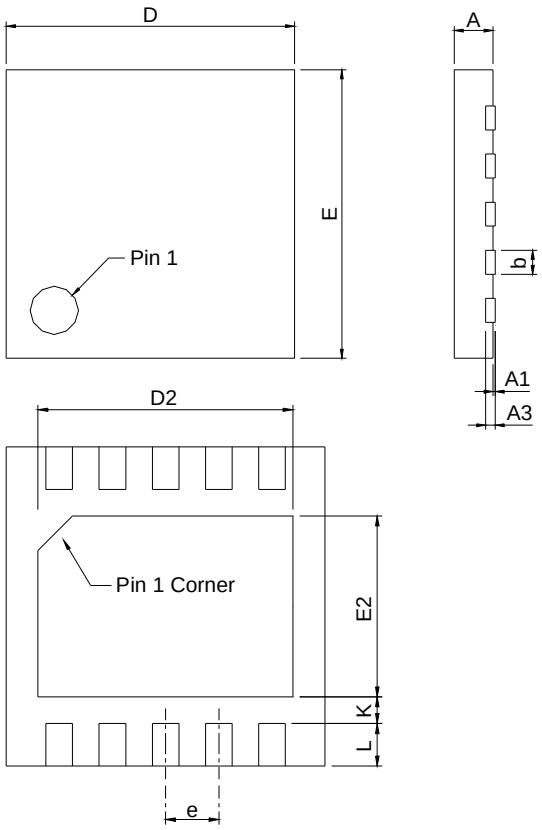
Recommended Minimum Footprint



TDFN3x3-10 Unit: mm

Package Information

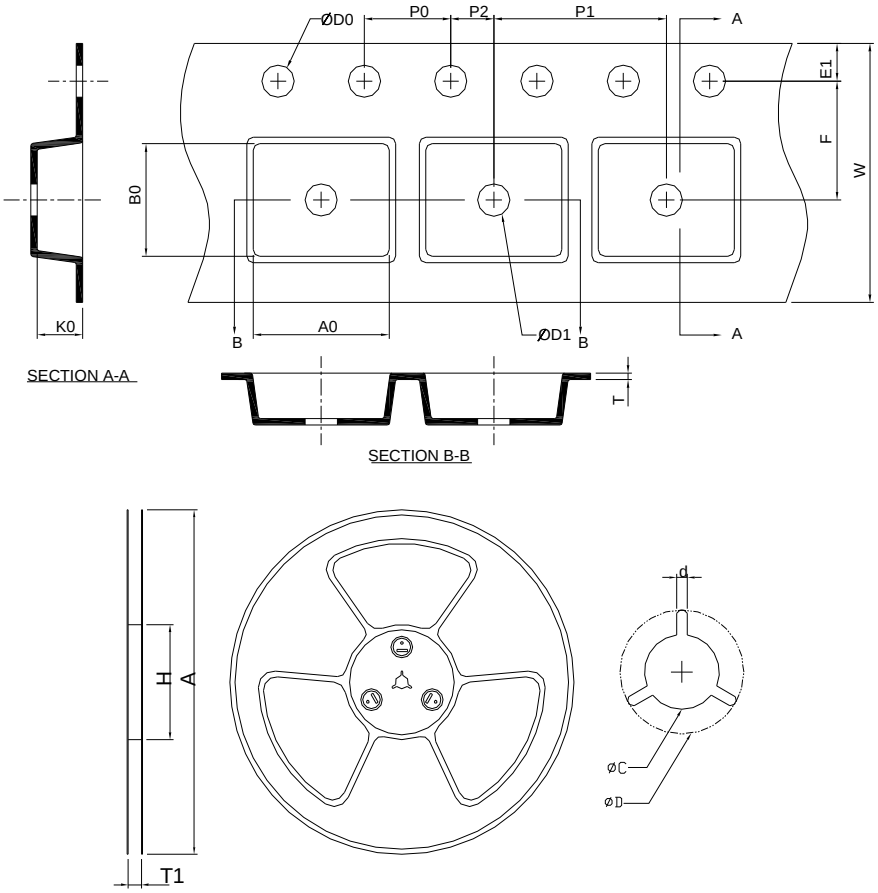
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

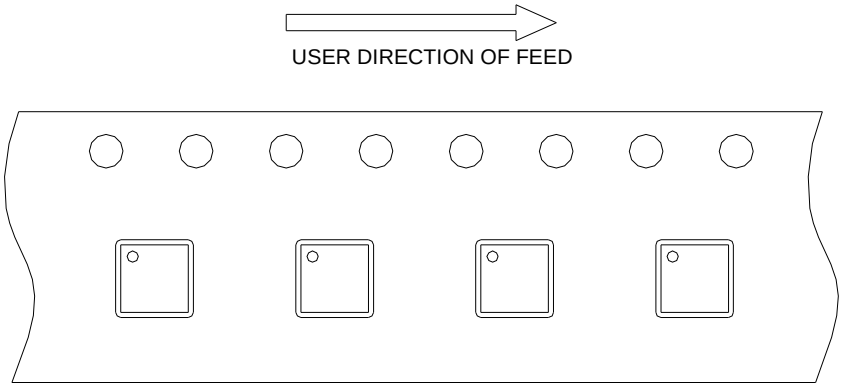
(mm)

Devices Per Unit

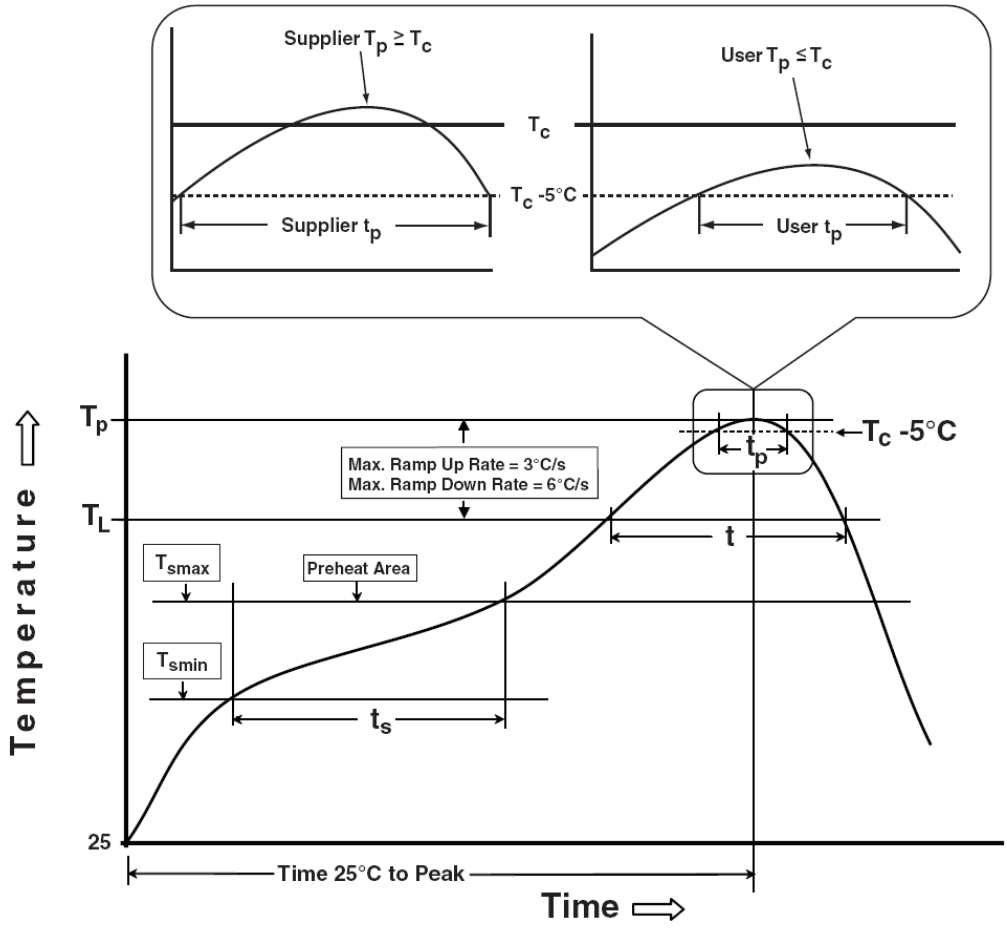
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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