Ultra-Low On-Resistance, Power Load Switch with Soft Start

Features

- **Ultra-Low On-Resistance: 15mΩ(typical)**
- **Low Quiescent Current: 20μA(max)**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Input Voltage Range (VIN): 0.8V to V_{DD}+0.3**
- **Supply Voltage Range (VDD): 3V to 5.5V**
- **Current Limit Protection**
- **Enable Input**
- **Output Discharge when Switch Disabled**
- **Over-Temperature Protection**
- **Tiny small WLCSP1.16x0.76-6 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

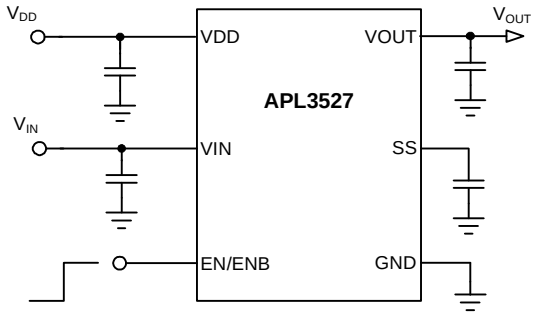
The APL3527 is an ultra-low on-resistance, power-distribution switch with external soft start control.

The device integrates some protection features, including current-limit protection and over-temperature protection. The current-limit protection can protect down stream devices from catastrophic failure by limiting the output current at current limit threshold during over-load or short-circuit events. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 150°C and will automatically turns on the power switch when the temperature drops by 30°C. The device is available in lead free WLCSP1.16x0.76-6 package.

Applications

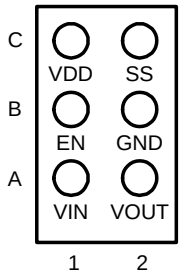
- **Notebook**
- **AIO PC**

Simplified Application Circuit



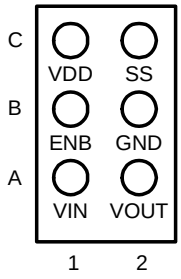
Pin Configuration

APL3527A/B/C/G



WLCSP1.16x0.76-6
(Top View)

APL3527D/E/F/H



WLCSP1.16x0.76-6
(Top View)

Ordering and Marking Information

APL3527 □□□□–□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- Output Current/Enable Function

Output Current/Enable Function
A : 1.5A/Active High B : 1A/Active High C : 0.4A/Active High
D : 1.5A/Active Low E : 1A/Active Low F : 0.4A/Active Low
G : 3A/Active High H : 3A/Active Low

Package Code
HA : WLCSP1.16x0.76-6

Operating Ambient Temperature Range
I : -40 to 85°C

Handling Code
TR : Tape & Reel

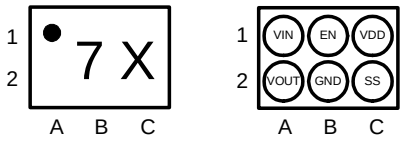
Assembly Material
G : Halogen and Lead Free Device

APL3527A~H HA: 7X

X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

WLCSP1.16x0.76-6 Marking (Top View)



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	VDD to GND Voltage	-0.3 ~ 6	V
V_{IN}	VIN to GND Voltage	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 6	V
V_{EN}, V_{ENB}	EN, ENB to GND Voltage	-0.3 ~ 6	V
I_{OUT}	Continuous Output Current	Internally Limited	A
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in free air (Note 2) WLCSP1.16x0.76-6	100	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Range	Unit
V_{DD}	VDD Input Voltage ($V_{DD} \geq V_{IN}$)		3.0 ~ 5.5	V
V_{IN}	VIN Input Voltage		0.8 ~ V_{DD}+0.3	V
I_{OUT}	VOUT Output Current	APL3527A/D	0 ~ 1.5	A
		APL3527B/E	0 ~ 1	A
		APL3527C/F	0 ~ 0.4	A
		APL3527G/H	0 ~ 3	A
V_{IH}	EN Logic High Input Voltage		0.9 ~ 5.5	V
V_{IL}	ENB Logic Low Input Voltage		0 ~ 0.3	V
C_{SS}	Soft-Start Capacitor		0 ~ 10	nF
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Note 3: Please refer to the typical application circuit.

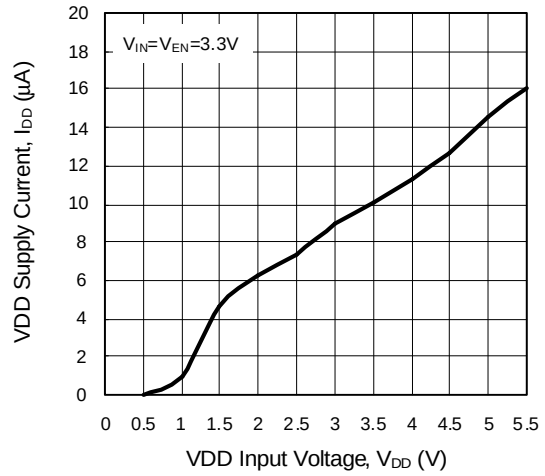
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}= 5V, V_{DD} =5V, V_{EN} =5V (or V_{ENB}=0V) and T_A= -40~85°C. Typical values are at T_A=25°C.

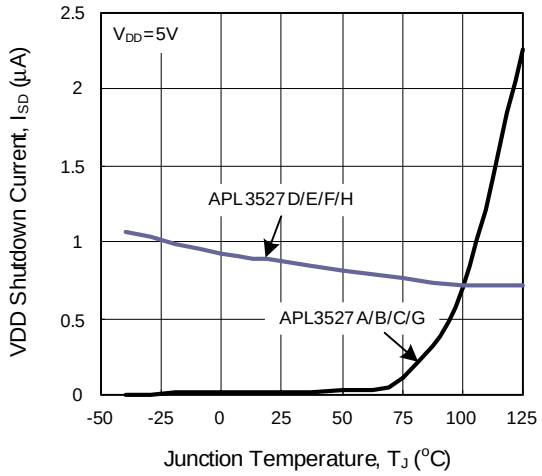
Symbol	Parameter		Test Conditions	APL3527			Unit
				Min	Typ	Max	
SUPPLY CURRENT							
I_{DD}	VDD Supply Current		No load	-	15	20	µA
I_{SD}	VDD Supply Current at Shutdown		No load, V_{DD}=5V, V_{EN}=Low (APL3527A/B/C/G)	-	-	1	µA
			No load, V_{DD}=5V, V_{EN}=High (APL3527D/E/F/H)	-	0.9	1.5	µA
	VIN Supply Current		No load	-	10	20	µA
I_{IN_OFF}	VIN Off-State Supply Current		No load, V_{DD}=5V, V_{EN}=0V or V_{ENB}=5V, V_{IN}=5V	-	0.1	8	µA
			No load, V_{DD}=5V, V_{EN}=0V or V_{ENB}=5V, V_{IN}=3.3V	-	0.1	3	µA
			No load, V_{DD}=5V, V_{EN}=0V or V_{ENB}=5V, V_{IN}=1.8V	-	0.1	2	µA
			No load, V_{DD}=5V, V_{EN}=0V or V_{ENB}=5V, V_{IN}=0.8V	-	0.1	1	µA
	VOUT Leakage Current		V_{DD}=5V, V_{IN}=5V, V_{EN}=0V or V_{ENB}=5V	-	0.1	7	µA
UNDER-VOLTAGE LOCKOUT (UVLO)							
	Rising VDD UVLO Threshold		V_{DD} rising, T_J= 25°C	1.9	2.2	2.5	V
	VDD UVLO Hysteresis			-	0.1	-	V
POWER SWITCH							
$R_{DS(ON)}$	Power Switch On Resistance		I_{OUT}=0.5A, T_J=25°C	-	15	18	mΩ
			I_{OUT}=0.5A, T_J=-40~125°C	-	-	20	mΩ
	VOUT Discharge Resistance		V_{EN}=0V or V_{ENB}=5V, VOUT force 1V	-	100	150	Ω
CURRENT LIMIT AND SHORT CIRCUIT PROTECTIONS							
I_{LIM}	Current Limit Threshold	APL3527A/D	T_J=25°C	2.3	2.5	2.7	A
			T_J=-40 to 125°C	2	-	-	A
		APL3527B/E	T_J=25°C	1.3	1.5	1.7	A
			T_J=-40 to 125°C	1.1	-	-	A
		APL3527C/F	T_J=25°C	0.5	0.85	1.2	A
		APL3527G/H	T_J=25°C	3.5	4	4.5	A
SOFT-START CONTROL PIN							
I_{SS}	SS Current		V_{SS}=0V	-	4	-	µA
	SS Discharge Resistance		V_{SS}=6V, V_{EN}=0V or V_{ENB}=5V, measured at SS	-	10	-	kΩ
EN OR ENB INPUT PIN							
	Input Logic High		V_{DD}=3~5.5V	0.9	-	-	V
	Input Logic Low		V_{DD}=3~5.5V	-	-	0.3	V
	Input Current			-	-	1	µA
t_D	Turn On Delay Time			-	1.75	-	ms
OVERT-TEMPERATURE PROTECTION (OTP)							
	Over-Temperature Threshold		T_J rising	-	150	-	°C
	Over-Temperature Hysteresis			-	30	-	°C

Typical Operating Characteristics

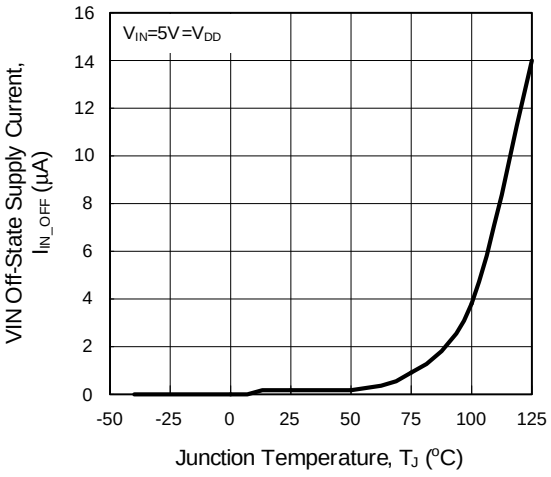
VDD Supply Current vs. VDD Input Voltage



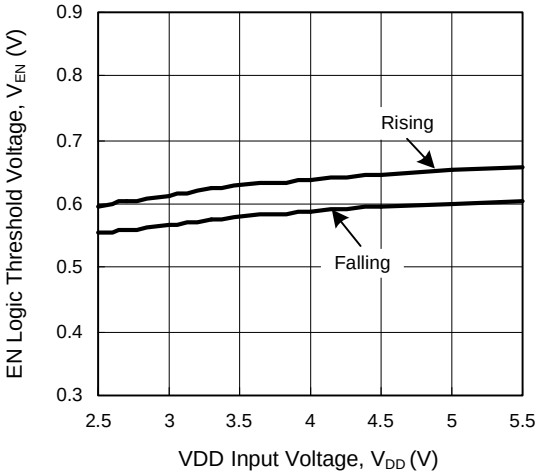
VDD Shutdown Current vs. Junction Temperature



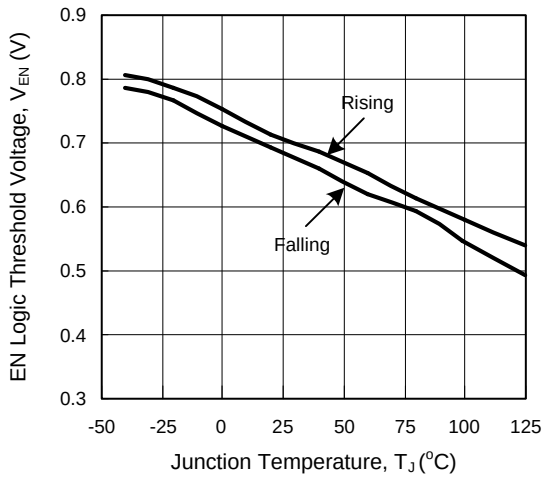
VIN Off-State Supply Current vs. Junction Temperature



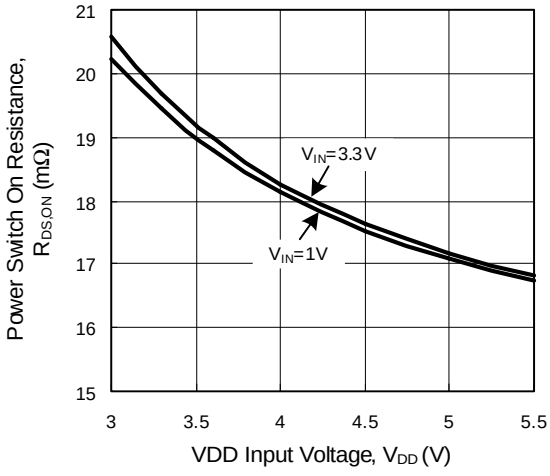
EN Logic Threshold Voltage vs. VDD Input Voltage



EN Logic Threshold Voltage vs. Junction Temperature

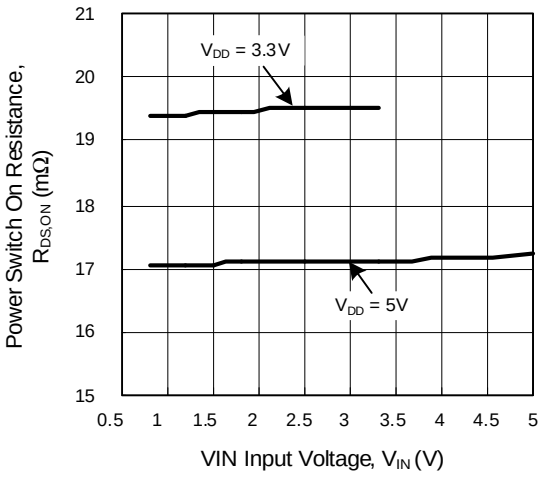


Power Switch On Resistance vs. VDD Input Voltage

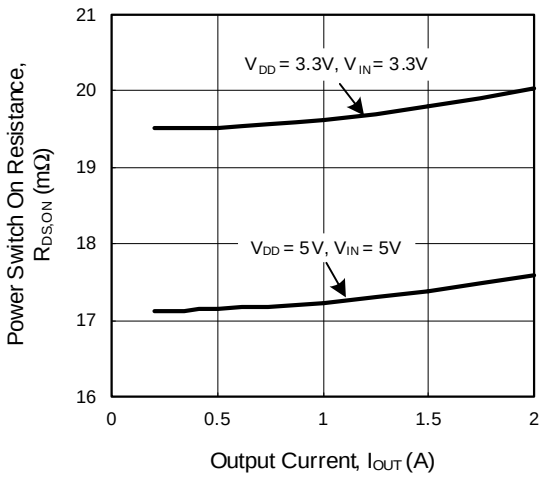


Typical Operating Characteristics(Cont.)

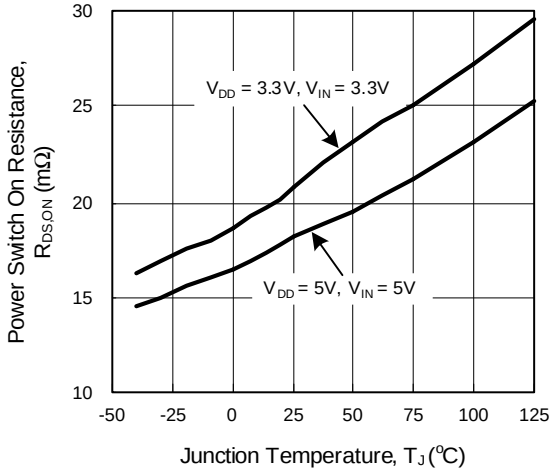
Power Switch On Resistance vs. VIN Input Voltage



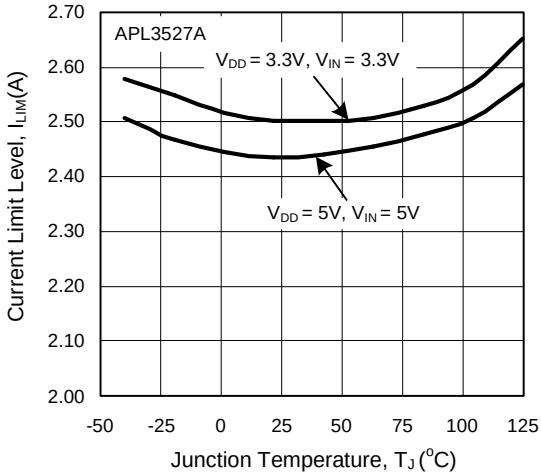
Power Switch On Resistance vs. Output Current



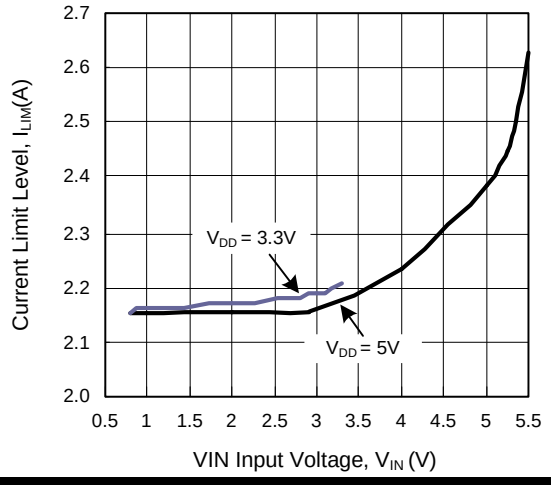
Power Switch On Resistance vs. Junction Temperature



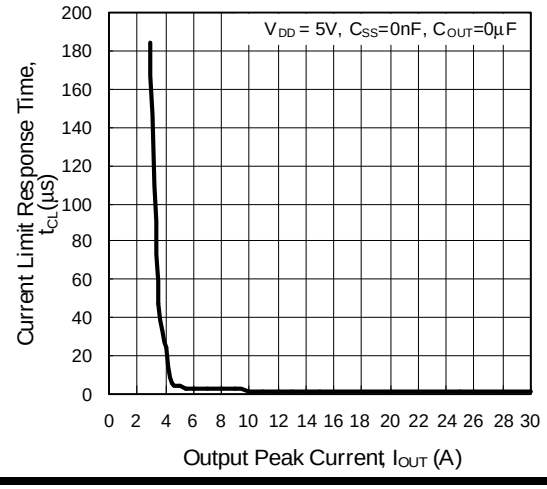
Current Limit Level vs. Junction Temperature



Current Limit Level vs. VIN Input Voltage



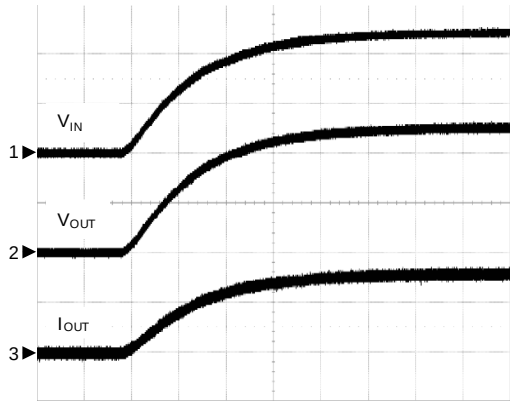
Current Limit Response Time vs. Output Peak Current



Operating Waveforms

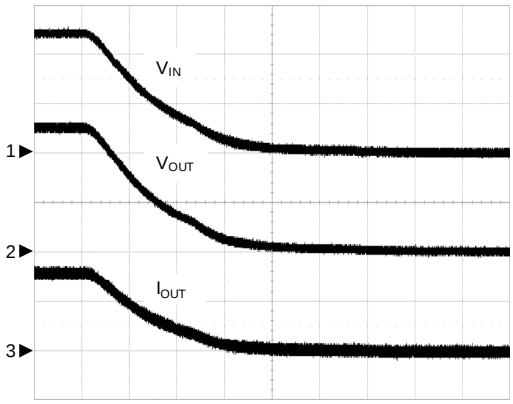
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

VIN Power On



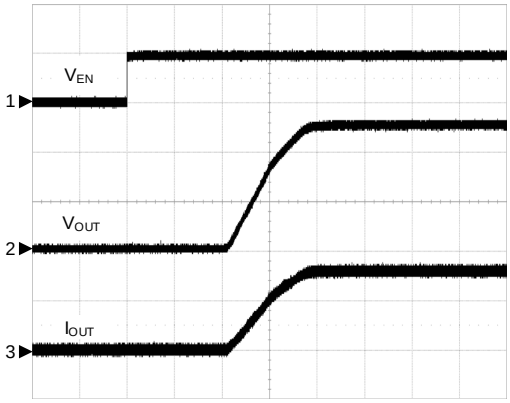
V_{DD}=5V, V_{EN}=5V
C_{SS}=1nF, R_L=3Ω
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

VIN Power Off



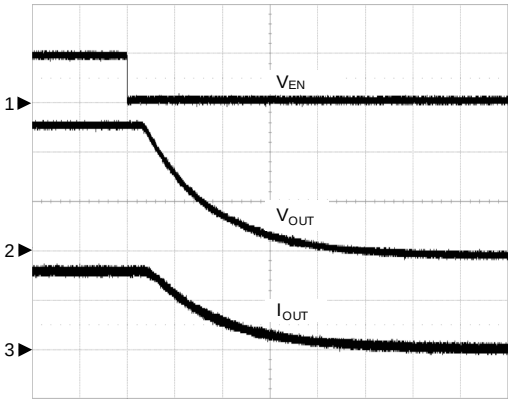
V_{DD}=5V, V_{EN}=5V
C_{SS}=1nF, R_L=3Ω
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

Enable



V_{DD}=5V, V_{IN}=5V
C_{SS}=1nF, R_L=3Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

Shutdown

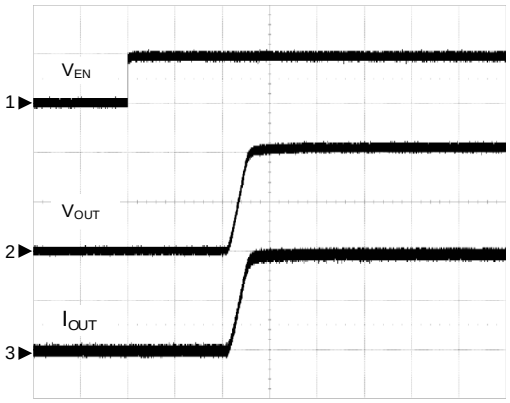


V_{DD}=5V, V_{IN}=5V
C_{SS}=1nF, R_L=3Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2µs/Div

Operating Waveforms(Cont.)

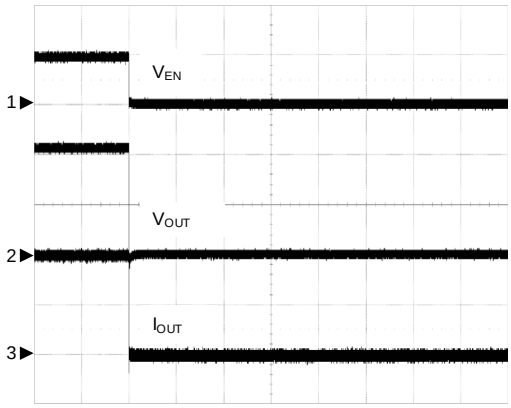
Refer to the typical application circuit. T_A= 25°C unless otherwise specified.

Enable



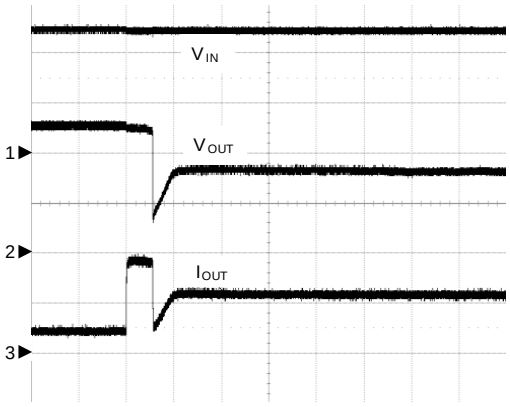
V_{DD}=3.3V, V_{IN}=1.05V
C_{SS}=1nF, R_L=0.5Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 0.5V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

Shutdown



V_{DD}=3.3V, V_{IN}=1.05V
C_{SS}=1nF, R_L=0.5Ω
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 0.5V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

Over Current Protection

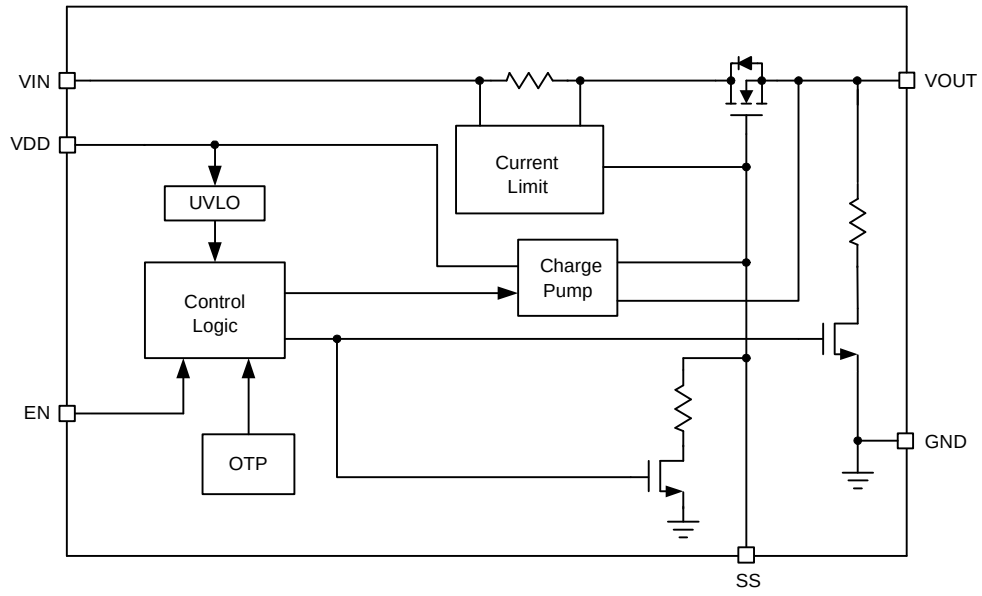


V_{DD}=5V, V_{EN}=5V
C_{SS}=0nF, R_L=5Ω to 1.5
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 2A/Div, DC
TIME: 100µs/Div

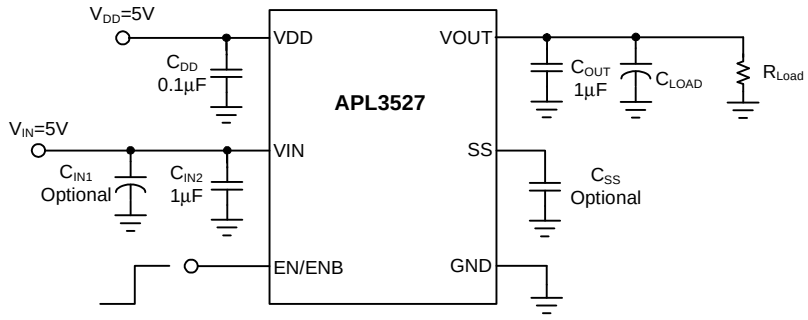
Pin Description

PIN		Function
NO.	NAME	
C1	VDD	VDD voltage input pin for internal control circuitry.
B1	EN	Enable input of switch. Logic high turns on switch. The EN pin cannot be left floating.
	ENB	Enable input of switch. Logic low turns on switch. The ENB pin cannot be left floating.
A1	VIN	Power supply Input of switch. Connect this pin to an external DC supply.
A2	VOUT	Switch output.
B2	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
C2	SS	Soft start control of switch. A capacitor from this pin to ground sets the VOUT's rise slew rate.

Block Diagram



Typical Application Circuits



Timing Chart

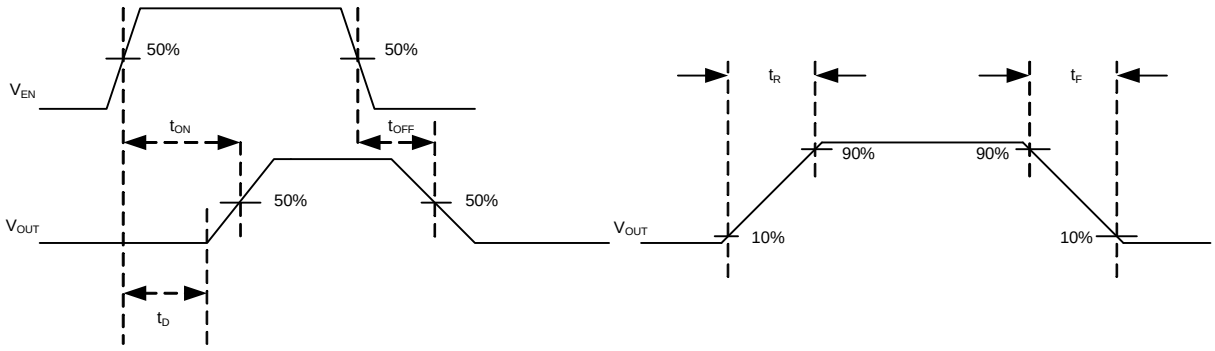


Figure 1. t_{ON}/t_{OFF}, t_R/t_F Waveforms

Soft Start

C_{SS}(pF)	Soft-Start Time (μs) Test Condition: V_{DD}=5V, C_{OUT}=1μF, C_{IN}=1μF, R_L=100Ω, Typical Values at T_A=25°C						
	V_{IN}=5V	V_{IN}=3.3V	V_{IN}=1.8V	V_{IN}=1.5V	V_{IN}=1.2V	V_{IN}=1.05V	V_{IN}=0.8V
0	95	60	39	30	26	24	20
220	385	235	131	109	85	84	62
330	524	308	171	141	116	103	79
470	783	433	250	207	164	150	116
1000	1461	854	469	388	324	285	222
2200	3250	1767	1026	839	681	592	472
4700	6900	4050	2294	1880	1552	1379	1062
10000	14280	7968	4888	3976	3180	2970	2216

C_{SS}(pF)	Soft-Start Time (μs) Test Condition: V_{DD}=3.3V, C_{OUT}=1μF, C_{IN}=1μF, R_L=100Ω, Typical values at T_A=25°C.					
	V_{IN}=3.3V	V_{IN}=1.8V	V_{IN}=1.5V	V_{IN}=1.2V	V_{IN}=1.05V	V_{IN}=0.8V
0	98	48	42	36	32	26
220	358	159	134	107	98	75
330	449	214	174	142	125	96
470	698	302	262	209	189	143
1000	1322	581	478	394	348	270
2200	2830	1257	1076	852	763	577
4700	6048	2714	2352	1851	1687	1312
10000	12100	5604	4432	3606	3208	2664

Turn on delay Time

C_{SS}(pF)	Turn on Delay Time (ms) Test Condition: C_{OUT}=1μF, C_{IN}=1μF, R_L=100Ω, Typical Values at T_A=25°C.	
	V_{DD}=V_{IN}=5V	V_{DD}=V_{IN}=3.3V
0	2.030	1.953
220	2.055	1.995
330	2.088	2.013
470	2.101	2.021
1000	2.162	2.101
2200	2.286	2.301
4700	2.536	2.696
10000	3.008	3.430

Note 4: The table Contains soft-start time values and turn on delay time values measured on a typical device. The soft-start times (t_R) and turn on delay times (t_D) shown are only valid for the power up sequence where V_{IN} and V_{DD} are already in steady state condition, and EN or ENB pin is asserted high or low.

Function Description

VIN Under-voltage Lockout (UVLO)

A under-voltage lockout (UVLO) circuit monitors the VDD pins voltage to prevent wrong logic controls. The UVLO function initiates a soft-start process after the VDD supply voltages exceed rising UVLO voltage threshold during powering on.

Current-Limit Protection

The APL3527 power switch provides the current-limit protection function. During current-limit, the devices limit output current at current-limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Soft-Start

The APL3527 Provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start time is set with a capacitor from the SS pin to the ground.

Over-Temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device¡¦s junction temperature cools by 30°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

A 1µF or higher ceramic bypass capacitor from VIN to GND, located near the APL3527, is strongly recommended to suppress the ringing during short circuit fault event.

When the load current trips the current limit threshold in an over load condition such as a short circuit, hot plug-in or heavy load transient the IC immediately turns off the internal power switch that will cause VIN ringing due to the inductance between power source and VIN. Without the bypass capacitor, the output short may cause sufficient ringing on the input to damage internal control circuitry.

Input capacitor is especially important to prevent V_{IN} from ringing too high in some applications where the inductance between power source to VIN is large (ex, an extra bead is added between power source line to VIN for EMI reduction), additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during over load conditions.

The recommended output capacitance of VOUT is 1µF at least. Please place the capacitors near the APL3527 as close as possible.

A bulk output capacitors, placed close to the load, is recommended to support load transient current.

Power Switch

The power switch is an N-channel MOSFET with a ultra-low $R_{DS(ON)}$. When IC is in shutdown state, the internal parasitic diodes connected from VOUT to VIN will be forward biased.

Thermal Consideration

The APL3527 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$P_{D(max)}$=(150-25)/100

= 1.25(W)

For normal operation, do not exceed the maximum operating junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

P_D=(125-25)/100

=1(W).....T_A=25°C

P_D=(125-85)/100

=0.4(W).....T_A=85°C

The power dissipation depends on operating ambient temperature for fixed T_J=125°C and thermal resistance θ_{JA}. For APL3527 packages, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

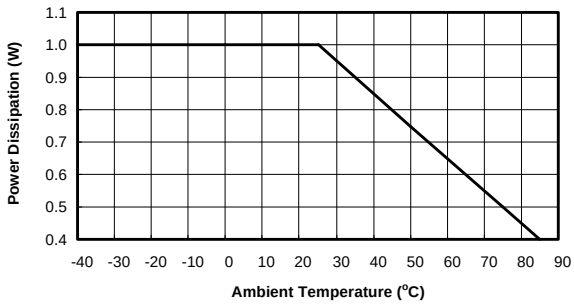
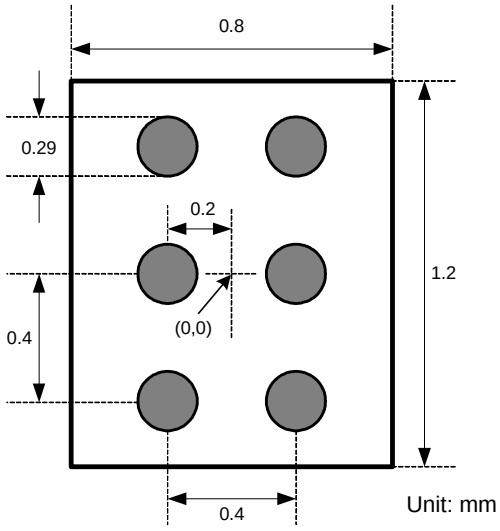


Figure 2. Derating Curves for APL3527 Package

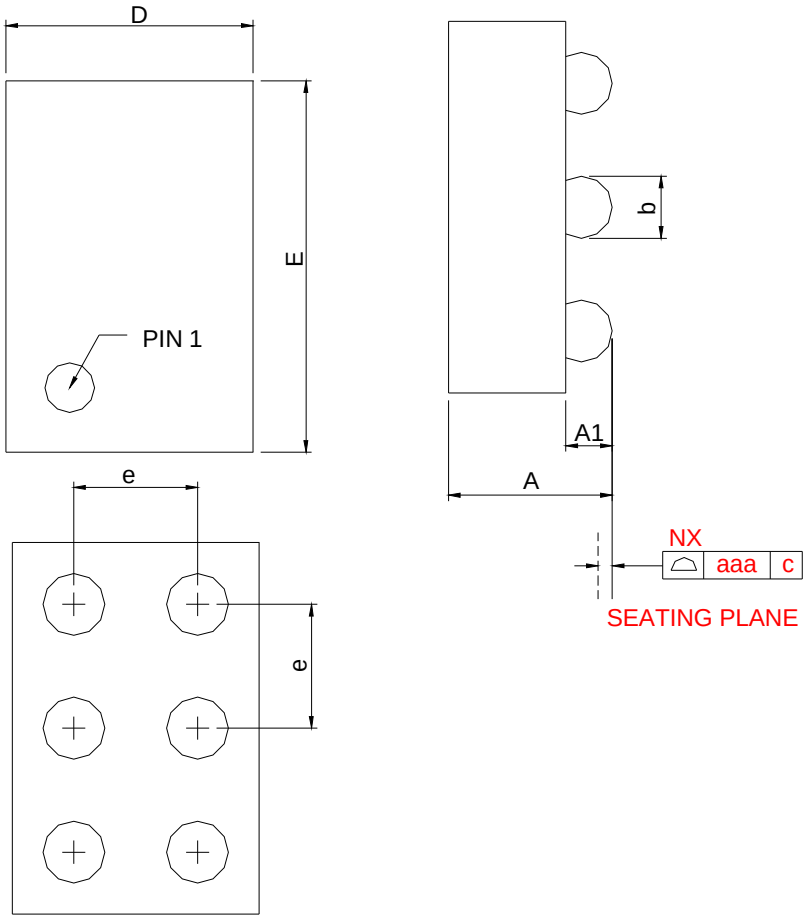
Recommended Minimum Footprint



WLCSP1.16x0.76-6

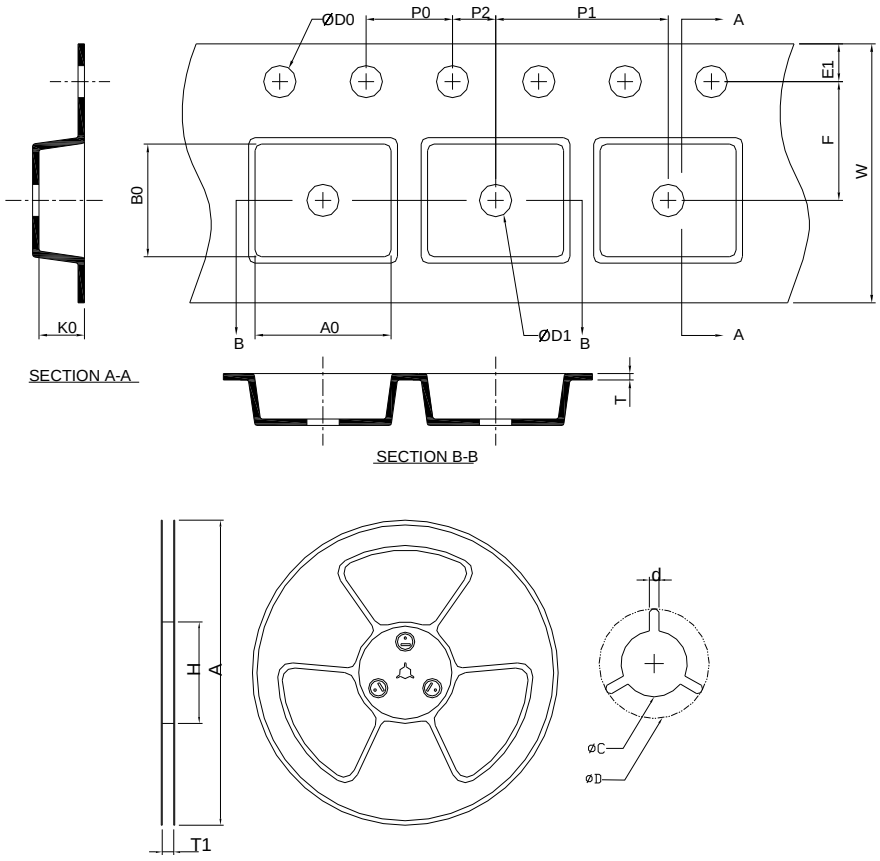
Package Information

WLCSP1.16x0.76-6



SYMBOL	WLCSP1.16*0.76-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.45	0.60	0.018	0.024
A1	0.15	0.25	0.006	0.010
b	0.23	0.29	0.009	0.011
D	0.76	0.82	0.030	0.032
E	1.16	1.22	0.046	0.048
e	0.40 BSC		0.016 BSC	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP (1.16x0.76)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.07±0.05	1.42±0.05	0.74±0.05

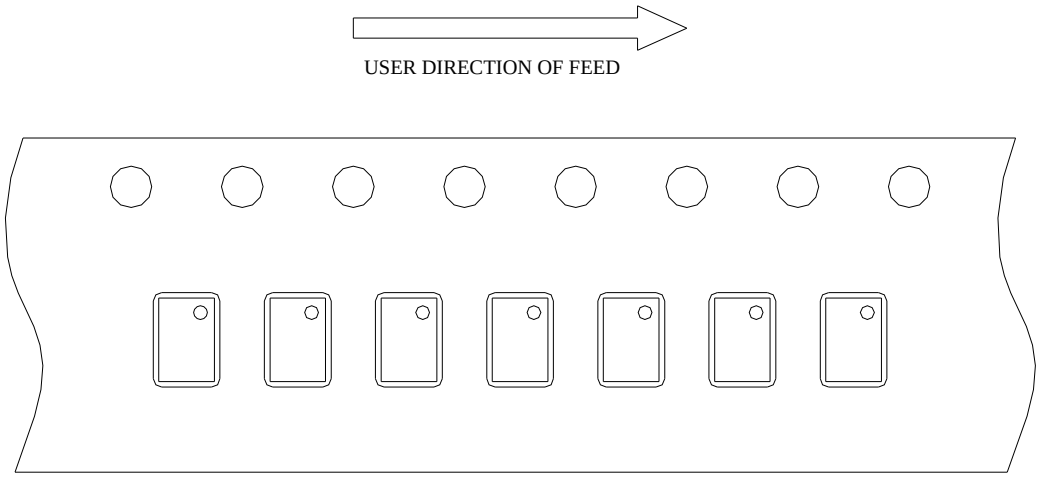
(mm)

Devices Per Unit

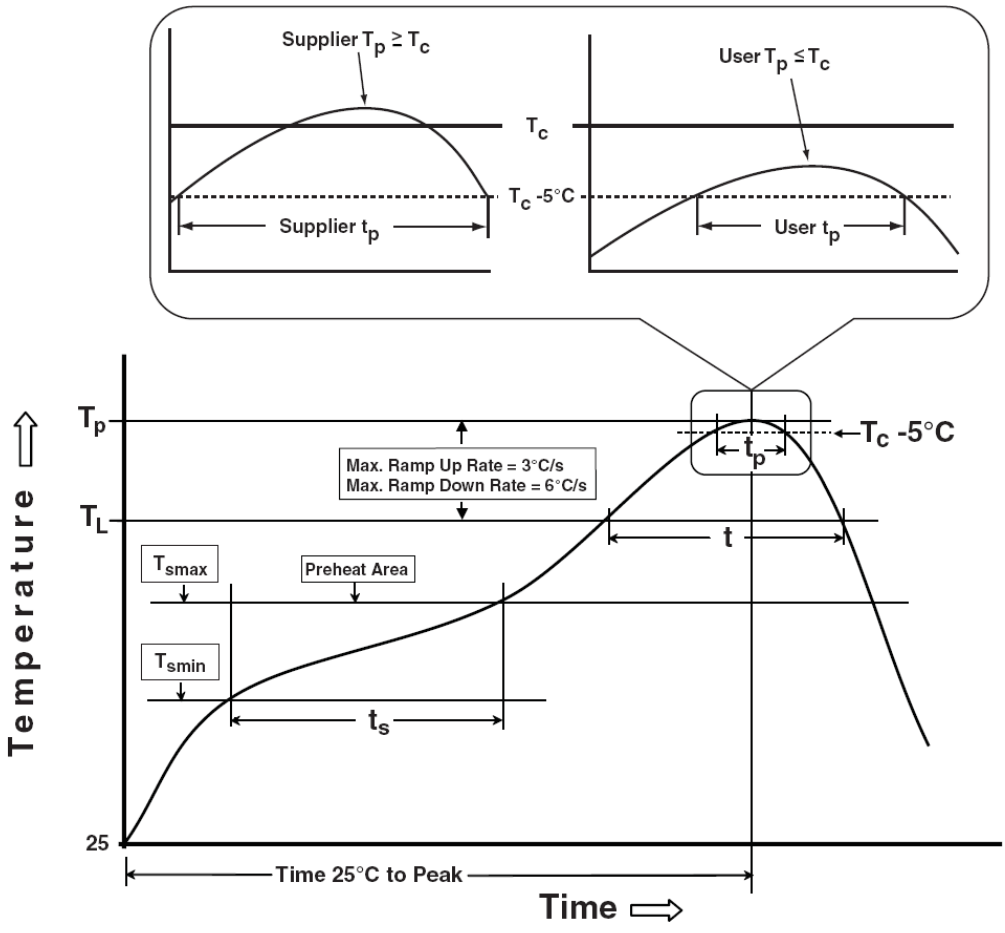
Package Type	Unit	Quantity
WLCSP1.16x0.76-6	Tape & Reel	3000

Taping Direction Information

WLCSP1.16x0.76-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838