Power-Distribution Switches with Soft Start

Features

- **84mΩ High Side MOSFET**
- **Soft Start Time Programmable by External Capacitor**
- **Wide Supply Voltage Range: 4.5V to 24V**
- **Current Limit Protections**
- **Under Voltage Lockout Protection**
- **Over- temperature Protection**
- **Logic Level Enable Input**
- **Lead Free and Green Devices Available (RoHS Compliant)**
- **Current Limit setting**

Applications

- **TFT LCD Modules**
- **Notebook and Desktop Computers**
- **USB Ports**
- **High-side Power Protection Switches**

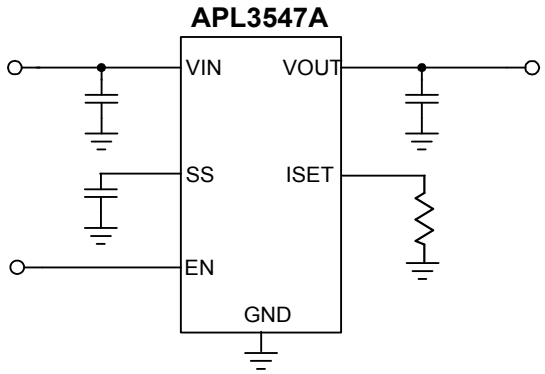
General Description

The APL3547A is a power-distribution switch with some protection functions. The device incorporates a N channel MOSFET power switch that is controlled by an enable logic pin and has a SS pin dedicated to soft start ramp-up rate control that can be used in application where the inrush current is concerned.

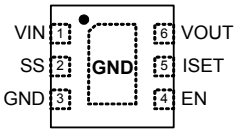
The device integrates some protection features, including current-limit protection, short-circuit protection, overtemperature protection, and UVLO. The current-limit and short-circuit protection can protect down-stream devices from catastrophic failure by limiting the output current at current-limit threshold during over-load or short-circuit events.When VOUT drops below VIN-1V, the devices limit the output current to a lower and safe level. The overtemperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 150°C and will automatically turns on the power switch when the temperature drops by 50°C. The UVLO function keeps the power switch in off state until there is a valid input voltage present. The current limit in APL3547A can be set by connecting resistor from the current limit adjustable pin ISET to ground.

The device is available in lead free SOP-8P and TDFN2x2-6 packages.

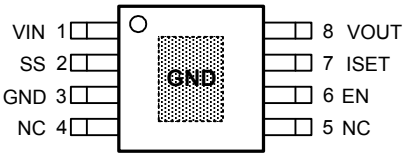
Simplified Application Circuit



Pin Configuration



TDFN2x2-6
(Top View)



SOP-8P
(Top View)

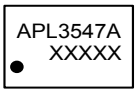
Ordering and Marking Information

APL3547A □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
KA : SOP-8P QB: TDFN2x2-6
Operating Ambient Temperature Range
I : -40°C to 80°C
Handling Code
TR : Tape & Real
Assembly Material
G : Halogen and Lead Free Device

APL3547A KA :



XXXXX - Date Code

APL3547A QB :

X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 26.5	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 26.5	V
V_{EN}	EN to GND Voltage	-0.3 ~ 7	V
V_{ISET}	ISET to GND Voltage	-0.3 ~ 7	V
V_{SS}	SS to GND Voltage	-0.3 ~ 7	V
I_{OUT}	IOUT output current	Setting by R_{ISET}	A
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air	SOP-8P	50	°C/W
		TDFN2x2-6	75	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	4.5 ~ 24	V
C_{SS_MIN}	Minimum SS Pin Soft-Start Capacitor	1	nF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{EN} =5V . Typical values are at T_A=25°C.

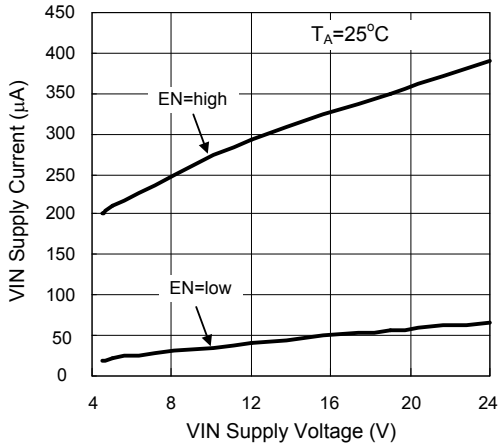
Symbol	Parameter	Test Conditions	APL3547A			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
	VIN Supply Current	No load, V_{EN}=0V	-	30	50	μA
		No load, V_{EN}=5V	-	250	400	μA
	Leakage Current	V_{OUT}=GND , V_{EN}=0V	-	-	1	μA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	I_{OUT}=2A, T_A= 25°C ,V_{IN}=12V	-	84	95	mΩ
		I_{OUT}=2A, V_{IN}=12V	-	84	105	mΩ
UNDER-VOLTAGE LOCKOUT						
	VIN UVLO Threshold Voltage	V_{IN} rising,	3.7	-	4.3	V
	VIN UVLO Hysteresis		-	0.25	-	V
CURRENT LIMIT AND SHORT CIRCUIT PROTECTIONS						
	Short Circuit Voltage Threshold		-	1	-	V
V_{ISET}	Current Limit Voltage		-	0.6	-	V
I_{OC}	Over Current Trip Threshold	R_{ISET}=82kΩ ,T_A=25°C	5.2	6.2	7.5	A
		R_{ISET}=330kΩ ,T_A=25°C	1.0	1.2	1.4	
	Over Current Trip Threshold Accuracy	R_{ISET}=82kΩ~330kΩ ,T_A=25°C	-20	-	+20	%
	Short Circuit Current		-	0.1	-	A
SOFT-START CONTROL PIN						
I_{SS}	SS Current	V_{IN}=12V,	1	2	3	μA
t_{SS}	Soft-Start Time	V_{IN}=12V, No load, C_{OUT}=1uF, C_{SS} =1nF	-	0.5	-	ms
		V_{IN}=12V, No load, C_{OUT}=1uF, C_{SS} =open	1	2	3	ms
	Soft-Start Discharge Resistance	V_{EN}=0V		250		Ω
EN INPUT PIN						
V_{IH}	Input Logic High		2	-	-	V
V_{IL}	Input Logic Low		-	-	0.6	V
	Input Current		-	-	1	μA
	VOUT Discharge Resistance	V_{EN}=0V	-	50	-	Ω
$t_{D(ON)}$	Turn on Delay Time		-	300	-	μs
$t_{D(OFF)}$	Turn off Delay Time		-	3	-	μs
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	150	-	C
	Over-Temperature Threshold Hysteresis	T_J falling	-	50	-	°C

Pin Description

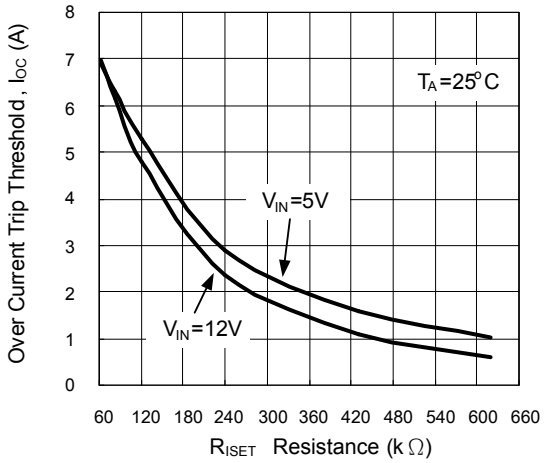
PIN		NAME	Description
SOP-8P	TDFN2x2-6		
1	1	VIN	Power Supply Input. Connect this pin to external DC supply.
2	2	SS	Soft Start Control Pin. Connect a capacitor to GND to control the soft start rate.
3, 9	3, 7	GND	GND.
4	-	NC	No connection.
5	-	NC	No connection.
6	4	EN	Enable Input. Pull this pin to high to enable the device and pull this pin to low to disable device. The EN pin cannot be left floating.
7	5	ISET	Connect a resistor to GND to adjust OCP level.
8	6	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When EN is low the output voltage is discharged by an internal resistor.

Typical Operating Characteristics

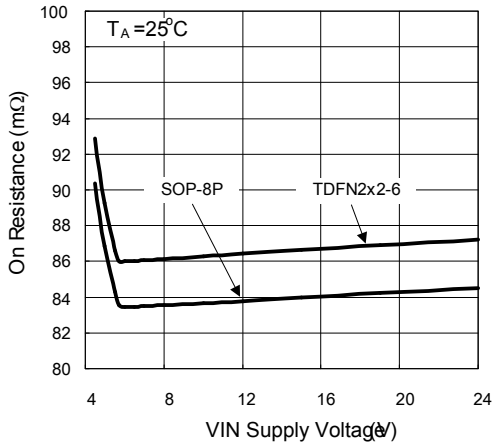
VIN Supply Current vs. VIN Supply Voltage



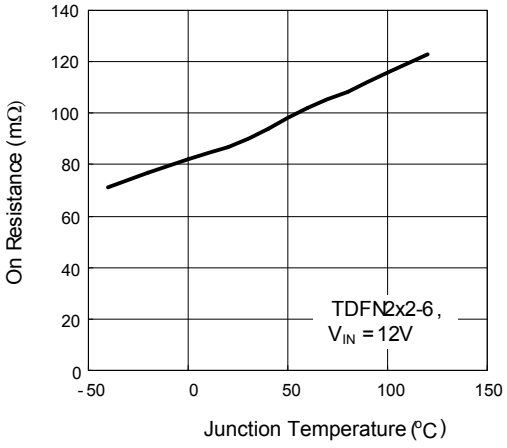
Over Current Trip Thrshold vsR$_{ISET}$ Resistance



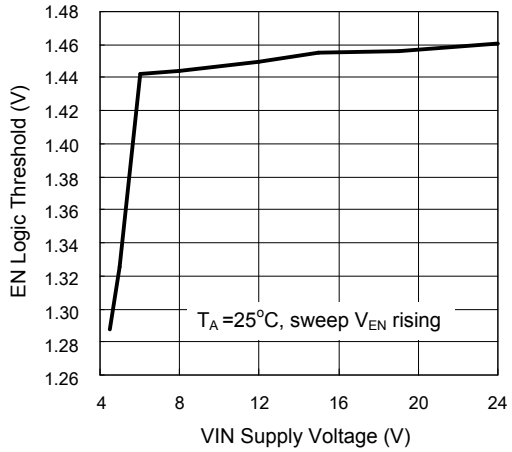
On Resistance vs VIN Supply Voltage



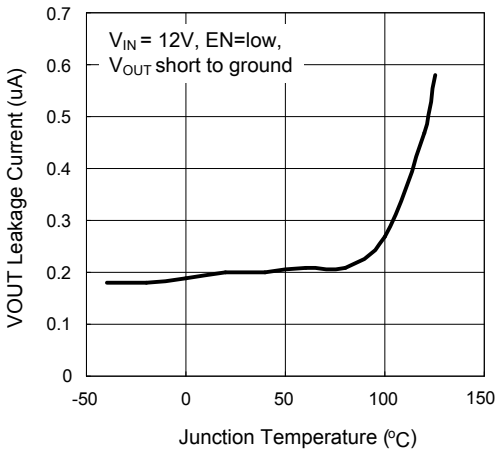
On Resistance vs Junction Temperature



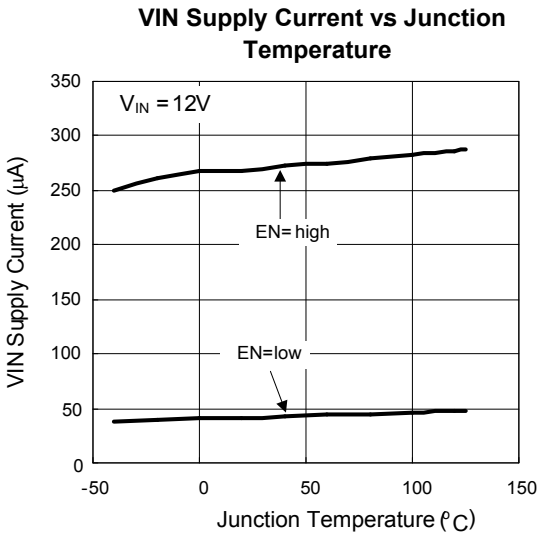
EN Logic Threshold Voltage vs. VIN Supply Voltage



VOUT Leakage Current vs. Junction Temperature



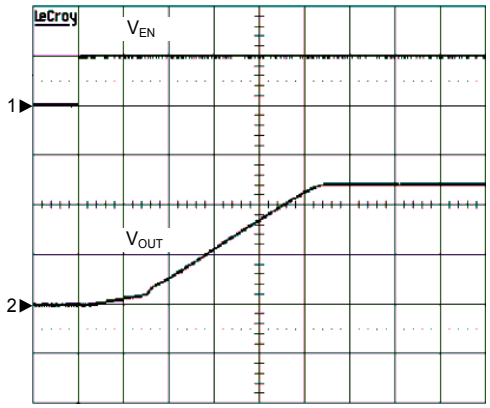
Typical Operating Characteristics



Operating Waveforms

The test condition T_A= 25°C unless otherwise specified.

Turn On Response



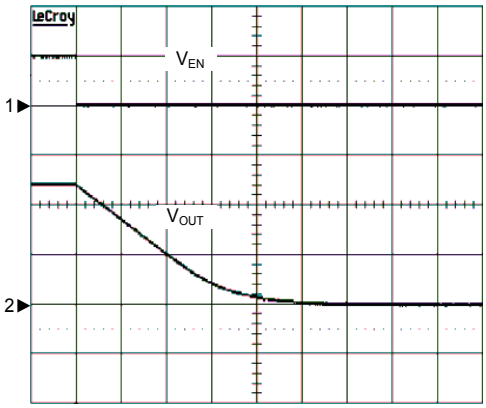
V_{IN} =12V, C_{IN} =10uF/MLCC, C_{OUT} =33µF/Electrolytic, No R_{LOAD}, C_{SS}=4.7nF

CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 5V/Div, DC

TIME: 1ms/Div

Turn Off Response



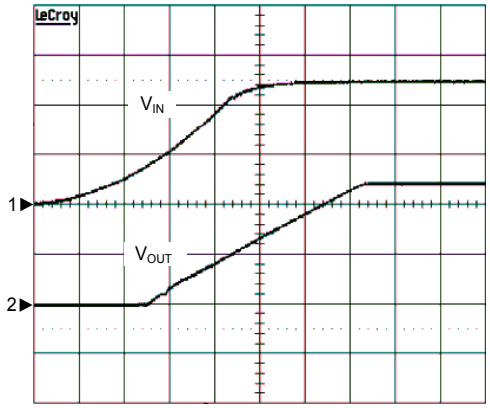
V_{IN} =12V, C_{IN} =10uF/MLCC, C_{OUT} =33µF/Electrolytic, No R_{LOAD}, C_{SS}=4.7nF

CH1: V_{EN}, 5V/Div, DC

CH2: V_{OUT}, 5V/Div, DC

TIME: 2ms/Div

UVLO at Rising



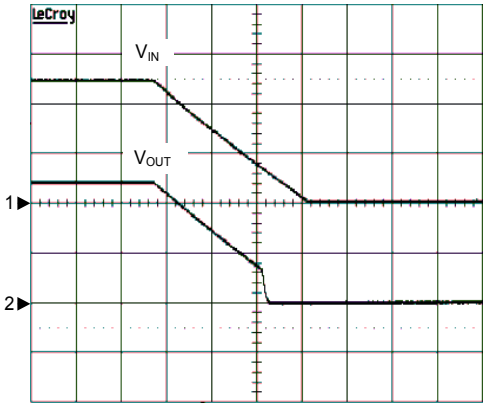
V_{IN} =12V, C_{IN} =10uF/MLCC, C_{OUT} =33µF/Electrolytic, No R_{LOAD}, C_{SS}=47nF

CH1: V_{IN}, 5V/Div, DC

CH2: V_{OUT}, 5V/Div, DC

TIME: 5ms/Div

UVLO at Falling



V_{IN} =12V, C_{IN} =10uF/MLCC, C_{OUT} =33µF/Electrolytic, No R_{LOAD}, C_{SS}=47nF

CH1: V_{IN}, 5V/Div, DC

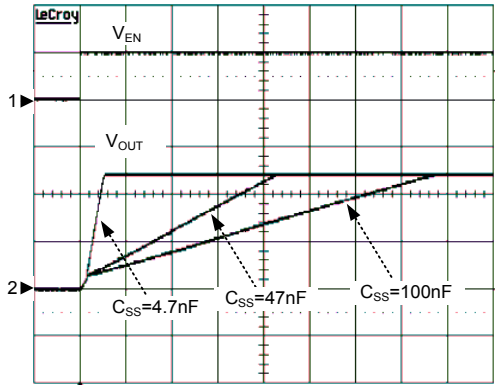
CH2: V_{OUT}, 5V/Div, DC

TIME: 5ms/Div

Operating Waveforms

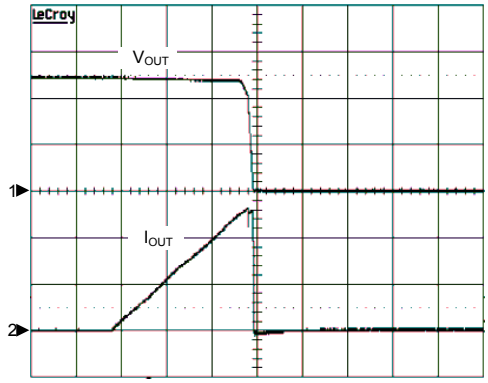
The test condition T_A= 25°C unless otherwise specified.

Softstart with Different C_{SS} Capacitor



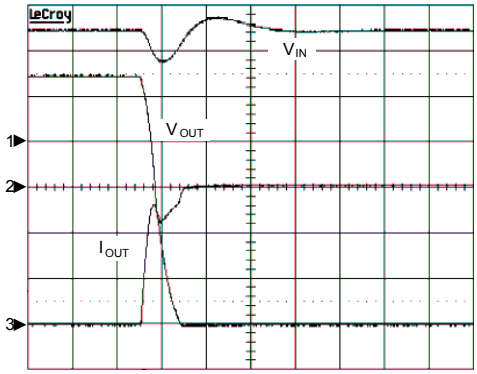
V_{IN} =12V, C_{IN} =10uF/MLCC, C_{OUT} =33µF/Electrolytic, No R_{LOAD}, C_{SS}=4.7/47/100nF
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 5V/Div, DC
TIME: 10ms/Div

Over Current Response with Ramped Load



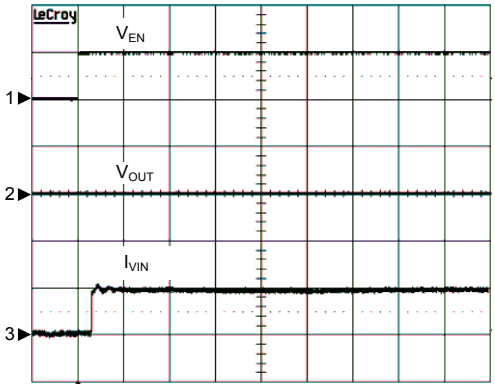
V_{IN} =12V, C_{IN}= 10uF/MLCC, C_{OUT} =33µF/ Electrolytic, R_{ISET}=200kΩ
CH1: V_{OUT}, 5V/Div, DC
CH2: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

Short Circuit Response



V_{IN} =12V, C_{IN} =47uF/ MLCC, C_{OUT} =1µF/ MLCC, R_{ISET}=200kΩ, V_{EN} =5V, VOUT short to ground
CH1: V_{IN}, 5V/Div, DC
CH2: V_{OUT}, 5V/Div, DC
CH3: I_{OUT}, 10A/Div, DC
TIME: 2µs/Div

Device Enabled into Short Circuit

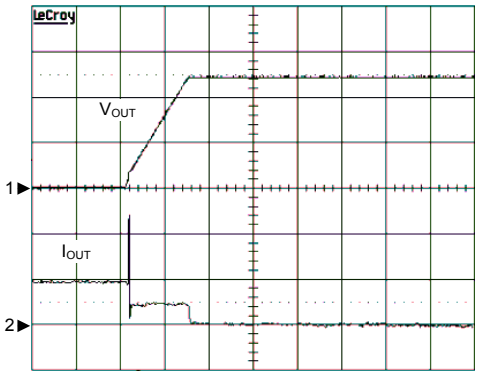


V_{IN} =12V, C_{IN} =10uF/MLCC,
VOUT short to ground then EN power on
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 5V/Div, DC
CH3: I_{VIN}, 100mA/Div, DC
TIME: 1ms/Div

Operating Waveforms

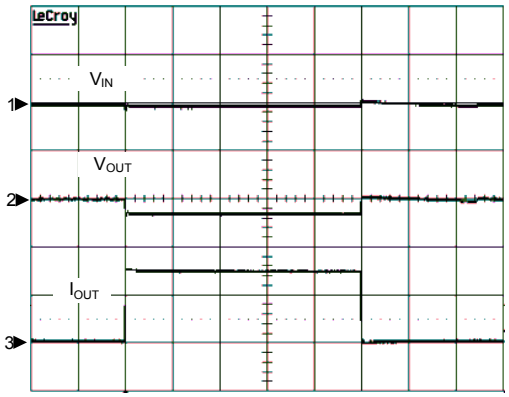
The test condition T_A= 25°C unless otherwise specified.

Short Circuit Release



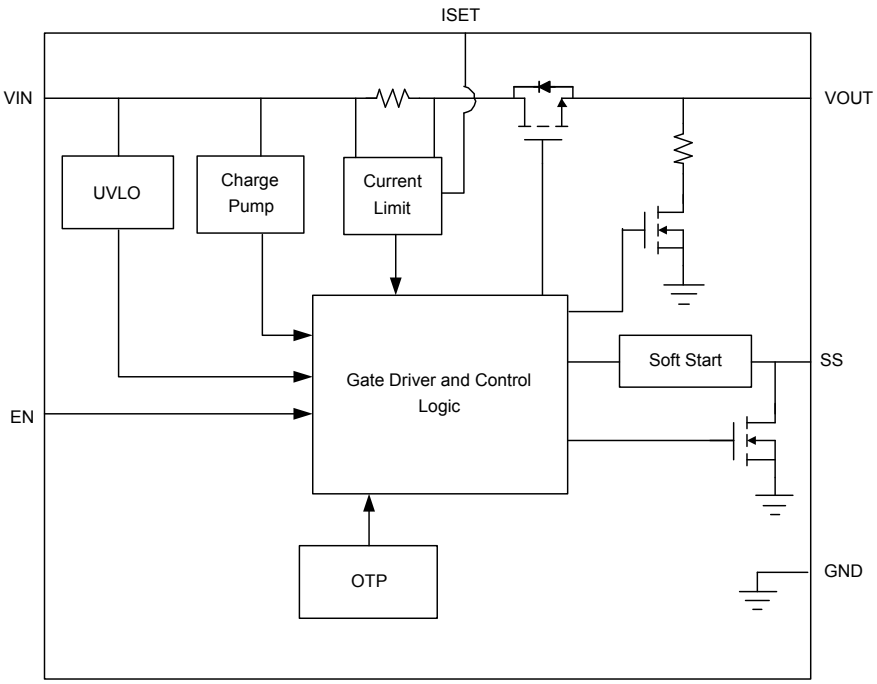
V_{IN}=12V, C_{IN}=10uF/MLCC,
C_{OUT}=120μF/Electrolytic, No R_{LOAD}, C_{SS}=47nF
CH1: V_{EN}, 5V/Div, DC
CH2: I_{OUT}, 100mA/Div, DC
TIME: 20ms/Div

Load Transient

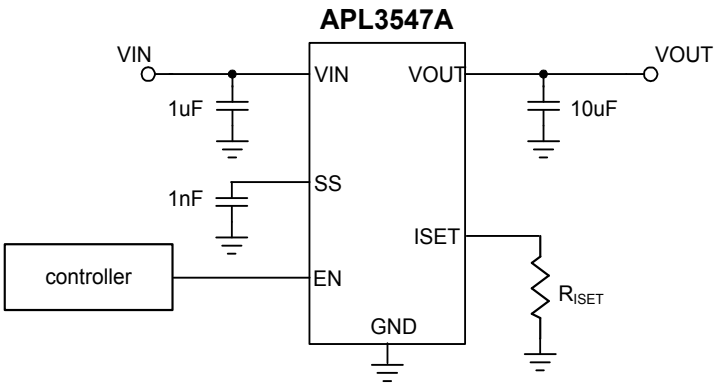


V_{IN}=12V, C_{IN}=120uF/ Electrolytic,C_{OUT}
=33μF/ Electrolytic,R_{ISET}=200kΩ,I_{OUT}=0-3-0A
CH1 : V_{IN}, 1V/Div, Offset=12V
CH2 : V_{OUT}, 1V/Div, Offset=12V
CH3 : I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

Block Diagram



Typical Application Circuit



Function Description

Under-voltage Lockout (UVLO)

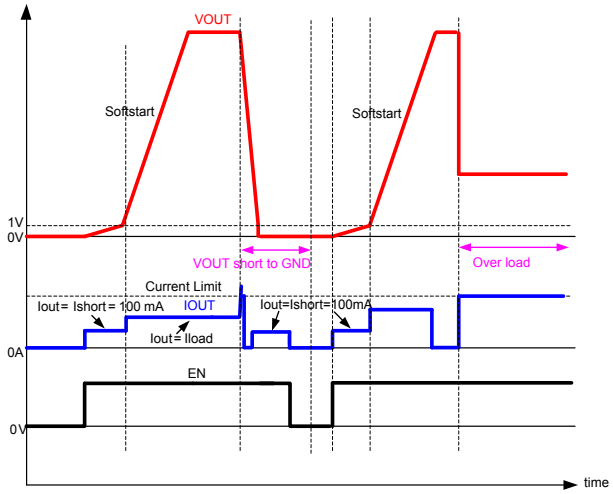
The APL3547A power switch is built-in an under-voltage lockout circuit to keep the output shuts off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Current Limit Protection

The APL3547A power switch provides the current limit protection. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Short Circuit Protection

When the output voltage drops below VIN-4V, which is caused by the over load or short-circuit, or at the very beginning of the softstart when VOUT<1V, the devices limit the output current down to a safe level. The short circuit current-limit is used to reduce the power dissipation during short-circuit condition. If the junction temperature is over the thermal shutdown temperature, the device will enter the thermal shutdown.



Soft-Start

The APL3547A provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start ramp-up rate is controlled by a capacitor from SS pin to ground. the soft start time can be calculated by this following equation:

$t_{SS} = 0.1(C_{SS} \times V_{IN})/I_{SS}$

where,
tSS is soft start time of VOUT rising from 0 to 100%, of which unit is second.
C_{SS} is the value of the capacitor connected from SS pin to GND, of which unit is micro-Farad.
V_{IN} is the amplitude of input voltage applied to this device, of which unit is volt.
I_{SS} is the SS pin charge current.
If the SS pin is left floating the soft start time is 2ms when V_{IN}=12V.

Enable/Disable

Pull the EN below 0.6V to disable the device and pull EN above 2V to enable the device. When the IC is disabled the supply current is reduced to less than 30μA. The enable input is compatible with both TTL and CMOS logic levels. The EN pin cannot be left floating.

Over-Temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 50°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over-temperature conditions. For normal operation, the junction temperature cannot exceed T_J=125°C.

Application Information

Input Capacitor

A 1μF or higher ceramic bypass capacitor from VIN to GND, located near the APL3547A, is strongly recommended to suppress the ringing during over-load or short-circuit fault event. Without the bypass capacitor, the over-load or output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry. Input capacitor is especially important to prevent VIN from ringing too high in some applications where the inductance between power source to VIN is large due to poor PCB layout or purposely adding an inductive component in front of VIN pin.

When the VIN's supply voltage is higher, say 19V or 24V, it is required to add some adequate amount of capacitance of input capacitor into VIN pin for overshoot suppression because a slight ringing of VIN is most likely to exceed VIN's absolute maximum rating, or else the device could be burnout during over load conditions.

Output Capacitor

A low-ESR 10μF MLCC, aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1μF ceramic capacitor improves the immunity of the device to short-circuit transients.

Soft-Start Capacitor

The APL3547A has a built-in adjustable soft-start control for user to set an optimum soft-start time for the application. The soft-start time can be calculated by the equation, described in the paragraph of Soft-Start in Functional Description section. Please note that there is minimum value of soft start capacitor in different VIN input voltage. Please make sure the C_{SS} is in the recommended value.

Current Limit Setting

The current limit can be set by connecting resistor from the current limit adjustable pin ISET to ground. The required value of resistor RISET for current limit is calculated as follows:

$R_{ISET} = 510000 / I_{LIM}$

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.

2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high frequency ripples.

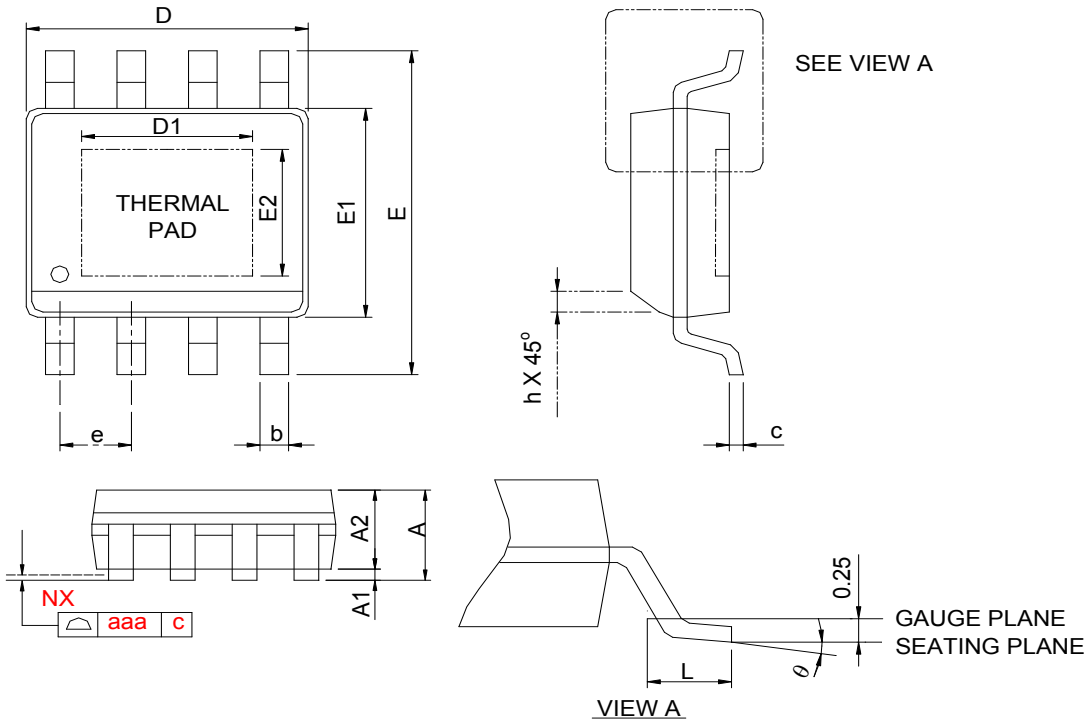
3. Locate APL3547A and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.

4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.

5. Keep VIN and VOUT traces as wide and short as possible.

Package Information

SOP-8P

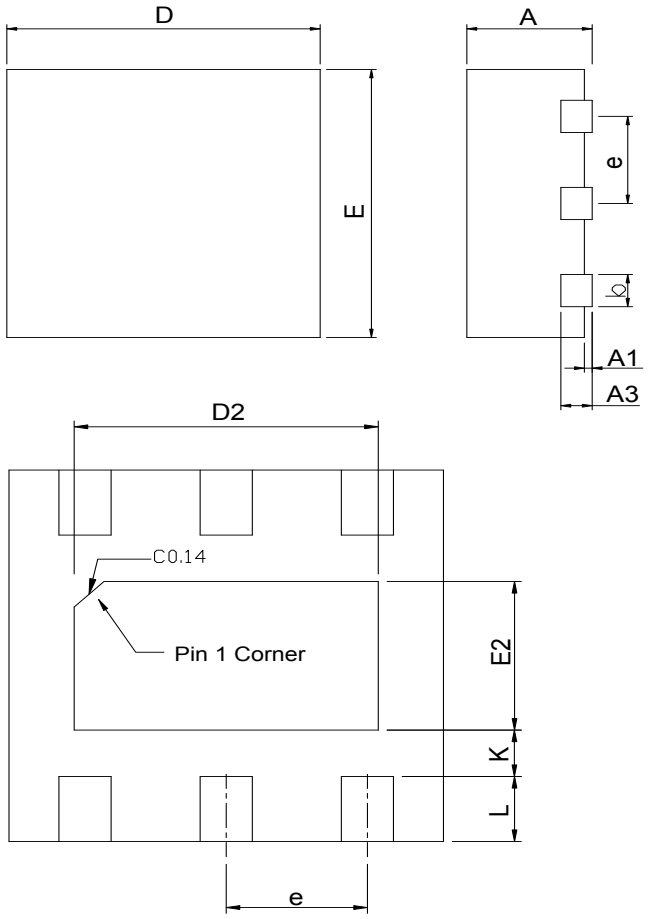


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C
aaa	0.10		0.004	

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

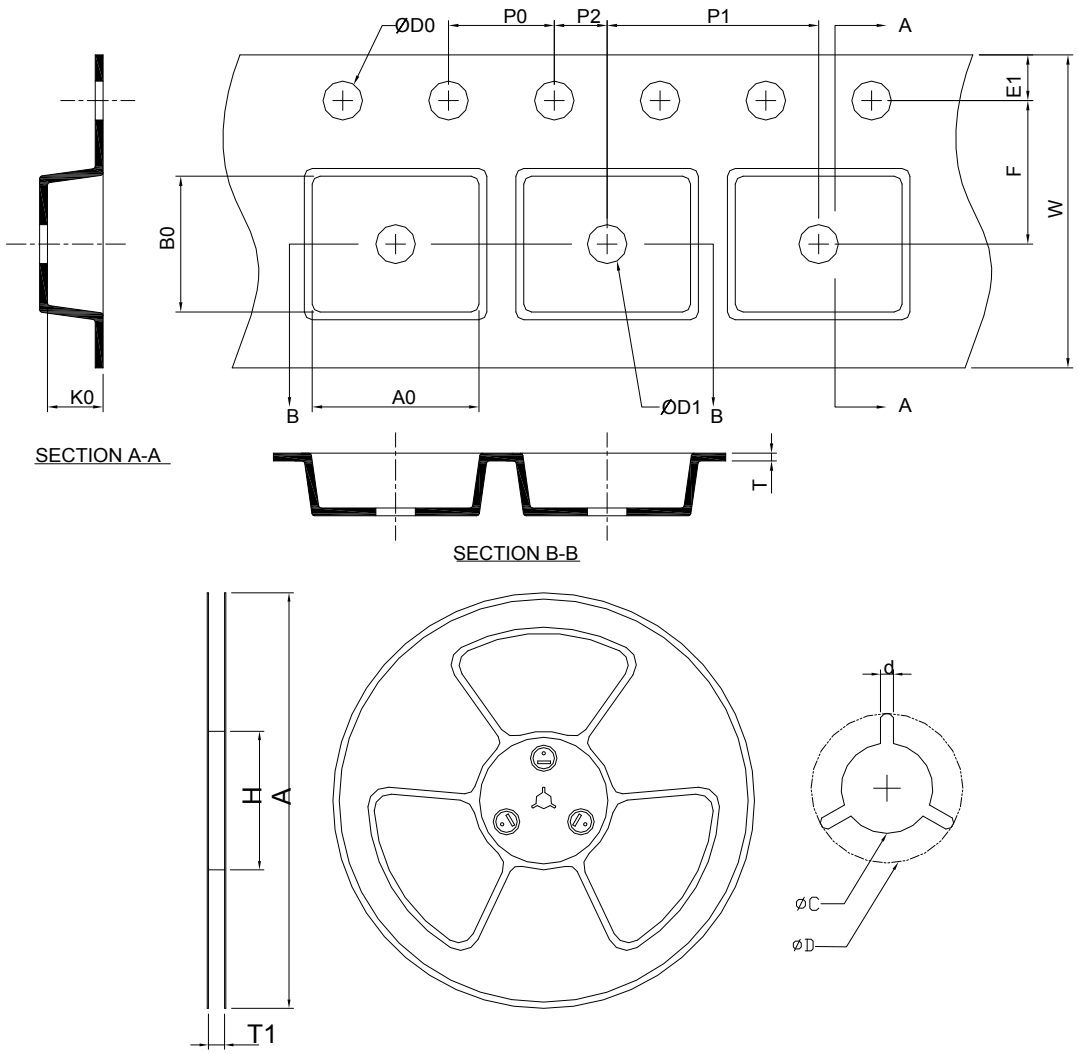
TDFN2x2-6



SYMBOL	TDFN2*2-6					
	MILLIMETERS			INCHES		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.03	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.24	0.30	0.007	0.009	0.012
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.00	1.30	1.60	0.039	0.051	0.063
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.60	0.80	1.00	0.024	0.031	0.039
e	0.65 BSC			0.026 BSC		
L	0.30	0.38	0.45	0.012	0.015	0.018
K	0.20			0.008		

Note : 1. Followed from JEDEC MO-229 WCCC.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.55±0.20	5.25±0.20	2.10±0.20

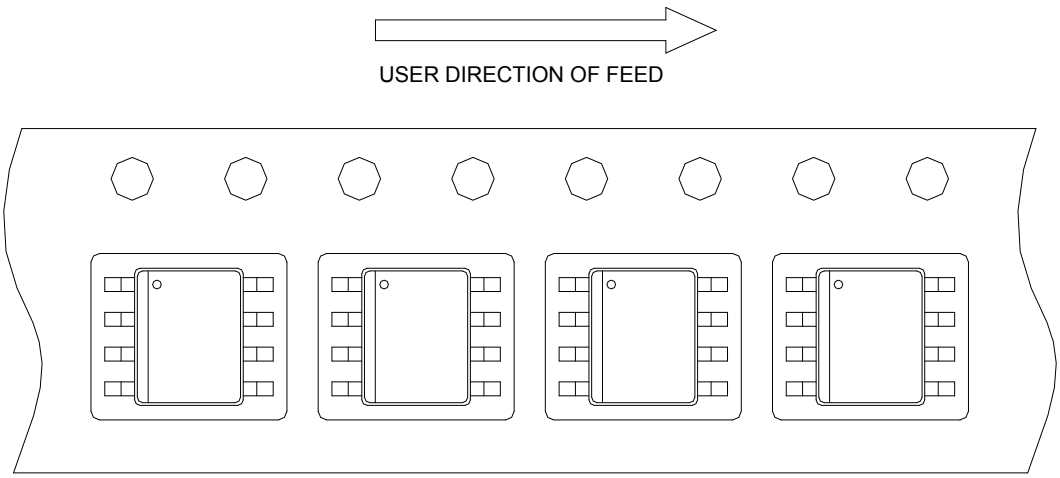
(mm)

Devices Per Unit

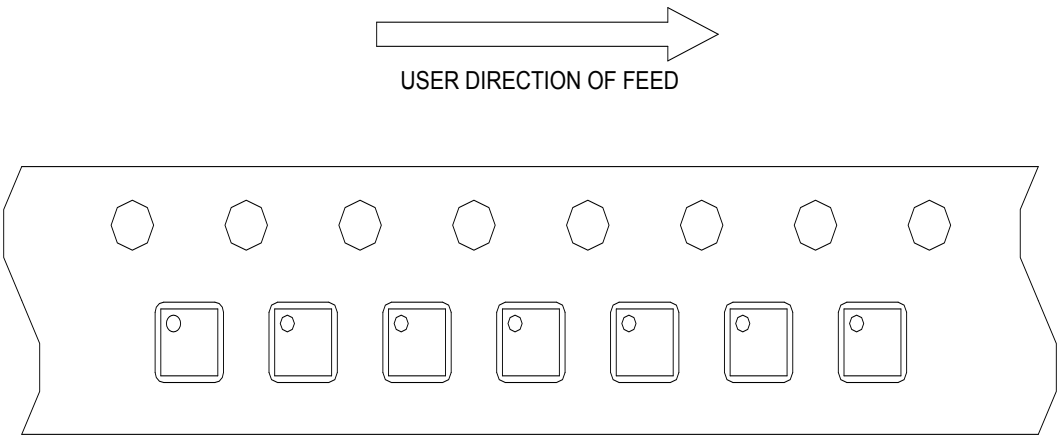
Package Type	Unit	Quantity
TDFN2x2	Tape & Reel	3000
SOP-8P	Tape & Reel	2500

Taping Direction Information

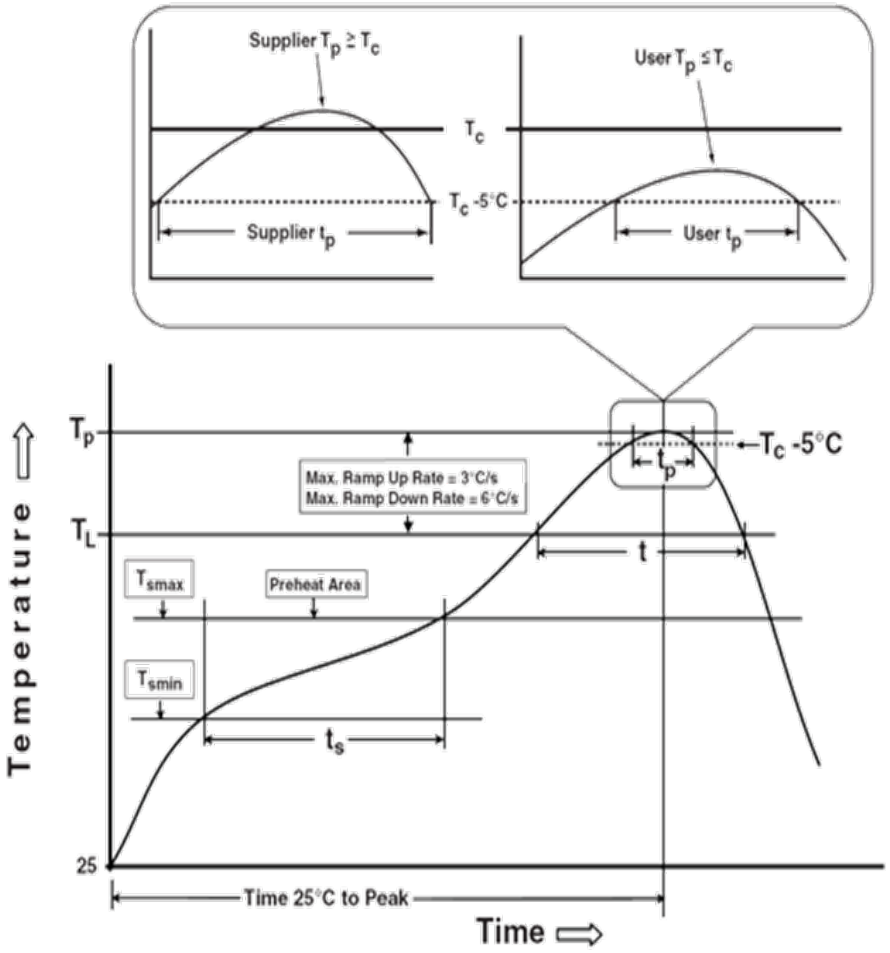
SOP-8P



TDFN2x2-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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