Single Channel Power-Load Switch

Features

- **Low On-resistance at VIN =3.3V : 35mΩ(typ.) 40mΩ(max.)**
- **Low Quiescent Current: 40μA (max.)**
- **VIN Supply Voltage Range: 2.7V to 4V**
- **Current Limit Protection**
- **Over-Temperature Protection**
- **Under Voltage Lockout Protection**
- **Reverse Current Blocking when Disabled**
- **Deglitched Fault IndicationOutput**
- **Internal Soft Start Control**
- **Output Discharge when Switch Disabled (APL3570A/C)**
- **No Output Discharge Function (APL3570B/D)**
- **Logic Level Enable Input**
- **Lead Free and Green Devices Available (RoHS Compliant)**
- **UL Approved-File No. E328191**
- **UL IEC/EN62368-1 CB Scheme Certified, No. DK-73439-UL**
- **TUV IEC/EN62368-1 Certified, No. 44 780 18 406748-006**

General Description

The APL3570 series are 35mΩ(3.3V input) high side load switches with an EN logic input and an OCB fault indication output.

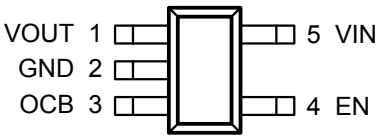
The protection features include current-limit protection and over-temperature protection. The current-limit protection can protect down stream devices from catastrophic failure by limiting the output current at current limit threshold during over-load or short-circuit events. The over temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 150°C and will automatically turns on the power switch when the temperature drops by 30°C.

The device is available in lead free TDFN2X2-8 and SOT-23-5 packages.

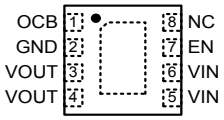
Applications

- **Notebook and Desktop Computers**
- **High-Side Power Protection Switchs**

Pin Configuration



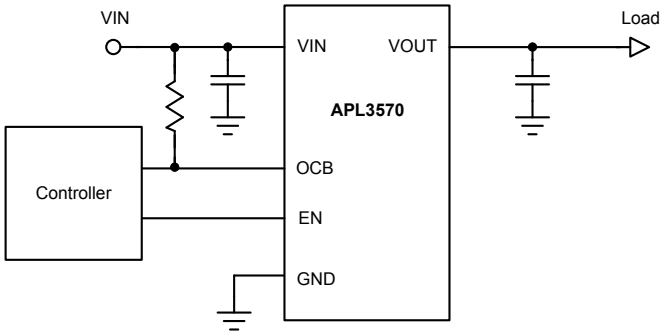
SOT-23-5
(Top View)



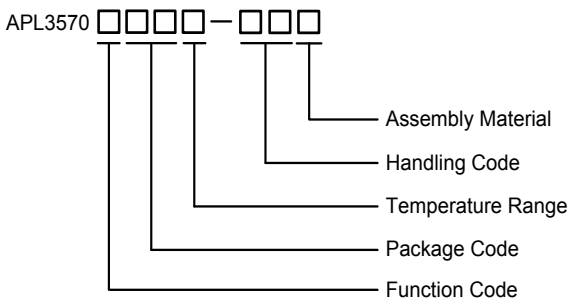
TDFN2X2-8
(Top View)

= Exposed Pad (connected to ground plane for better heat dissipation)

Simplified Application Circuit



Ordering and Marking Information



Function Code
A : Output Current 1A / Built in VOUT discharge function
B : Output Current 1A / VOUT discharge function is disabled
C : Output Current 2A / Built in VOUT discharge function
D : Output Current 2A / VOUT discharge function is disabled
Package Code
B : SOT23-5 QB : TDFN2x2-8
Operating Junction Temperature
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL3570A B:	70AX	X - Date Code
APL3570B B:	70BX	X - Date Code
APL3570C B:	70CX	X - Date Code
APL3570D B:	70DX	X - Date Code
APL3570A QB:	L70A ● X	X - Date Code
APL3570B QB:	L70B ● X	X - Date Code
APL3570C QB:	L70C ● X	X - Date Code
APL3570D QB:	L70D ● X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 4.5	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 4.5	V
V_{EN}	EN to GND Voltage	-0.3 ~ 4.5	V
V_{OCB}	OCB to GND Voltage	-0.3 ~ 4.5	V
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under“recommended operating conditions”is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)		°C/W
	SOT-23-5	100	
	TDFN2x2-8	75	
θ_{JC}	Junction-to-Case Resistance in free air		°C/W
	SOT-23-5	50	
	TDFN2x2-8	13	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 4	V
I_{OUT}	VOUT Output Current		A
	APL3570A/B	0 ~ 1	
	APL3570C/D	0 ~ 2	
V_{EN_H}	EN Logic High Input Voltage	1.2 ~ V_{IN}	V
V_{EN_L}	EN Logic Low Input Voltage	0 ~ 0.4	V
C_{IN}	Input Capacitor	10 ~ 330	µF
C_{OUT}	Output Capacitor	10 ~ 330	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

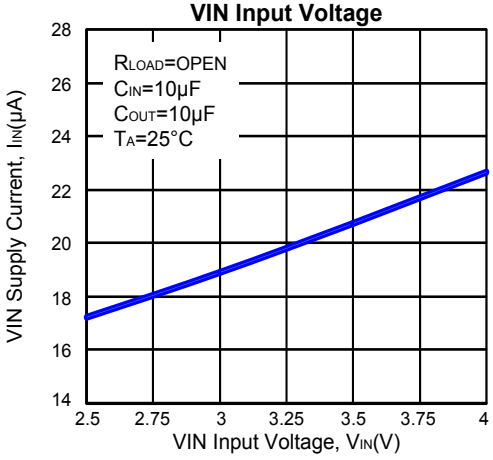
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.3V, V_{EN}=3.3V or and T_A= -40 to 85°C. Typical values are at T_A=25°C.

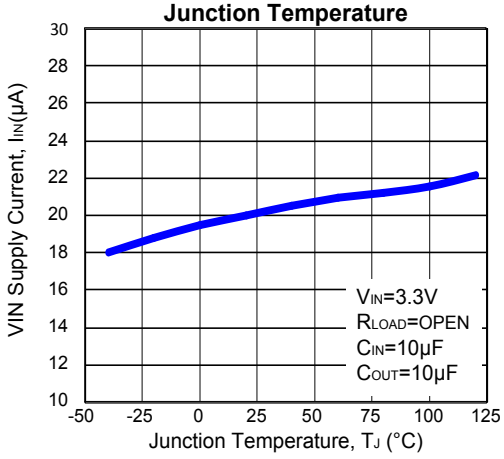
Symbol	Parameter	Test Conditions	APL3570			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{IN}	VIN Supply Current	V_{IN}=3.3V, No load	-	19	25	μA
		V_{IN}=4V, No load	-	25	40	μA
I_{SD}	VIN Off-State Supply Current	V_{IN}=2.7V to 4V, V_{EN}=0V, T_A= 25°C	-	0.1	1	μA
		V_{IN}=2.7V to 4V, V_{EN}=0V	-	0.1	3	μA
	VOUT Leakage Current	V_{IN}=2.7V to 4V, V_{EN}=0V, V_{OUT}=0V, T_A = 25°C	-	0.1	1	μA
		V_{IN}=2.7V to 4V, V_{EN}=0V, V_{OUT}=0V	-	0.1	3	μA
I_{RV}	Reverse Leakage Current	V_{IN}=0V, V_{EN}=0V, V_{OUT}=2.7V to 4V, T_A = 25°C	-	0.1	1	μA
		V_{IN}=0V, V_{EN}=0V, V_{OUT}=2.7V to 4V	-	0.1	3	μA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	V_{IN}=2.7V to 4V, I_{OUT}=1A, T_A = 25°C	-	35	40	mΩ
		V_{IN}=3.3V, I_{OUT}=1A	-	-	45	mΩ
		V_{IN}=4V, I_{OUT}=1A	-	-	40	mΩ
UNDER-VOLTAGE LOCKOUT (UVLO)						
	VIN UVLO Threshold Voltage	V_{IN} rising, T_A=25°C	2	2.2	2.4	V
	VIN UVLO Hysteresis		-	0.1	-	V
CURRENT LIMIT AND SHORT CIRCUIT PROTECTIONS						
I_{LIM}	Current Limit Threshold **(APL3570A/B)**	V_{IN}=2.7V to 4V	1.1	-	2.2	A
	Current Limit Threshold **(APL3570C/D)**	V_{IN}=2.7V to 4V	2.1	-	2.7	A
I_{SC}	Fold-back Current Limit Threshold **(APL3570A/B)**	V_{OUT} < V_{IN}-1.3V, V_{IN}=2.7V to 4V	0.2	0.7	-	A
	Fold-back Current Limit Threshold **(APL3570C/D)**	V_{OUT} < V_{IN}-1.3V, V_{IN}=2.7V to 4V	0.6	1.5	-	A
t_B	Fold-back Current Limit Blanking Time	From beginning of soft-start, V_{IN}=2.7V to 4V	-	1.7	-	ms
OCB OUTPUT PIN						
	OCB Output Low Voltage	I_{OCB}=5mA	-	-	0.4	V
	OCB Input Leakage Current	V_{OCB}=4V	-	-	1	μA
$t_{D(OCB)}$	OCB Deglitch Time	OCB assertion	-	3.2	-	ms
EN INPUT PIN						
V_{EN_H}	EN Input Logic High	V_{IN}=2.7V to 4V	1.2	-	-	V
V_{EN_L}	EN Input Logic Low	V_{IN}=2.7V to 4V	-	-	0.4	V
	EN Input Current		-	-	1	μA
	VOUT Discharge Resistance **(APL3570A/C)**	V_{EN}=0V, VOUT force 1V	-	100	150	Ω
$t_{D(ON)}$	Turn on Delay Time	V_{IN}=3.3V, from EN rising threshold to V_{OUT} 90%	-	250	-	μs
		V_{IN}=4V, from EN rising threshold to V_{OUT} 90%	-	250	-	μs
$t_{D(OFF)}$	Turn off Delay Time **(APL3570 A/C)**		-	8	-	μs
t_{SS}	Soft-Start Time	No load, C_{OUT}=1μF, V_{IN}=3.3V	-	100	-	μs
		No load, C_{OUT}=1μF, V_{IN}=4V	-	100	-	μs
OVERT-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold (Note 4)	T_J rising	-	150	-	°C
	Over-Temperature Hysteresis (Note 4)		-	30	-	°C

Typical Operating Characteristics

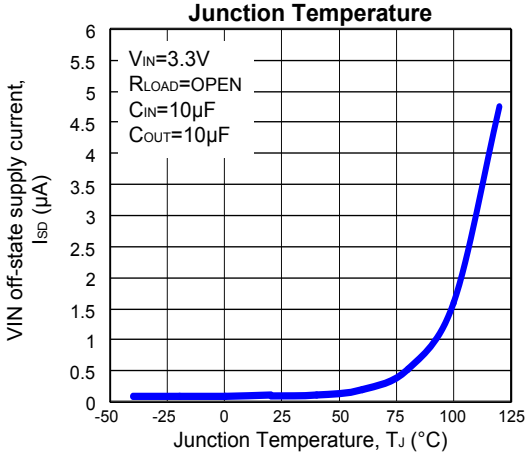
VIN Supply Current vs. VIN Input Voltage



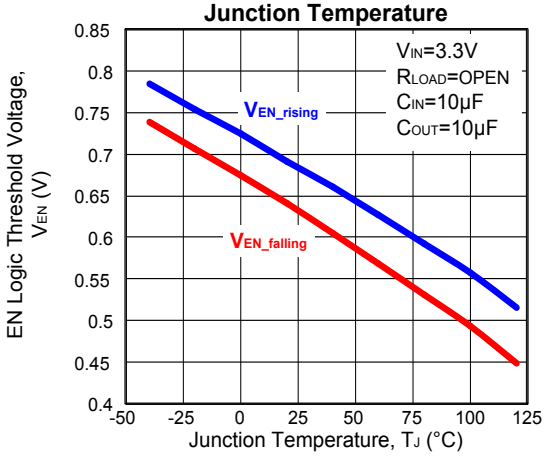
VIN supply current vs. Junction Temperature



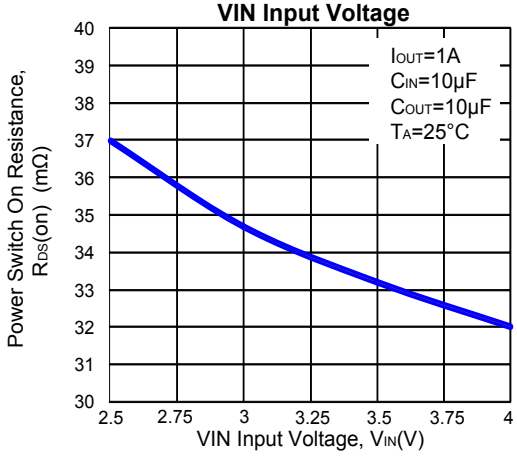
VIN off_state supply current vs. Junction Temperature



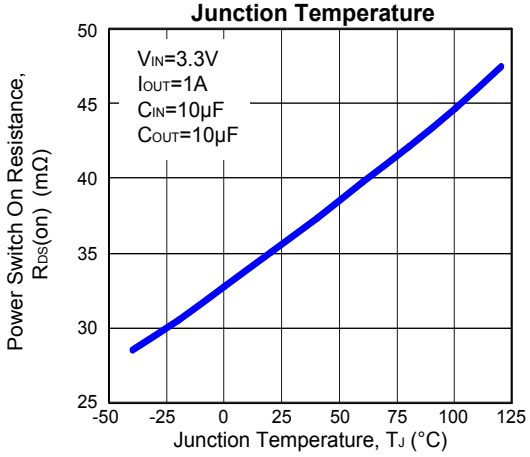
EN Logic Threshold Voltage vs. Junction Temperature



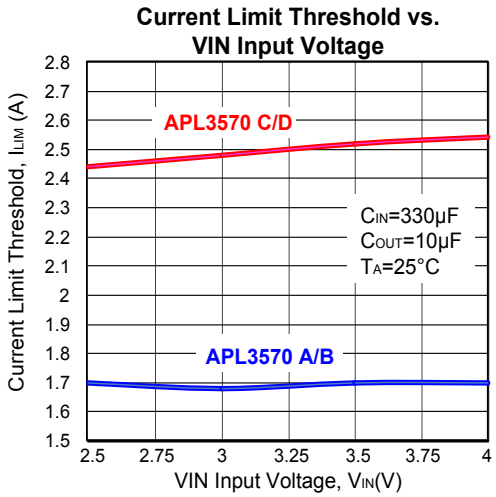
Power Switch On Resistance vs. VIN Input Voltage

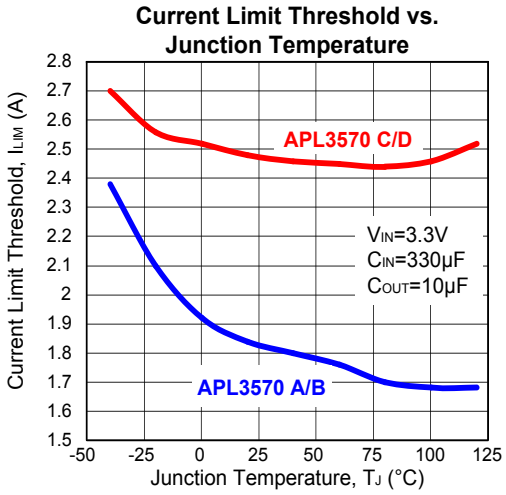


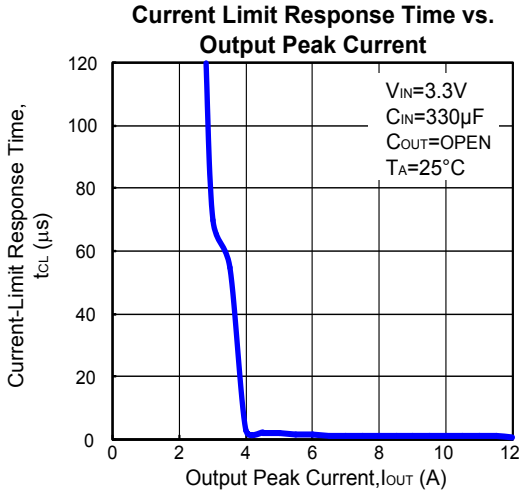
Power Switch On Resistance vs. Junction Temperature



Typical Operating Characteristics (Cont.)



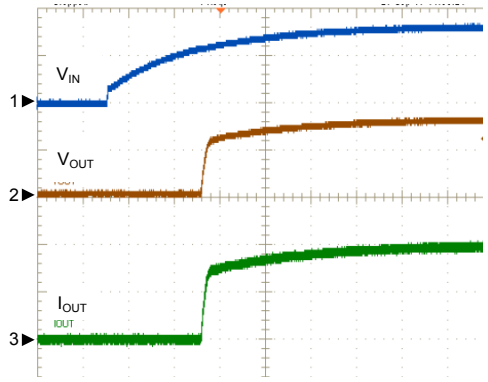




OperatingWaveforms

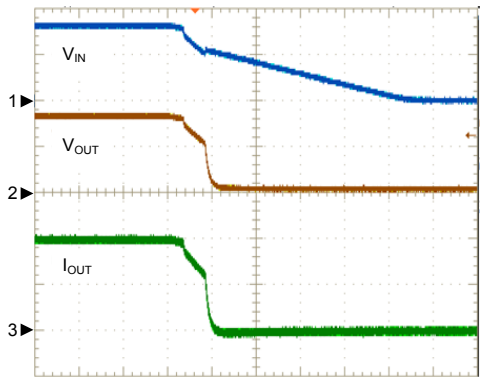
Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A= 25°C unless otherwise specified.

VIN Power ON



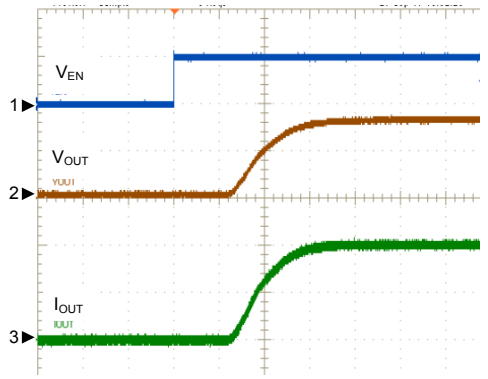
V_{IN}=3.3V, V_{EN}=3.3V, R_{LOAD}=1.65Ω
C_{IN}=10μF, C_{OUT}=10μF
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

VIN Power OFF



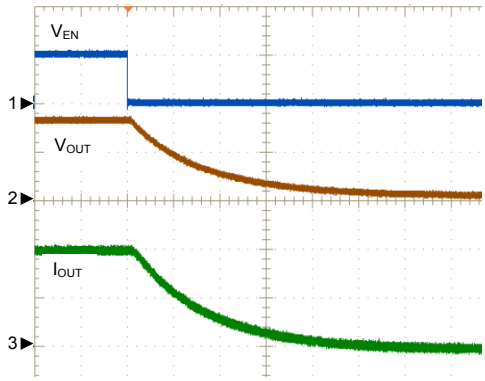
V_{IN}=3.3V, V_{EN}=3.3V, R_{LOAD}=1.65Ω
C_{IN}=10μF, C_{OUT}=10μF
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 200μs/Div

Enable Power ON



V_{IN}=3.3V, V_{EN}=3.3V, R_{LOAD}=1.65Ω
C_{IN}=10μF, C_{OUT}=10μF
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 100μs/Div

Enable Shutdown

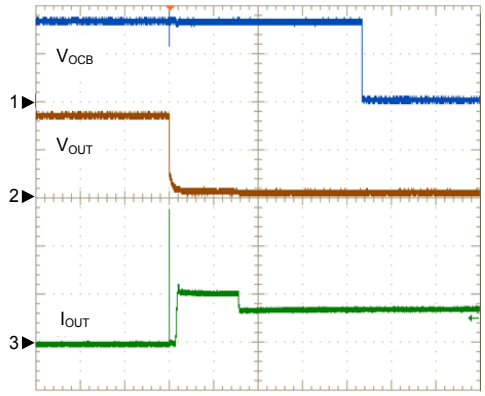


V_{IN}=3.3V, V_{EN}=3.3V, R_{LOAD}=1.65Ω
C_{IN}=10μF, C_{OUT}=10μF
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 10μs/Div

OperatingWaveforms (Cont.)

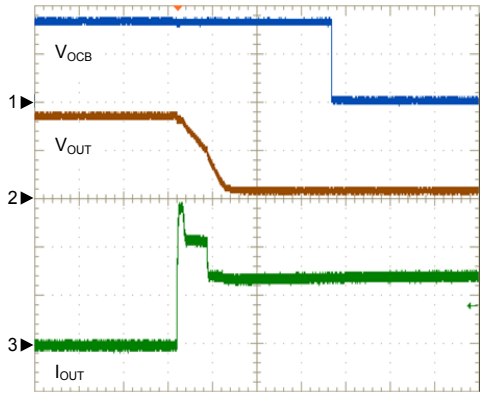
Refer to the typical application circuit. The test condition is V_{IN}=3.3V, T_A= 25°C unless otherwise specified.

OCB Response During Short Circuit



V_{IN}=3.3V, V_{EN}=3.3V, R_{LOAD}=0Ω
C_{IN}=330µF, C_{OUT}=330µF
CH1: V_{OCB}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 2A/Div, DC
TIME: 1ms/Div

OCB Response with Ramped Load

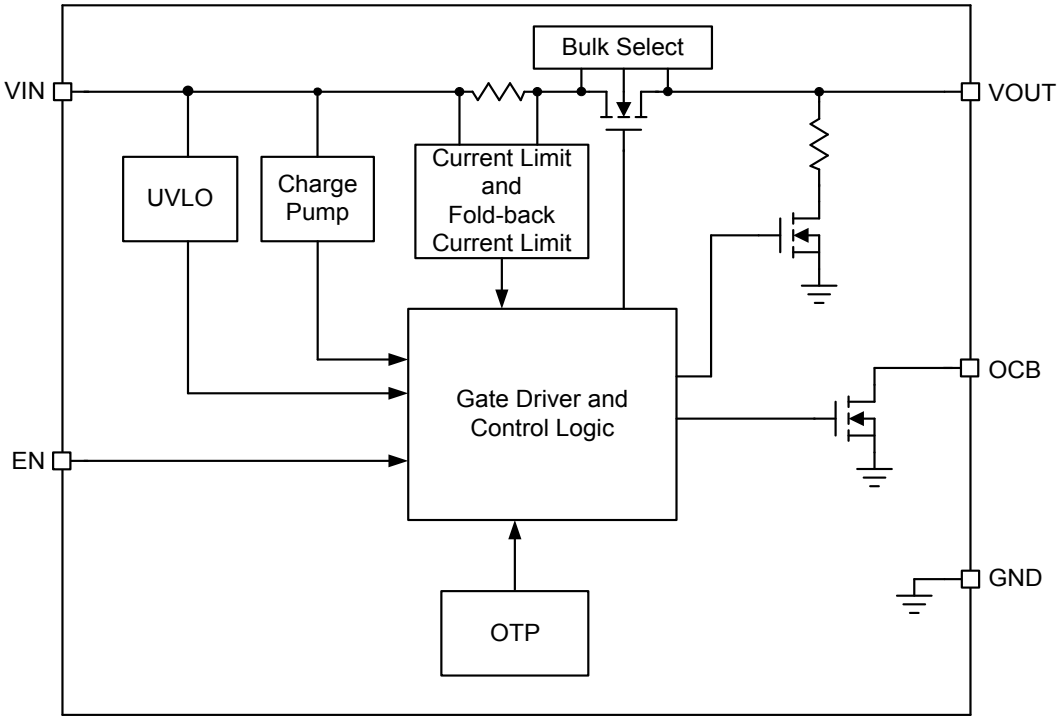


V_{IN}=3.3V, V_{EN}=3.3V
C_{IN}=330µF, C_{OUT}=330µF
CH1: V_{OCB}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 1ms/Div

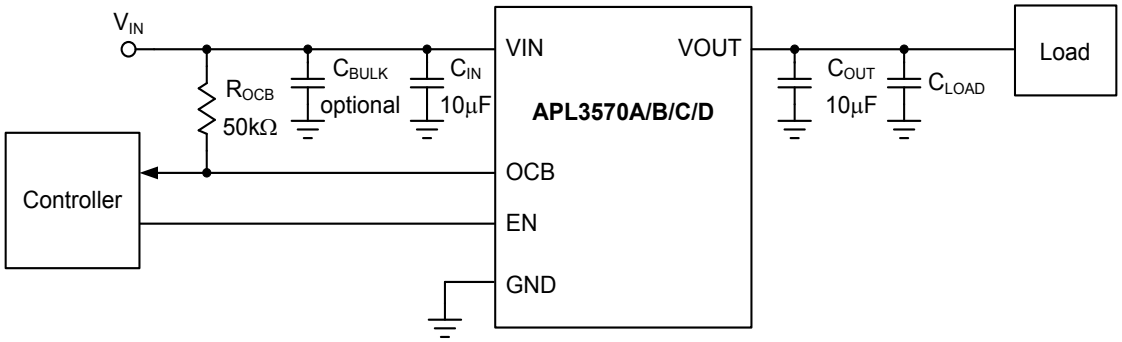
Pin Descriptions

PIN		NAME	FUNCTION
SOT-23-5	TDFN2x2-8		
NO.	NO.		
1	3, 4	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When EN is low, the output voltage is discharged by an internal resistor **(for APL3570A/C only).**
2	2	GND	Ground.
3	1	OCB	Fault Indication Pin. This pin goes low when a current limit, or an over-temperature condition is detected after a 3.2ms deglitch time.
4	7	EN	Enable Input. Pull this pin to high to enable the device and pull this pin to low to disable device. The EN pin cannot be left floating.
5	5, 6	VIN	Power Supply Input. Connect this pin to external DC supply.
-	8	NC	No Connection.
-	9	Exposed Pad	Connect this pad to system ground plane for good thermal conductivity.

Block Diagram



Typical Application Circuit



Function Descriptions

VIN Under-voltage Lockout (UVLO)

The APL3570 series of power switches are built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Reverse Current Blocking Circuit

The APL3570 series has a built-in reverse current blocking circuit to prevent a reverse current flowing through the body diode of power switch from the VOUT back VIN pin when power switch disabled.

Current Limit Protection

The APL3570 series of power switches provide the current limit protection function. During current limit, the devices limit output current at current limit threshold. For reliable operation, the device should not be operated in current limit for extended period time.

Fold-back Current Limit Protection

When the output voltage drops below VIN-1.3V, which is caused by the over load or short circuit, the devices limit the output current down to a safe level. The short circuit current limit is used to reduce the power dissipation during short circuit condition. If the junction temperature is over the thermal shutdown temperature the device will enter the thermal shutdown.

OCBOutput

The APL3570 series of power switches provide an open-drain output to indicate that a fault has occurred. When any of current limit or over-temperature protection occurs for a deglitch time of $t_{D(OCB)}$, the OCB goes low. Since the OCB pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Disable

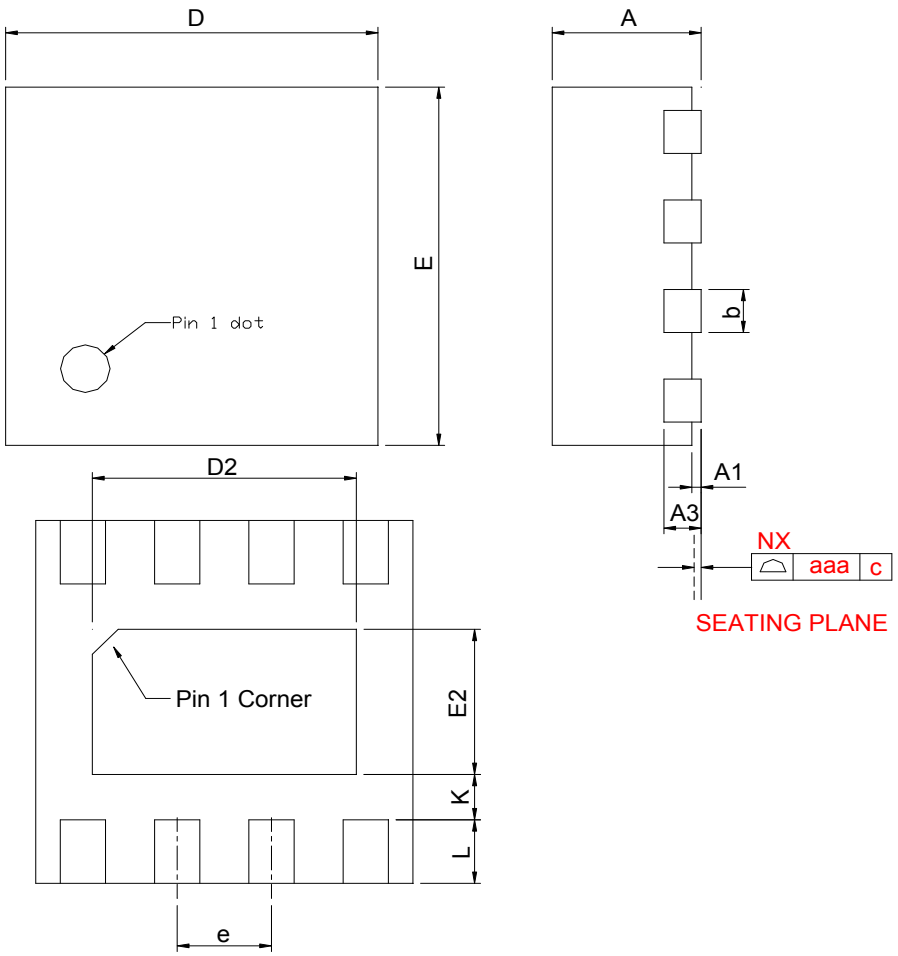
Pull the EN below 0.4V to disable the device and pull EN above 1.2V to enable the device. When the IC is disabled the supply current is reduced to less than 1μA. The enable input is compatible with both TTL and CMOS logic levels. The EN pins cannot be left floating.

Over-temperature Protection

When the junction temperature exceeds 150°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 30°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Package Information

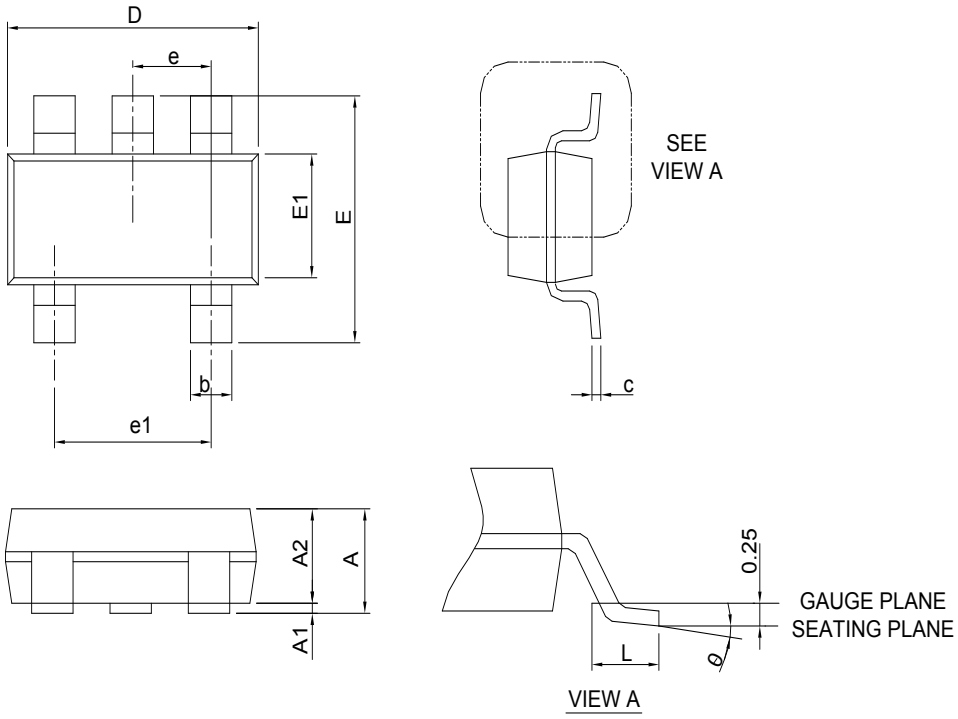
TDFN2x2-8



SYMBOL	TDFN2*2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20	0.30	0.008	0.012
aaa	0.08		0.003	

Package Information

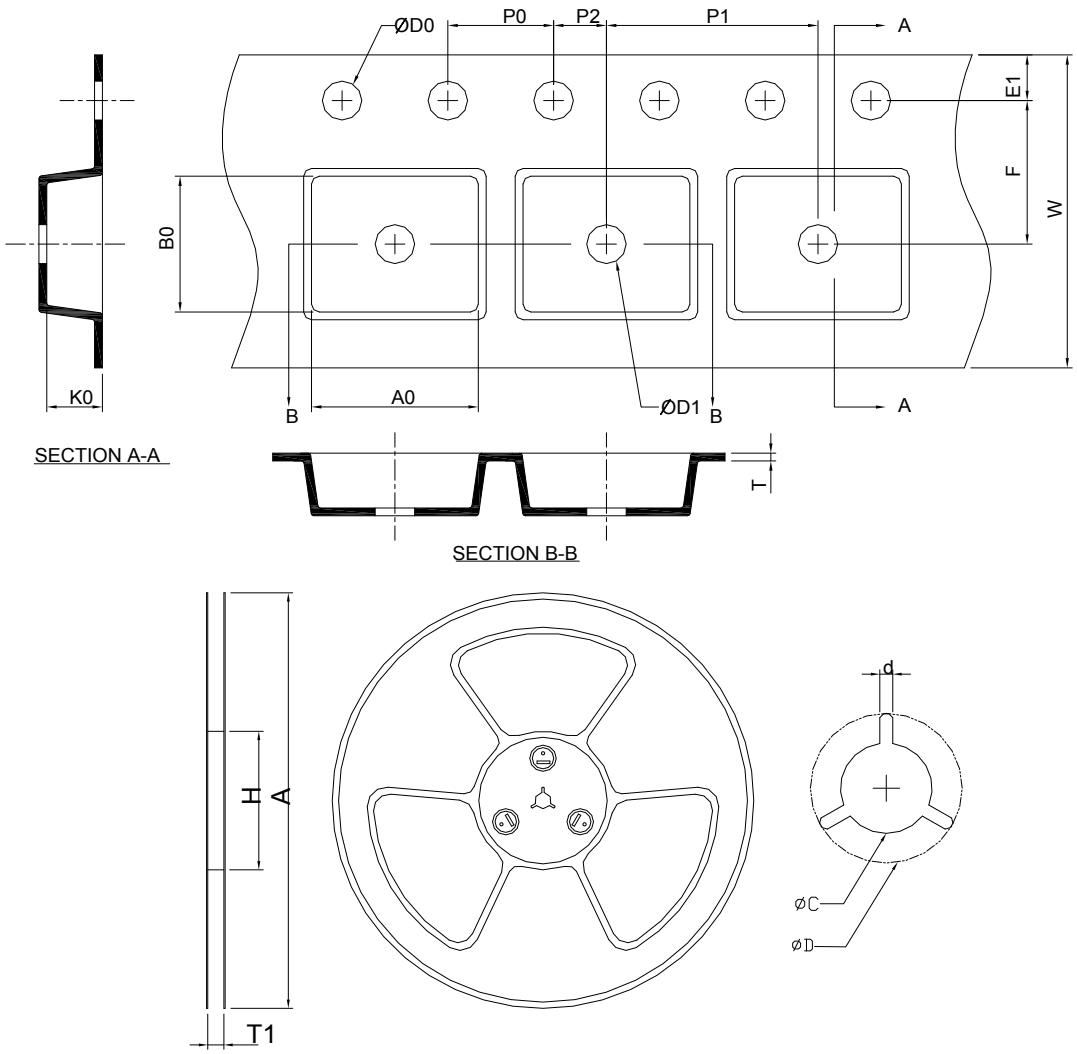
SOT-23-5



SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

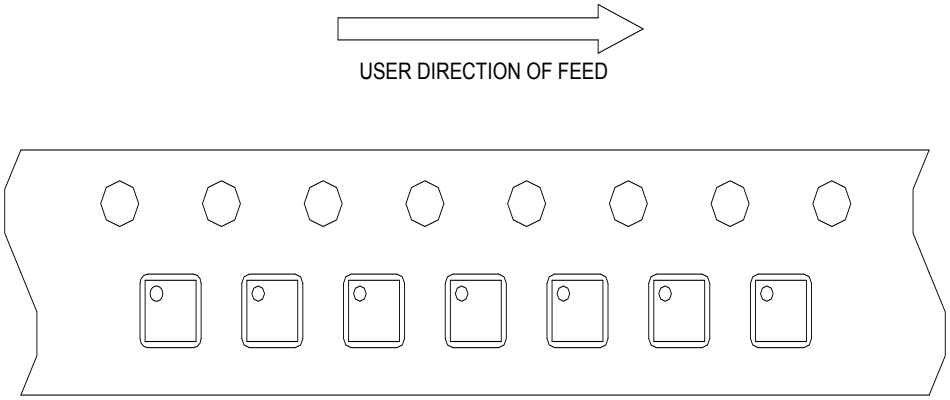
(mm)

Devices Per Unit

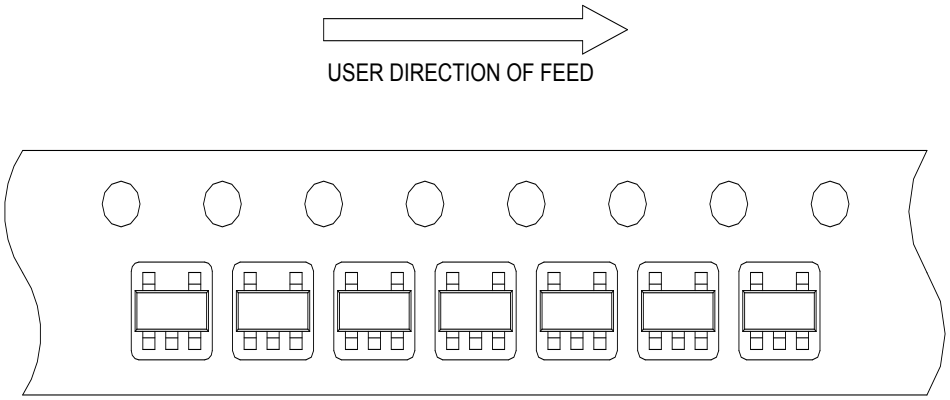
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000
SOT-23-5	Tape & Reel	3000

Taping Direction Information

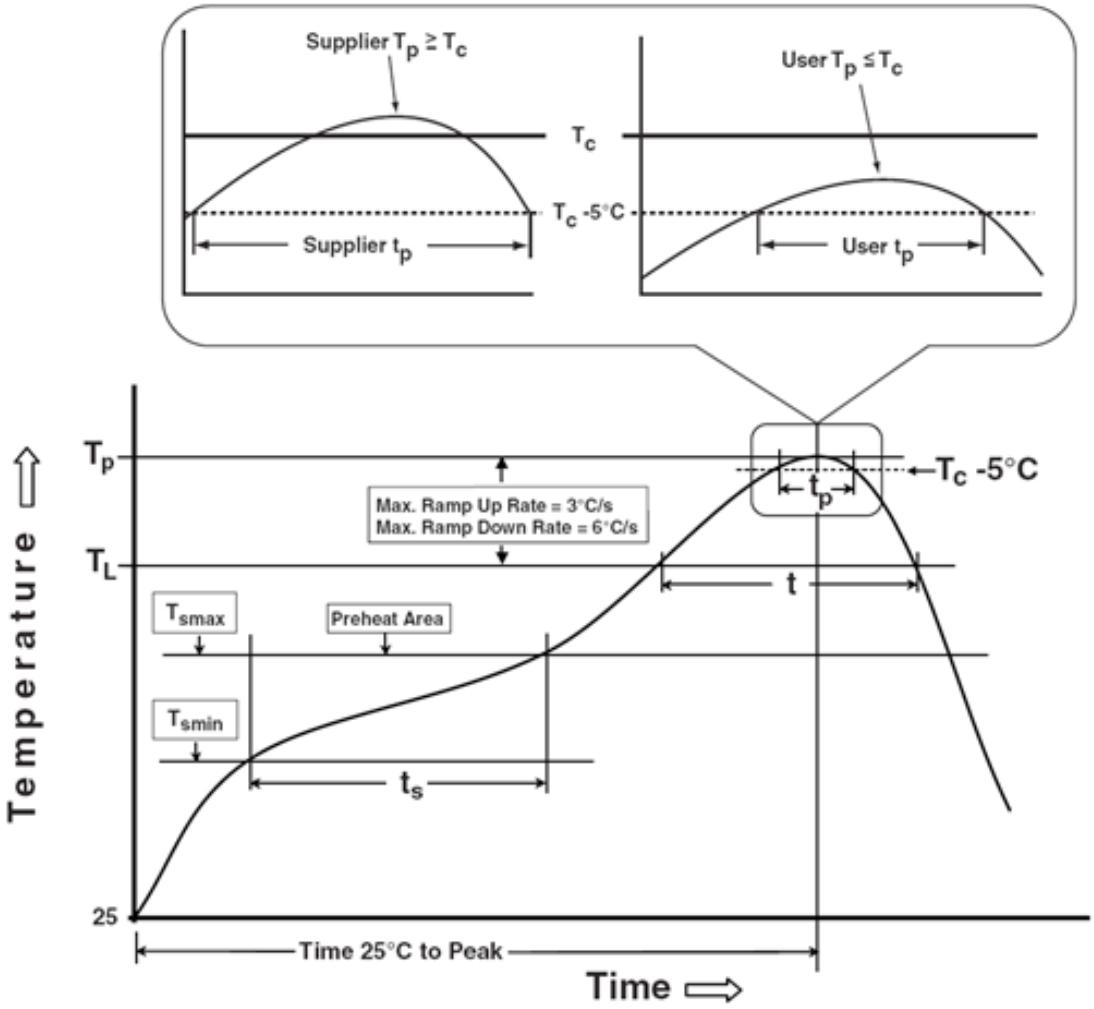
TDFN2x2-8



SOT-23-5



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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