PMIC for LED BL + LCD Bias Power

Features

- **2.9V to 5.5V Input Supply Range**
- **Current Mode Step-up Regulator (LCD bias)**
  - **1MHz Fixed Operating Frequency**
  - **Fast Transient Response**
  - **18V/700mA ,1.5Ω Internal N-MOS**
- **Positive & Negative Charge Pump Driver for V_{GH}, V_{GL}**
- **Current Mode Step-up Regulator (LED BL)**
  - **1MHz Fixed Operating Frequency**
  - **0.2V Feedback Voltage**
  - **18V/2A, 0.3Ω internal N-MOS**
- **Control Output for External P-MOS to Support**
- **Completely Disconnecting the Battery**
- **Adjustable Power Sequencing by External Capacitor**
- **Internal Soft-Start**
- **Multiple Overload Protection**
- **Thermal Shutdown**
- **Available in Small Package:TQFN3x3-20**

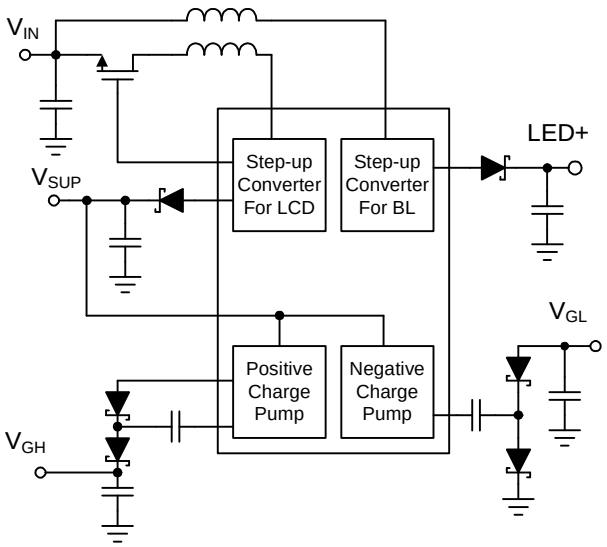
General Description

The APW7279 integrates with two high-performance step-up converter and two charge pump controllers for TFT-LCD and Backlight applications. Both the two step-up regulators are a current-mode, fixed-frequency PWM switching regulator. The 1.0MHz switching frequency allows the usage of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The charge pump controllers provide regulated the gate-driver of TFT-LCD V_{GH} and V_{GL} supplies. The APW7279 is available in a tiny 3mm x 3mm 20-pin TQFN package (TQFN3x3-20).

Applications

- **Tablet PC**

Simplified Application Circuit



Ordering and Marking Information

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<tr>
<td>APW7279 □□□-□□□
Assembly Material
Handling Code
Temperature Range
Package Code</td>
<td>Package Code
QB: TQFN3x3-20
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device</td>
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<td colspan="2">APW7279 QB: APW 7279 XXXXX — XXXXX - Date Code</td>
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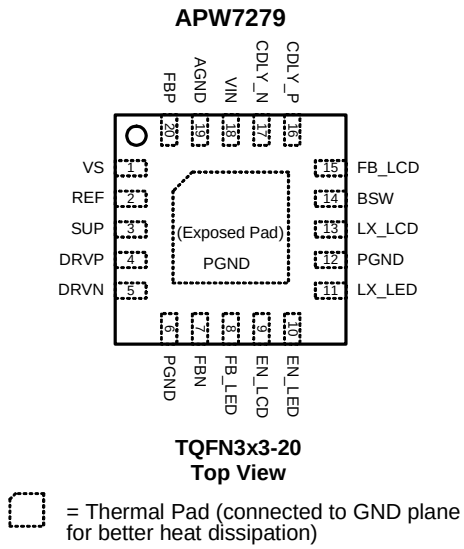
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN3x3-20
Top View

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
VIN	Input Bias Supply Voltage (VIN to GND)	-0.3 ~ 6	V
	LX_LCD, DRVN, DRVP, SUP, VS to GND Voltage	-0.3 ~ 20	V
	LX_LED	-0.3 ~ 20	V
	EN_LCD, EN_LED, FB_LCD, FB_LED, FBP, FBN, BSW, CDLY_N, VDLY_P, REF to GND Voltage	-0.3 ~ VIN	V
PD	Power Dissipation	Internally Limit	W
TJ	Maximum Junction Temperature	150	°C
TSTG	Storage Temperature	-65 ~ 150	°C
TSDR	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics (Note 2, 3)

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TQFN3x3-20	50	°C/W
θ_{JC}	Case-to-Ambient Resistance in free air (Note 2)	TQFN3x3-20	12	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Input Bias Supply Voltage (VIN to GND)	2.9 ~ 5.5	V
V_{SUP}	LCD Driver Step-up Converter Output Voltage	V_{IN} ~ 15	V
V_{GH}	Positive Charge Pump Output Voltage	0 ~ (2 x V_{SUP}) -2	V
V_{GL}	Negative Charge Pump Output Voltage	-V_{SUP} +2 ~ V_{REF}	V
C_{IN}	Input Power Capacitor	4.7 ~ 10	µF
L1	Inductor Range	1 ~ 10	µH
C_{GH}	VGH Capacitor	0.22 ~ 2.2	µF
C_{GL}	VGL Capacitor	0.22 ~ 2.2	µF
C_{REF}	VREF Capacitor	0.1 ~ 0.47	µF
R1	Feedback Resistance of V_{SUP}	0.1 ~ 1	MΩ
R3	Feedback Resistance of V_{GH}	0.1 ~ 1	MΩ
R5	Feedback Resistance of V_{GL}	0.1 ~ 0.54	MΩ
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7279			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
V_{IN}	Input Voltage Range		2.9	-	5.5	V
I_{OC}	VIN Operating Current	V_{FB_LCD} = 1.1V, switching V_{FB_LED} = 0.2V, switching	-	3	7	mA
I_{SD}	VIN Shutdown Current	V_{EN_LCD} = V_{EN_LED} = GND	-	0.1	1	uA
UNDER VOLTAGE LOCKOUT (UVLO)						
V_{IN}	UVLO Threshold Voltage	V_{IN} Rising	2.4	2.6	2.8	V
	UVLO Hysteresis Voltage		200	250	300	mV
STET-UP REGULATOR FOR LCD POWER						
V_{REF}	Reference Voltage	V_{IN} = 2.9V ~ 5.5V, T_A = -40 ~ 85°C I_{REF} = 0 ~ 2mA	1.22	1.25	1.28	V
I_{REF}	Reference Voltage Output Current		2	-	-	mA
V_{FB_LCD}	FB_LCD Regulation Voltage	V_{IN} = 2.9V ~ 5.5V, T_A = -40 ~ 85°C	1.22	1.25	1.28	V
I_{FB_LCD}	FB_LCD Input Current		-50	-	50	nA
F_{SW_LCD}	Switching Frequency	V_{FB_LCD} = 1.1V	0.85	1.0	1.15	MHz
R_{ON_LCD}	Power Switch On Resistance	V_{IN} = 3.6V	-	1.1	-	Ω
I_{LIM_LCD}	Power Switch Current Limit		1	-	-	A
	LX_LCD Leakage Current	V_{IN} = 5V, V_{EN_LCD} = GND, V_{LX_LCD} = 16V	-1	-	1	uA
D_{MAX_LCD}	LX_LCD Maximum Duty Cycle		92	95	98	%
T_{SS_LCD}	Step-up Regulator Soft-start Duration	(Note 4)	-	2	-	ms
V_{FB_UVP}	FB_LCD Under Voltage Protection (UVP)		-	1	-	V
	UVP Debounce time		-	250	-	us
STET-UP REGULATOR FOR LED BACKLIGHT						
V_{FB_LED}	FB_LED Regulation Voltage	V_{IN} = 2.9V ~ 5.5V, T_A = -40 ~ 85°C (T_J = -40 ~ 125°C)	190	200	210	mV
I_{FB_LED}	FB_LED Input Current		-50	-	50	nA
F_{SW_LED}	Switching Frequency	V_{FB_LED} = GND	0.85	1.0	1.15	MHz
R_{ON_LED}	Power Switch On Resistance	V_{IN} = 3.6V	-	0.3	-	Ω
I_{LIM_LED}	Power Switch Current-Limit		2	-	-	A
	LX_LED Leakage Current	V_{IN} = 5V, V_{EN_LED} = GND, V_{LX_LED} = 16V	-1		1	uA
D_{MAX_LED}	LX_LED Maximum Duty Cycle		92	95	98	%
V_{LX_OVP}	LX_LED Over Voltage Threshold	V_{LX_LED}Rising	16.5	18	19.9	V
T_{SS_LED}	Step-up Regulator Soft-start Duration	(Note 4)	-	2	-	ms

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7279			Unit
			Min	Typ	Max	
SHUTDOWN						
V_{ENH_LCD}	EN_LCD High Threshold	V_{EN_LCD} Rising	1.4	-	-	V
V_{ENL_LCD}	EN_LCD Low Threshold	V_{EN_LCD} Falling	-	-	0.4	V
	EN_LCD Leakage Current	V_{IN} = 5V, V_{EN_LCD} = 5V	-1	-	5	uA
V_{ENH_LED}	EN_LED High Threshold	V_{EN_LED} Rising	1	-	-	V
V_{ENL_LCD}	EN_LED Low Threshold	V_{EN_LED} Falling	-	-	0.4	V
	EN_LED Leakage Current	V_{IN} = 5V, V_{EN_LED} = 5V	-1	-	1	uA
CHARGE CURRENT AND INTERNAL SWITCH						
I_{CDLY_N}	CDLY_N Charge Current		-	10	-	uA
	CDLY_N High Threshold	V_{GL} Soft-start without Delay from V_{AVDD}	-	1	-	V
I_{CDLY_P}	CDLY_P Charge Current		-	10	-	uA
	CDLY_P High Threshold	V_{GH} Soft-start without Delay from V_{GL}	-	1	-	V
I_{BSW}	BSW Pull-down Current		3	5	10	uA
	BSW to VIN Ron		-	200	-	Ω
R_{VS}	SUP to VS On Resistance		-	300	-	Ω
	SUP to VS Leakage Current		-	-	100	nA
	VS Soft-start Duration	(Note 4)	-	2	-	ms
POSITIVE REGULATED CHARGE PUMP						
V_{FBP}	FBP Regulation Voltage	V_{IN} = 2.9V ~ 5.5V, T_A = -40 ~ 85°C	1.22	1.25	1.28	V
I_{FBP}	FBP Input Current		-50	-	50	nA
I_{DRVP}	RMS DRVP Output Current	V_{SUP} = 12V	5	-	-	mA
	Positive Charge Pump Frequency		400	500	600	kHz
T_{SSP}	Positive Charge Pump Soft-start Duration	(Note 4)	-	2	-	ms
NEGATIVE REGULATED CHARGE PUMP						
V_{FBN}	FBN Regulation Voltage	V_{IN}=2.9V~5.5V, T_A = -40 ~ 85°C	-25	0	25	mV
I_{FBN}	FBN Input Current		-50	-	50	nA
I_{DRVN}	RMS DRVN Output Current	V_{SUP} = 12V	5	-	-	mA
	Negative Charge Pump Frequency		400	500	600	kHz
T_{SSN}	Negative Charge Pump Soft-start Duration	(Note 4)	-	2	-	ms
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over-Temperature Protection (note4)	T_J Rising	-	160	-	°C
	Over-Temperature Protection Hysteresis (note4)		-	40	-	°C

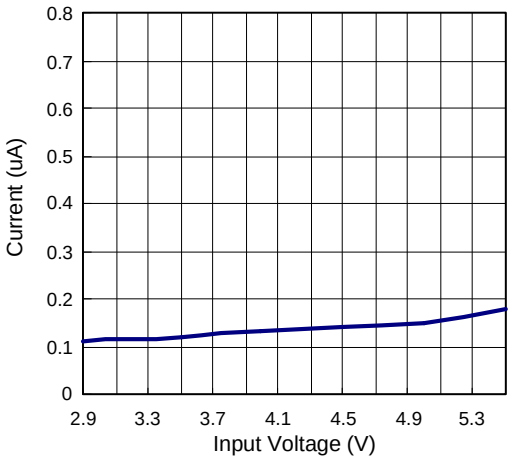
Note 4: Guarantee by design, not production test.

Pin Description

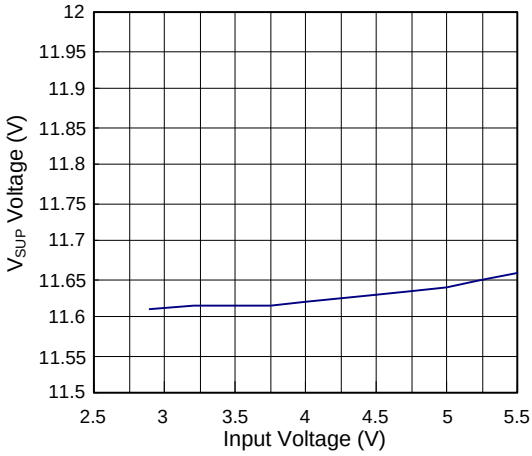
Pin		Function
TQFN3x3-20	NAME	
1	VS	The supply voltage of positive charge pump regulator.
2	REF	Internal 1.25V reference voltage output. Connect 1μF capacitor to this pin.
3	SUP	This is the supply pin of the positive and negative charge pump driver. Connected this pin to the output of the LCD Driver step-up converter V_{SUP}.
4	DRVP	Regulated charge pump driver for V_{GH}. Connect to flying capacitor.
5	DRVN	Regulated charge pump driver for V_{GL}. Connect to flying capacitor.
6	PGND	Power Ground.
7	FBN	Negative charge pump feedback input.
8	FB_LED	Step-up converter feedback input of LED driver.
9	EN_LCD	Enable pin of LCD driver. Logic high initiates power-up sequencing. Logic low disable the LCD Driver.
10	EN_LED	Enable pin of LED driver. Logic high initiates power-up sequencing. Logic low disable the LED Driver.
11	LX_LED	Step-up converter inductor/diode connection.
12	PGND	Power Ground.
13	LX_LCD	Step-up converter inductor/diode connection.
14	BSW	Bi-direction switch control pin. This switch disconnects VOUT from VIN during shutdown and any fault evens.
15	FB_LCD	Step-up converter feedback input of LCD driver.
16	CDLY_P	Delay Setting Capacitor Connection Pin. Connecting a capacitor from this pin to GND allows the setting of delay time between V_{SUP} to V_{GL} during start-up. Pull this pin exceed 1V ignore the delay time.
17	CDLY_N	Delay Setting Capacitor Connection Pin. Connecting a capacitor from this pin to GND allows the setting of delay time between V_{GL} to V_{GH} during start-up. Pull this pin exceed 1V ignore the delay time.
18	VIN	IC power input.
19	AGND	Analog Ground.
20	FBP	Positive charge pump feedback input.
Exposed Pad	PGND	Power Ground.

Typical Operating Characteristics

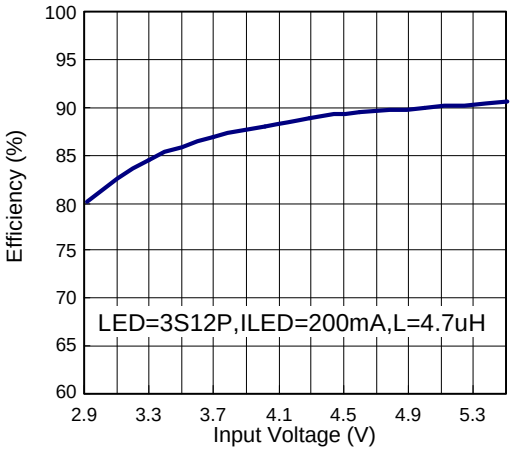
Shutdown Current VS Input Voltage



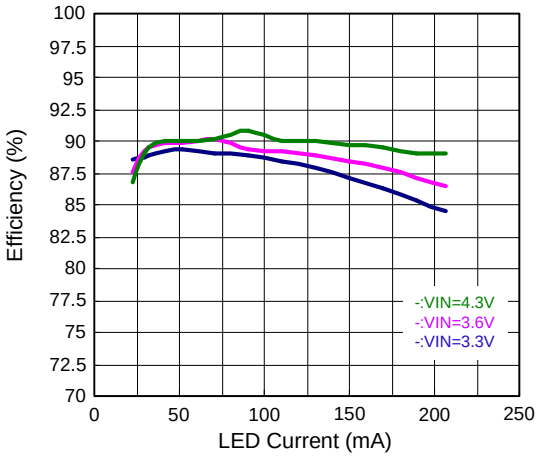
V_{SUP} Voltage VS Input Volatge



Efficiency VS Input Voltage

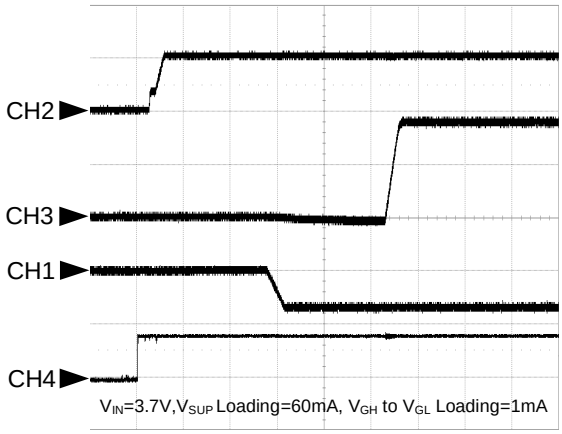


Efficiency VS LED current



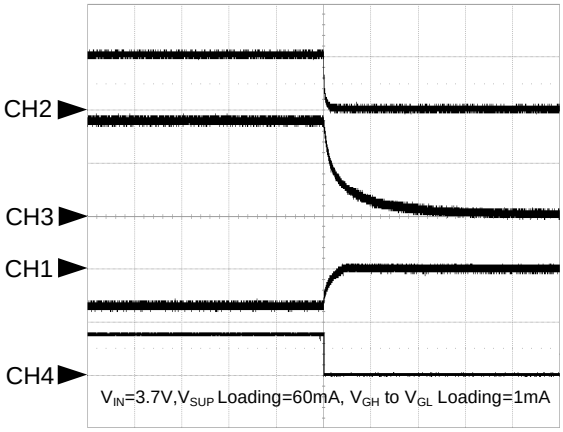
Operating Waveforms

Power on EN_LCD



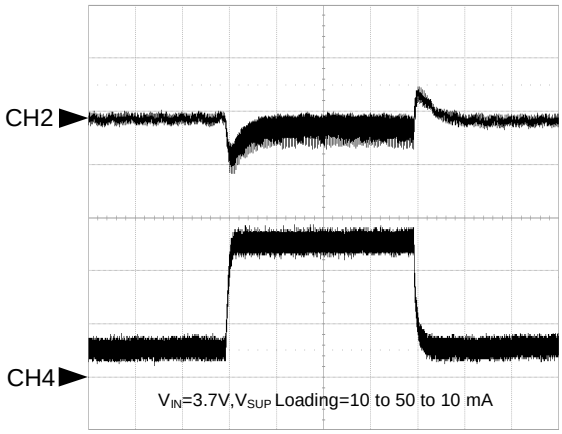
CH1:V_{GL}-10V/div
CH2:V_{GH}-10V/div
CH3:V_{SUP}-10V/div
CH4:V_{EN_LCD}-5V/div
Time:5ms/div

Power off EN_LCD



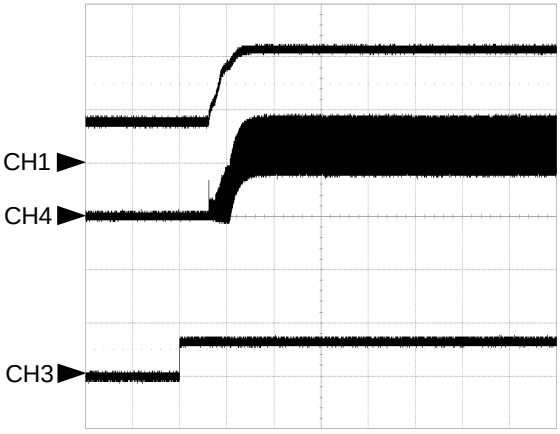
CH1:V_{GL}-10V/div
CH2:VGH-10V/div
CH3:V_{SUP}-10V/div
CH4:V_{EN_LCD}-5V/div
Time:50ms/div

V_{SUP} Load Transient



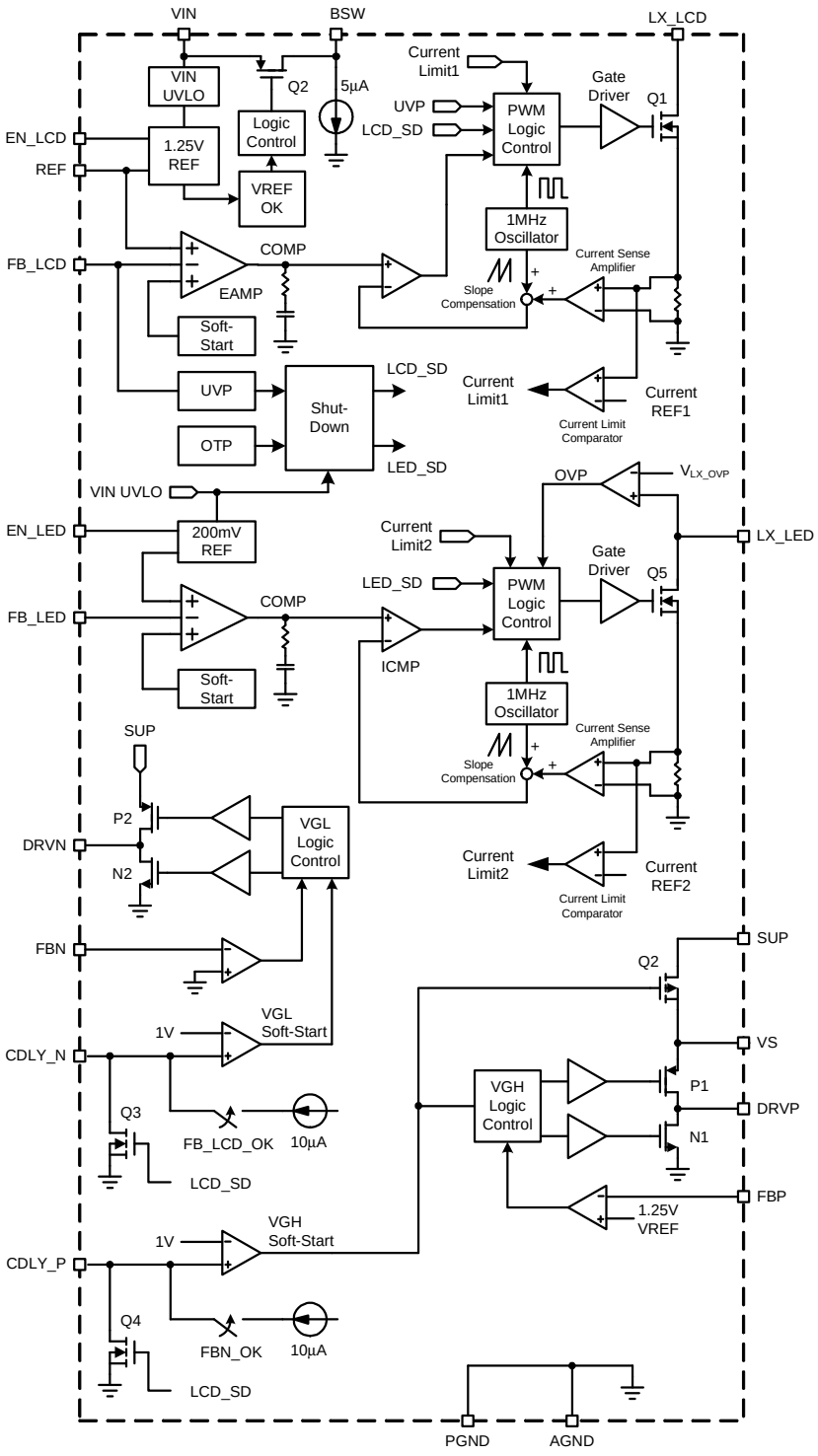
CH2:V_{SUP}-20mV/div
CH4:I_{SUP}-20mA/div
Time:500us/div

Power on EN_LED

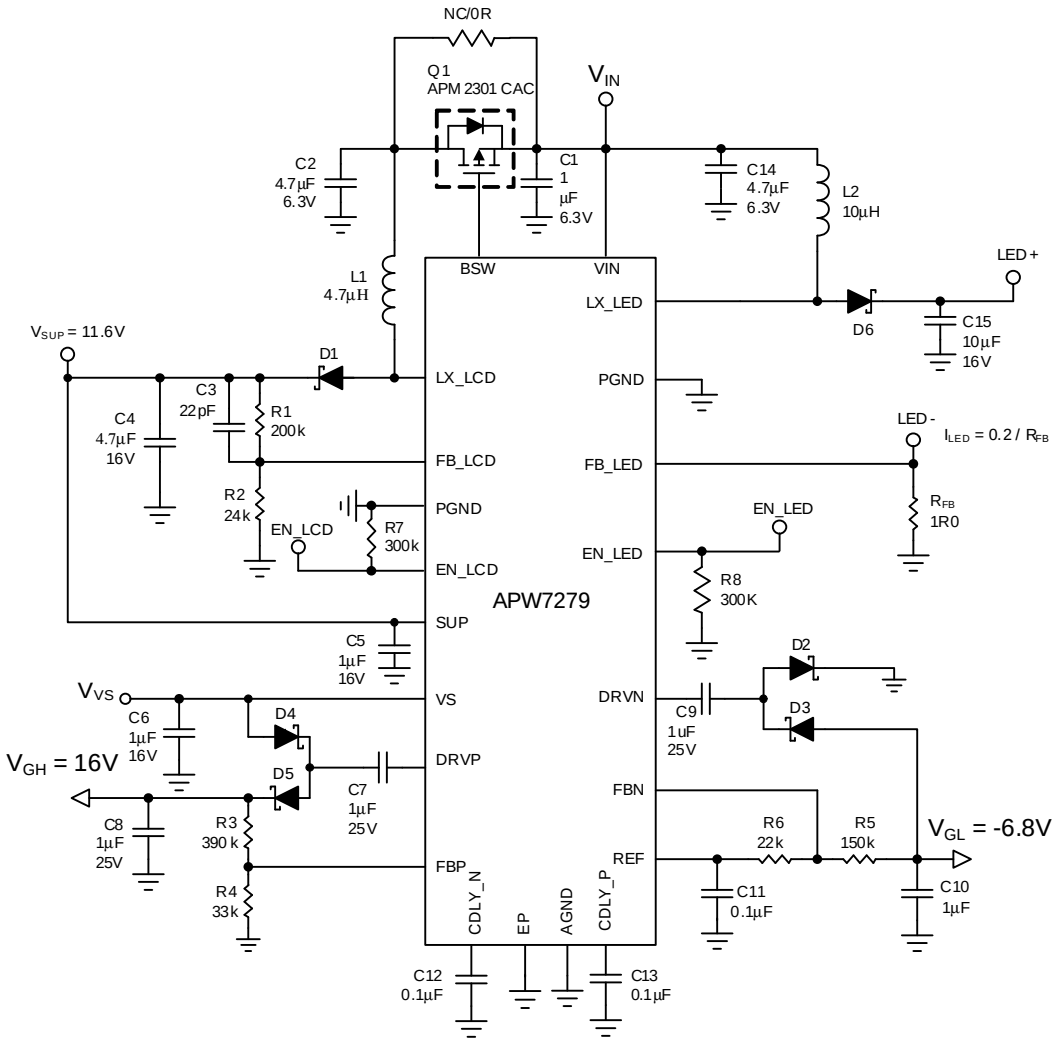


CH1:V_{LED}-5V/div
CH3:V_{EN_LED}-5V/div
CH4:I_L-500mA/div
Time:2ms/div

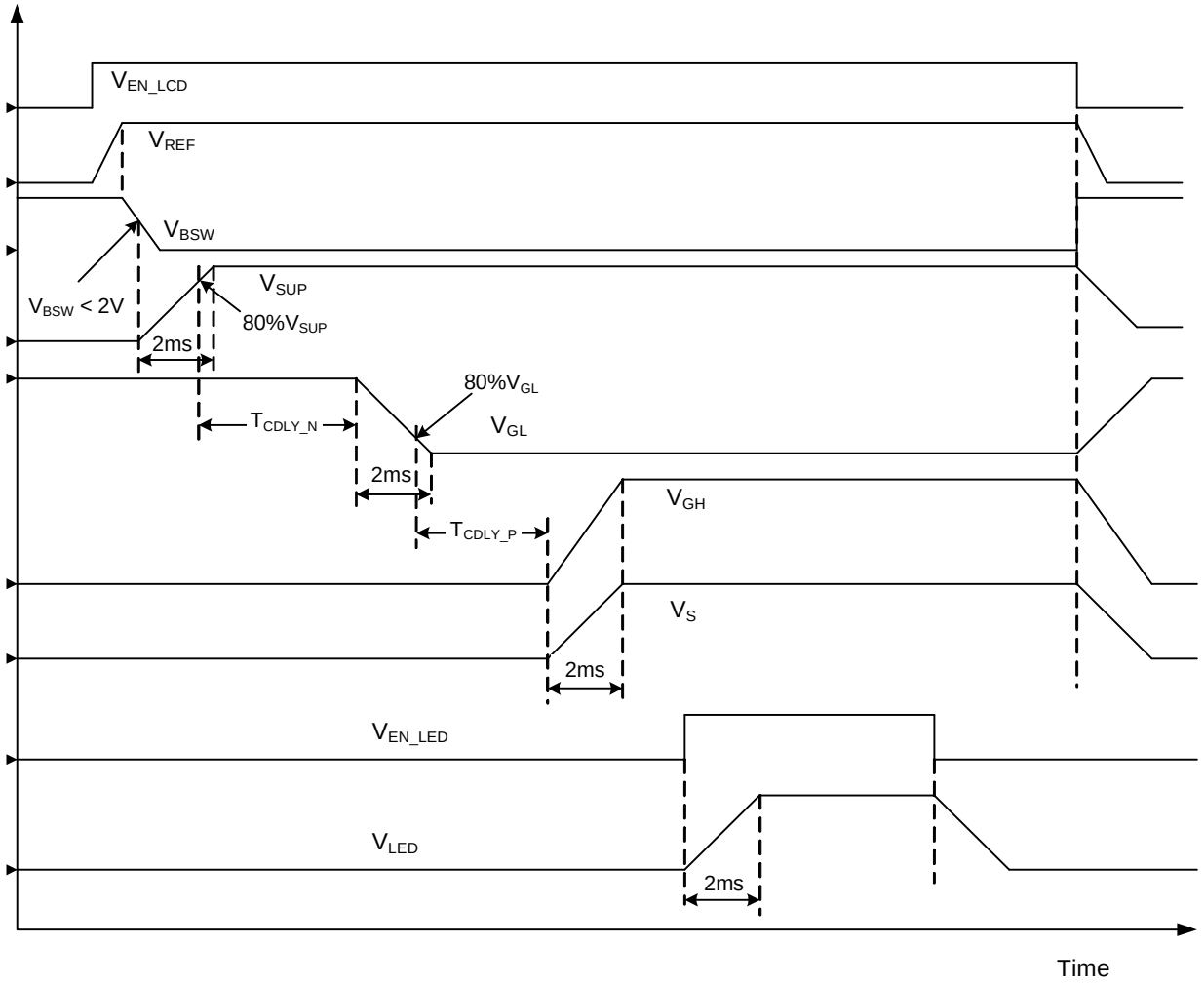
Block Diagram



Typical Application Circuit



Power On Sequence



The output voltage falling slew rate after shutdown depend on external resistance.

Function Description

VIN Under-Voltage Lockout (UVLO)

The Under-voltage lockout (UVLO) circuit compares the input voltage at VIN with the UVLO threshold to ensure the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the device.

LCD Driver Step-up Converter Control Loop

The APW7279 includes a constant frequency, synchronous rectifier and current-mode switching regulator. In normal operation, the internal main switch (Q1) is turned on each cycle. The peak inductor current at which EAMP turn off the Q1 is controlled by the voltage on the COMP node which is the output of the error amplifier (EAMP). An external resistive divider connected between VSUP and ground allows the EAMP to receive an output feedback voltage VFB at FB pin. When the load current increases, it causes a slightly decrease in VFB relative to the reference voltage, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current. At light load current, the COMP voltage is lower. The APW7279 auto skips pulse.

Pulse Skip Modulation

APW7279 auto skip pulse at light load.

LCD Driver Step-up Converter Current Limit

The APW7279 integrated a current-limit-comparator in main step-up converter. It monitors the inductor current, flows through the N-channel MOSFET(Q1), and limits the current peak at current-limit level to prevent loads and the APW7279 from damaging during overload or short-circuit conditions.

VREF

The VREF initiates soft-start process after POR and EN_LCD goes high. Shutdown if POR and EN_LCD goes low.

CDLY_N

Connecting a capacitor from this pin to GND allows the setting of delay time between V_{GL} and V_{SUP}. Once V_{SUP} reaches 80% of its normal regulated output voltage, an internal 10uA current source starts to charge C_{CDLY_N}, the V_{GL} channel initiates soft-start process once V_{CDLY_N} exceed 1V. If the V_{CDLY_N} exceeds 1V before V_{SUP} start up, the V_{SUP} and V_{GL} start up simultaneously.

CDLY_P

Connecting a capacitor from this pin to GND allows the setting of delay time between V_{GH} and V_{GL}. Once V_{GL} reaches 80% of its normal regulated output voltage, an internal 10uA current source starts to charge C_{CDLY_P}, the V_{GH} channel initiates soft-start process once V_{CDLY_P} exceed 1V. If the V_{CDLY_P} exceeds 1V before V_{GL} start up, the V_{GL} and V_{GH} start up simultaneously.

BSW

Once V_{REF} is within 8% of its normal regulated output voltage, an internal current source from the BSW to GND to pull BSW low. Once the VBSW below 2V, the LCD driver step-up converter initiates soft-start process. The V_{BSW} pull to VIN if main step-up current limit detected without delay, EN_LCD pull low or VIN below POR.

An Isolation Switch from VSUP to VS (Q2)

The VS is the voltage source of positive charge pump (V_{GH}). Once V_{GL} reaches 80% of its normal regulated output voltage, the timer will start counting T_{CDLY_P}. The P-FET(Q2) starts switching soft on after T_{CDLY_P} and the Q2 fully turns on after 2ms. The Q2 turns off at Q1 current limit detected and EN_LCD goes low.

Function Description

Positive Charge Pump

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The charge pump includes a high-side p-channel MOSFET(P1) and a low-side n-channel MOSFET(N1) to control the power transfer as shown in Figure 1. During the first half-cycle, N1 turns on and charges flying capacitors C8 (Figure 1). During the second half cycle, N1 turns off and P1 turns on, level shifting C8 by V_{SUP} volts. The amount of charge transferred to the output is determined by the error amplifier that controls P1's on-resistance. The positive charge-pump regulator's startup can be delayed by C_{CDLY_P} from negative charge pump reaches 80% of its normal regulated output voltage, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V. The soft-start period is 2ms (typ). The soft-start feature effectively limits the inrush current during startup. The t_{CDLY_P} is calculated by the following equation.

$$t_{COLY\_P} = \frac{C_{CDLY\_P}}{10uA}$$

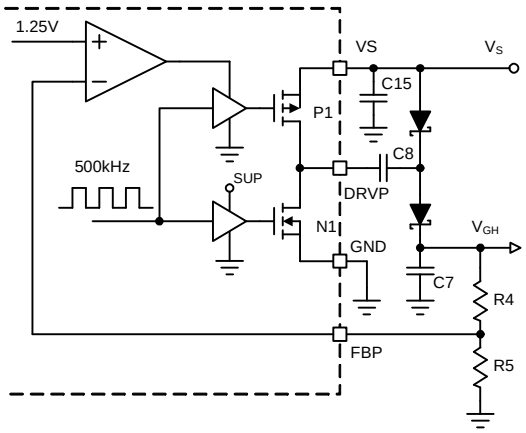


Fig1. Positive Charge Pump Regulator Block Diagram

Negative Charge Pump

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 2.

During the first half cycle, P2 turns on, and flying capacitor C10 charges to V_{SUP} minus a diode drop. During the second half cycle, P2 turns off, and N2 turns on, level shifting C10. This connects C10 in parallel with reservoir capacitor C11. If the voltage across C11 minus a diode drop is greater than the voltage across C10, charge flows from C11 to C10 until the diode (D5) turns off. The amount of charge transferred from the output is determined by the error amplifier, which controls N2's on-resistance. The negative charge-pump regulator is enabled when the LCD driver step-up regulator reaches 80% of its normal regulated output voltage and V_{CDLY_N} exceed 1V. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 0mV. The soft-start period is 2ms typically. The soft-start feature effectively limits the inrush current during startup. The t_{CDLY_N} is calculated by the following equation.

$$t_{COLY\_N} = \frac{C_{CDLY\_N}}{10uA}$$

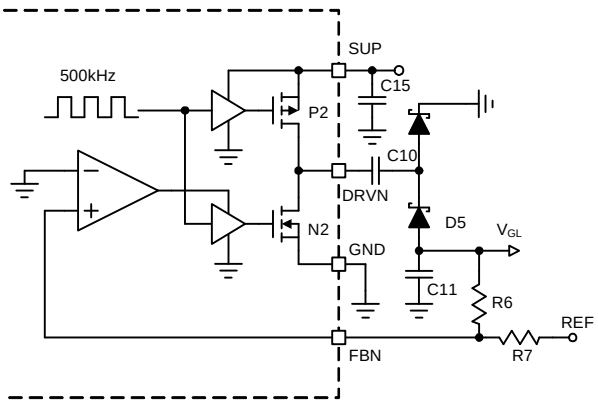


Fig2. Negative Charge Pump Regulator Block Diagram

Function Description

LED Driver Step-up Converter Control Loop

The APW7279 includes a constant frequency current-mode switching regulator. During normal operation, the internal N-channel power MOSFET (Q5) is turned on each cycle when the oscillator sets an internal RS latch and turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP node, which is the output of the error amplifier (EAMP). An external current-sense resistor connected between cathode of the lowest LED and ground allows the EAMP to receive a current feedback voltage V_{FB_LED} at FB_LED pin. When the LEDs voltage decreases to cause the LEDs current to decrease, it causes a slightly decrease in V_{FB_LED} relative to the reference voltage, which in turn causes the COMP voltage to increase until the LEDs current reaches the set point. The soft-start period is 2ms (typ). The soft-start feature effectively limits the inrush current during startup.

LED Driver Current-Limit Protection

The APW7279 monitors the inductor current, flowing through the N-channel MOSFET (Q5), and limits the current peak at current-limit level to prevent loads and the APW7279 from damaging during overload conditions.

EN_LED/Dimming

Driving EN_LED to ground places the APW7279 in shutdown mode. When in shutdown, the internal power MOSFET (Q5) turns off, all internal circuitry shuts down and the quiescent supply current reduces to 1mA maximum. This pin also could be used as a digital input allowing brightness controlled by using a PWM signal with frequency from 5kHz to 100kHz. The 0% duty cycle of PWM signal corresponds to zero LEDs current and 100% corresponds to full one. If use EN Pin to enable the device, suggestion dimmimg duty range is from 15% to 100% at 100kHz dimmimg frequency.

EN_LED/Dimming

In driving LED applications, the feedback voltage on FB_LED pin falls down if one of the LEDs, in series, is failed. Meanwhile, the converter unceasingly boosts the output voltage like an open-loop operation. Therefore, an over-voltage protection monitoring the output voltage via LX pin prevents the LX and the output voltages from exceeding their maximum voltage ratings. Once the voltage on the LX pin rises above the OVP threshold, the converter stops switching and prevents the output voltage from rising. The converter can work again when the LX voltage falls below the falling of OVP voltage threshold.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7279. When the junction temperature exceeds 160°C, a thermal sensor turns off the power MOSFET allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulates the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions increasing the lifetime of the device.

Application Information

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller with larger C_{IN}. For reliable operation, it is recommended to select the capacitor voltage rating at least 1.2 times higher than the maximum input voltage. The capacitors should be placed close to the V_{IN} and GND.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔI_L, is 30% to 50% of the average inductor current. The recommended inductor value can be calculated as below:

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{F_{SW} \cdot I_{OUT(MAX)}} \left(\frac{\eta}{\frac{\Delta I_L}{I_{L(AVG)}}}\right)$$

Where

VIN = input voltage

VOUT = output voltage

F_{SW} = switching frequency in MHz

I_{OUT} = maximum output current in amp.

η = Efficiency

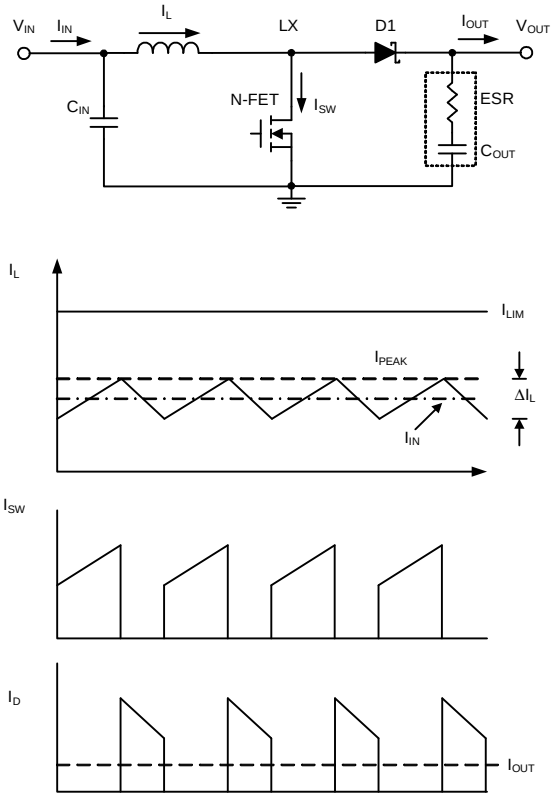
$\Delta I_L / I_{L(AVG)}$ = (0.3 to 0.5 typical)

To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)} - V_{OUT}}{V_{IN} \cdot \eta}$$

The peak inductor current is calculated as follow equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \times \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot L \cdot F_{SW}}$$



Application Information

Output Capacitor Selection

The current-mode control scheme of the APW7279 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$

$\Delta V_{ESR} \cong I_{PEAK} \cdot R_{ESR}$

Where I_{PEAK} is the peak inductor current. For ceramic capacitor application, the output voltage ripple is dominated by the ΔV_{COUT}. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

Setting the LED Current

In Typical Application Circuit, the converter regulates the voltage on FB_LED pin, connected with the cathode of the lowest LED and the current- sense resistor RFB at V_{REF}. Therefore, the current (I_{LED}), flowing via the LEDs and the RFB, is calculated by the following equation:

$$I_{LED} = \frac{V_{REF}}{R_{FB}}$$

Layout Consideration

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor C1, C5 and C14 should be placed close to the VIN/SUP and GND. Connecting the capacitor with VIN/SUP and GND pins by short and wide tracks for filtering and minimizing the input voltage ripple.
2. The inductor and Schottky diode should be placed as close as possible to the LX_LCD/LX_LED pin to minimize length of the copper tracks as well as the noise coupling into other circuits.
3. A star ground connection or ground plane minimizes ground shifts and noise is recommended.
4. Since the feedback pin (FBx) and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.

TQFN 3x3 - 20

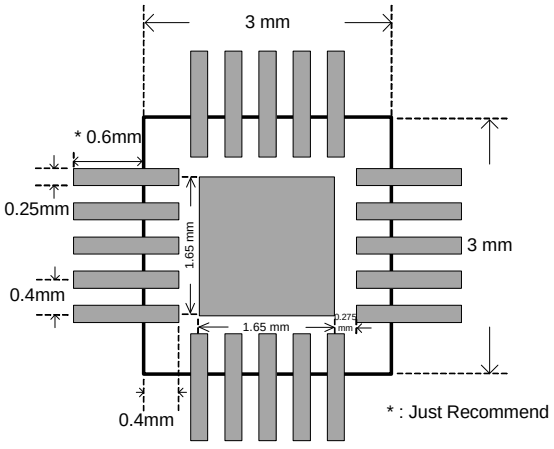
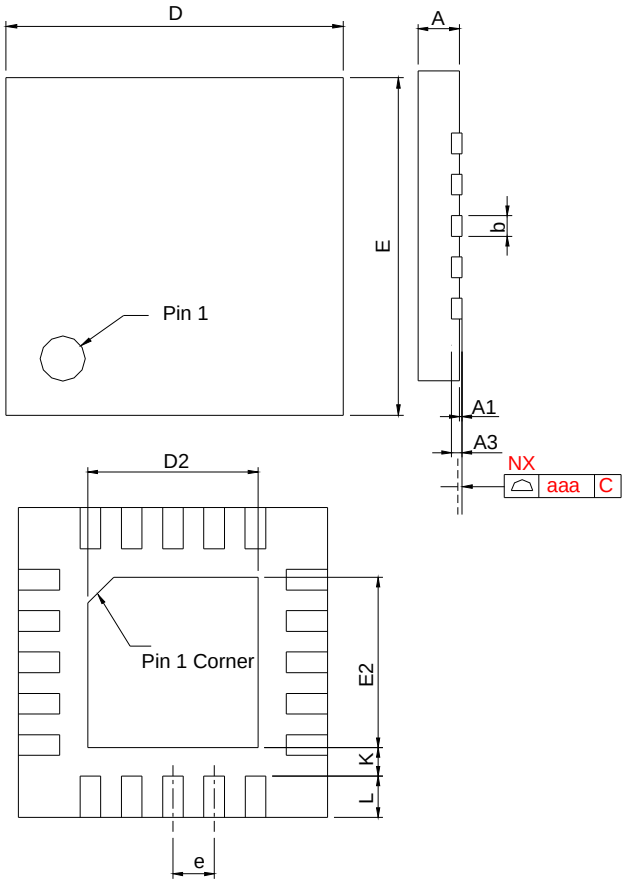


Figure : Recommended Minimum Footprint

Package Information

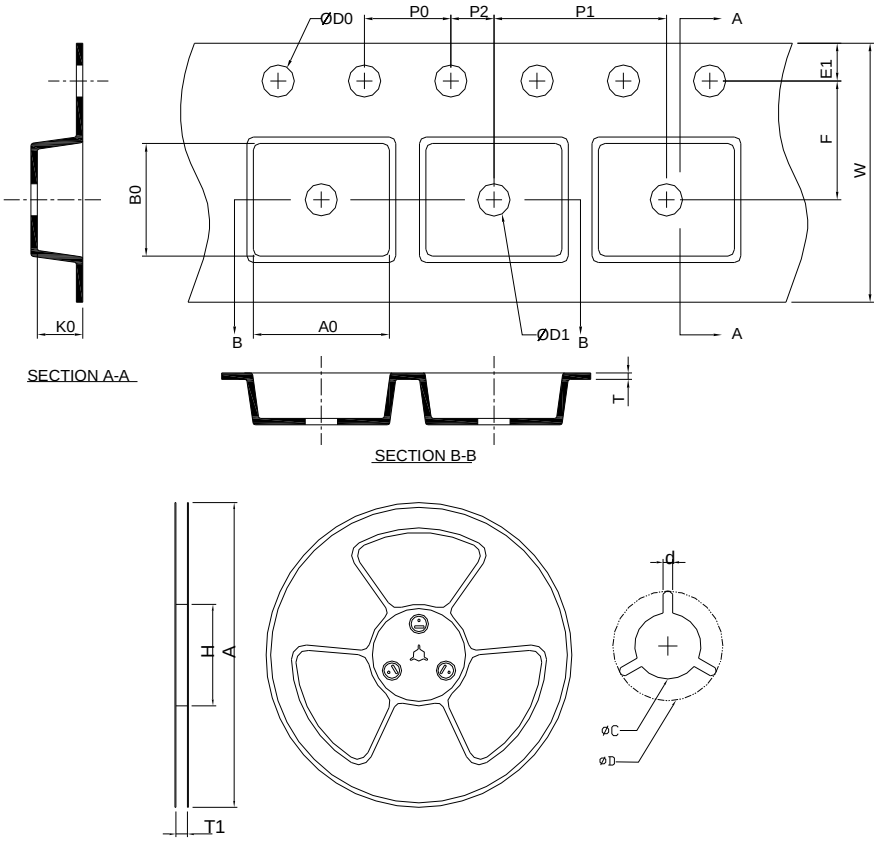
TQFN3x3-20



SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN3x3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

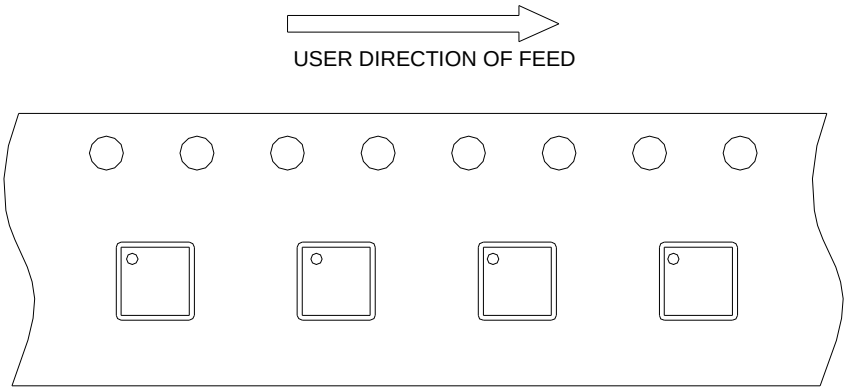
(mm)

Devices Per Unit

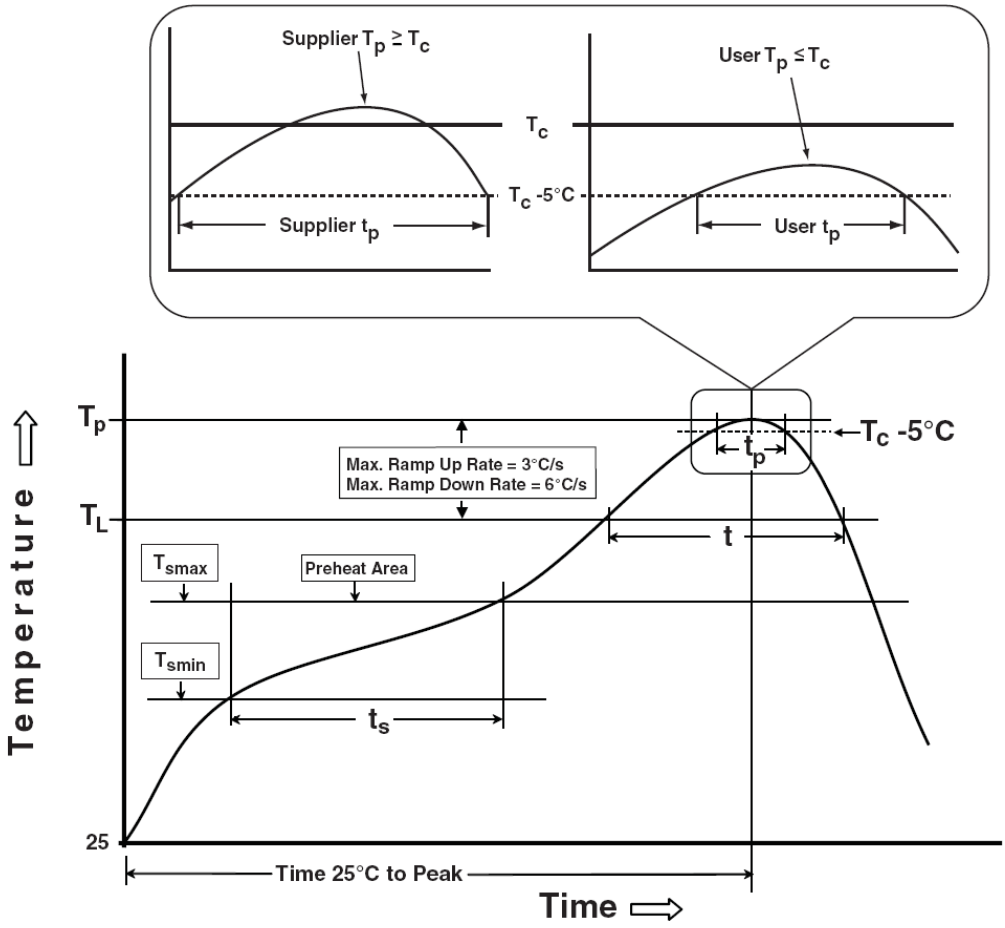
Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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