1.5MHz PMIC for Battery Powered System with I²C Controller

Features

■ Charger

- Available in Linear Mode or Switch Mode Charge
- High Efficiency 1.5A at Switch Mode Charge
- Single Input USB-compliant/Adapter Charge
  - Input Voltage and Current Limit Supports USB2.0 and USB3.0
  - Programmable Input Current Limit : 100mA, 500mA, 900mA, 1300mA, 1700mA, 2100mA , 2500mA
- 3.9V-6V Input Operating Voltage Range
  - Support Input Voltage DPM Regulation
- 1.5MHz Switching Frequency for Low Profile Inductor
- Autonomous Battery Charging with or without Host Management
  - Battery Charge Enable
  - Battery Charge Preconditioning
  - Charge Termination and Recharge
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±7% Charge Current Regulation
  - ±7.5% Input Current Regulation
- Safety
  - Battery Precharge and Fast Charg Safety Timer
  - Thermal Shutdown
  - Input Over-Voltage Protection
  - MOSFET Over-Current Protection

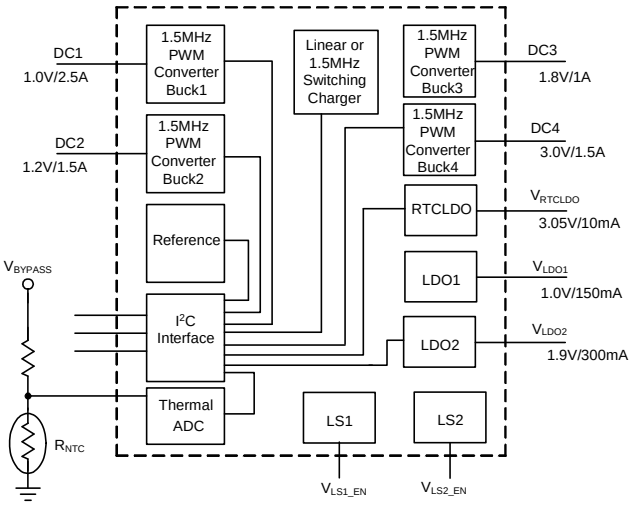
■ Voltage Rail

- Provide 4 Buck Single Phase PWM Converters
  - DC1: 0.6V - 1.5V at 2.5A
  - DC2: 0.6V - 3.3V at 1.5A
  - DC3: 0.6V - 3.3V at 1A
  - DC4: 0.6V - 3.3V at 1.5A
- Provide 3 LDO Output
  - RTCLDO 1.5V - 3.05V, 10mA
  - LDO1 0.6V - 3.3V, 150mA, Reference = 0.6V
  - LDO2 1.5V - 3.05V, 300mA, Controlled by I²C
- Provide 2 Load Switches Enable Signal
- 30㎂ Low Battery Leakage Current
- TQFN 5x5-40A Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- DSC/ DVR
- Action Camera
- Li-Ion battery powered devices

Simplified Application Circuit



General Description

The APW7703D is a Power Management IC (PMIC) with a battery powered system designed to provide complete Power Management solution for the camera applications. The IC operates from a single supply voltage of 2.7V to 5. 5V allowing it to be used in Adapter/USB or 1 Cell battery applications. The APW7703D is designed to provide maximum number of regulators in the smallest available cost effective package. Included in the IC are: One selectable linear mode or switch mode charger; Four switching Buck converters for DC1/DC2/DC3/DC4, Three LDOs for Image Signal Process and RTC applications, and Two Load Switch Enable Signal Control for Wi-Fi, DRAM applications. For Charger part, when the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode operation prevents overloading the input source. The devices initiate and complete a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The device provides various safety features for battery charging operation, including a pack negative thermistor monitoring, charging safety timer and over-voltage/over-current protections.

For the other VRs, the IC is equipped with all the standard protection features such as current limit, over voltage and internal under voltage lock out protection as well as thermal shutdown.

The serial interface is an I^2C communication interface which allows supply sequencing as well as controlled margining of ramp up and ramp down of all supplies to optimize battery power consumption. The I^2C interface also allows for adjustability of VRs' voltage and Forced PWM Mode in default operation and Auto PSM/PWM Mode in OFF mode state. Also, the power sequenc is defined by strobes and delay times under I^2C Control.

The device is available in a 40-pin, 5x5 mm^2 thin QFN package for best thermal performance while optimizing the cost.

Ordering and Marking Information

<table>
<tr>
<td>APW7703D □□-□□□
Assembly Material
Handling Code
Temperature Range
Package Code</td>
<td>Package Code
QB: TQFN5x5-40A
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device</td>
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<tr>
<td colspan="2">APW7703D QB : APW7703D XXXXX
XXXXX - Date Code</td>
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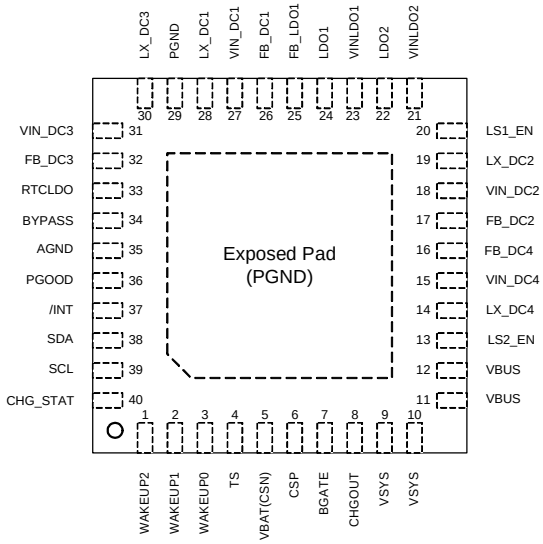
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{VBUS}	VBUS to GND Voltage	-0.3 ~ 20	V
V_{VSYS}	VSYS to GND Voltage	-0.3 ~ 6.5	V
	VIN_DC1, VIN_DC2, VIN_DC3, VIN_DC4, VINLDO1, VINLDO2, LS1_EN, LS2_EN to GND Voltage	-0.3 ~ 6.5	V
	LX_DC1, LX_DC2, LX_DC3, LX_DC4 to GND Voltage	-0.3 ~ 6.5	V
	FB_DC1, FB_DC2, FB_DC3, FB_DC4, RTCLDO, LDO1, LDO2, FB_LDO1 to GND Voltage	-0.3 ~ 6.5	V
	All other pins to GND Voltage	-0.3 ~ 6.5	V
	PGND to AGND	-0.3 ~ 0.3	V
P_D	Power Dissipation, T_A=25 °C	3.64	W
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	30	°C/W
θ_{JC}	Junction-to-Case Resistance in free air (Note 2)	6	°C/W

Note 2: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5x5-40A is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VBUS}	USB/Adapter Input Voltage	3.9~5.5	V
V_{VBAT}	Battery Voltage	2.7~4.4	V
V_{DC1}	Buck1 Output Voltage	0.6~1.5	V
I_{DC1}	Buck1Output Current	~2.5	A
V_{DC2}	Buck2 Output Voltage	0.6~3.3	V
I_{DC2}	Buck2 Output Current	~1.5	A
V_{DC3}	Buck3 Output Voltage	0.6~3.3	V
I_{DC3}	Buck3 Output Current	~1	A
V_{DC4}	Buck4 Output Voltage	0.6~3.3	V
I_{DC4}	Buck4 Output Current	~1.5	A
V_{RTCLDO}	RTCLDO Output Voltage	1.5 ~ 3.05	V
I_{RTCLDO}	RTCLDO Output Current	~10	mA
V_{LDO1}	LDO1 Output Voltage	0.6~3.3	V
I_{LDO1}	LDO1 Output Current	~150	mA
V_{LDO2}	LDO2 Output Voltage	1.5~3.3	V
I_{LDO2}	LDO2 Output Current	~300	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLO}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$, and T_A= -40 to 85°C. Typical values are at T_A=25°C.

· **Charger**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
QUIESCENT CURRENTS						
I_{BAT}	Battery Supply Current (BAT, CHGOUT, SYS)	All other rails disabled, No V_{BUS}, BGATE Enabled, V_{BAT}= 4.2V	-	32	55	μA
I_{VBUS}	Input Supply Current (VBUS)	V_{BUS}=5V, All other rails disabled, No Battery, RTCLDO enabled, No Load, T_A=-40~85℃	-	600	-	μA
		$V_{BAT} > V_{BATUVLO}$, $V_{BUS} - V_{BAT} > V_{SLEEPZ}$ (V_{BUS}=5V, V_{BAT}=4.2V), Charge converter not switching , All other rails disabled	-	4.5	6	mA
VBUS/BAT POWER UP, POWER POR						
V_{BUS}	USB Input Voltage Range	Valid range for charging	3.9	-	6	V
V_{BUS_POR}	USB Valid	V_{BUS} Rising	3.4	3.6	3.8	V
$V_{BUS\_POR\_HYS}$	USB Valid Hysteresis	V_{BUS} Falling	-	200	-	mV
V_{BAT}	Battery Input Voltage Range	USB is connected	0	-	5.5	V
		USB is not connected	2.7	-	5.5	V
V_{SLEEP}	Sleep Mode Falling Threshold	V_{VBUS} falling, V_{VBUS}-V_{BAT} (Into Sleep Mode)	35	80	120	mV
V_{SLEEPZ}	Sleep Mode Rising Threshold	V_{VBUS} rising, V_{VBUS}-V_{BAT} (Out of Sleep Mode)	170	250	300	mV
$V_{SYS\_POR\_R}$	VSYS UVLO Voltage Threshold	VSYS Rising	2.9	3.0	3.1	V
$V_{SYS\_POR\_F}$	VSYS UVLO Voltage Threshold	VSYS Falling	2.7	2.8	2.9	V
$V_{SYS\_POR\_HYS}$	VSYS UVLO Voltage Hysteresis		-	0.2	-	V
V_{ACOV}	USB Over Voltage Rising Threshold	V_{BUS} rising	6.2	6.4	6.6	V
V_{ACOV_HYS}	USB Over Voltage Falling Hysteresis	V_{BUS} falling	-	200	-	mV
POWER PATH MANAGEMENT`						
$R_{ON(RBFET)}$	Internal Top Reverse Blocking MOSFET On-Resistance Between VBUS and VSYS	Measured between VBUS and SYS, V_{BUS}=5V, I_{SYS}=1A	-	100	-	mΩ
$R_{ON(HSET)}$	Internal High Side MOSFET On-Resistance Between VSYS and CHGOUT	Measured between HS D-S Terminal volage, V_{BUS}=5V, I_{HS_DS}=1A	-	50	-	mΩ
V_{SYS_BAT}	SYS/BAT Comparator	V_{BAT} -$V_{SYS, VSYS}$ Faling	-	30	-	mV
BYPASS LDO						
V_{BYPASS}	BYPASS Output Voltage	V_{VBUS}=5V, I_{BYPASS}=0mA	-	4	-	V
		V_{VBUS}=5V, I_{BYPASS}=20mA	3	-	4.5	V
I_{BYPASS}	BYPASS Output Current	V_{VBUS}=5V, BYPASS Shortr to GND	-	40	-	mA
BATTERY CHARGER						
$V_{OREG\_ACC\_SW}$	Charge Voltage Regulation Accuracy	V_{BAT}= 4.208V, T_A= 25°C, Switch Mode	-0.5	-	0.5	%
$V_{OREG\_ACC\_LR}$		V_{BAT}= 4.208V, T_A= 25°C, Linear Mode	-1	-	1	%
	Charge Voltage Regulation Range	I^2C selectable; Default: 4.208V	3.504	-	4.464	V

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLO}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
BATTERY CHARGER (Cont.)						
$I_{CHG\_REG\_ACC\_SW}$	Switch Mode Fast Charge Current Regulation Accuracy	V_{BAT}= 3.8V, I_{CHG}= 1024mA, T_A= 25°C	-7	-	7	%
		V_{BAT}= 3.8V, I_{CHG}= 512mA , T_A= 25°C	-10	-	10	
		V_{BAT}= 3.8V, I_{CHG}= 128mA , T_A= 25°C	-20	-	20	
$I_{CHG\_REG\_ACC\_LR}$	Linear Mode Fast Charge Current Regulation Accuracy	V_{BAT}= 3.8V, I_{CHG}= 640mA, T_A= 25°C	-10		10	%
		V_{BAT}= 3.8V, I_{CHG}= 440mA , T_A= 25°C	-12		12	
		V_{BAT}= 3.8V, I_{CHG}= 255mA , T_A= 25°C	-15		15	
		V_{BAT}= 3.8V, I_{CHG}= 100mA , T_A= 25°C	-25		25	
I_{CHG_SW}	Switch Mode, R_{SNS}= 100mΩ, Battery Fast Chage Current Range, V_{OREG} > V_{BAT} > V_{LOWV}, V_{BUS}= 5V	ICHG[2:0]=000	-	128	-	mA
		ICHG[2:0]=001	-	256	-	
		ICHG[2:0]=010	-	384	-	
		ICHG[2:0]=011		512		
		ICHG[2:0]=100	-	640	-	
		ICHG[2:0]=101	-	768	-	
		ICHG[2:0]=110	-	896	-	
		ICHG[2:0]=111	-	1024	-	
I_{CHG_LR}	Linear Mode, Battery Fast Chage Current Range, V_{OREG} > V_{BAT} > V_{LOWV}, V_{BUS}= 5V	ICHG[2:0]=000	-	100	-	mA
		ICHG[2:0]=001	-	255	-	
		ICHG[2:0]=010	-	440	-	
		ICHG[2:0]=011		640		
$V_{BATLOWV\_F}$	Battery LOWV Falling Threshold	Fast charge to precharge, V_{BUS}=5V, VPRECHG= 0	2.4	2.6	2.8	V
$V_{BATLOWV\_R}$	Battery LOWV Rising Threshold	Precharge to fast charge, V_{BUS}=5V, VPRECHG= 0	2.6	2.8	3.0	V
$I_{PRECHG\_ACC\_SW}$	Switch Mode Precharge Current Regulation Accuracy	V_{BAT}= 2.6V, I_{PRECHG}= 128mA, T_A= 25°C	-20	-	20	%
$I_{PRECHG\_ACC\_LR}$	Linear Mode Precharge Current Regulation Accuracy	V_{BAT}= 2.6V, I_{PRECHG}= 100mA, T_A= 25°C	-25	-	25	%
	Switch Mode, R_{SNS}=100mΩ, Battery Precharge Chage Current Range, V_{BAT} < V_{LOWV}, V_{VBUS}=5V	IPRECHG[1:0]=00	-	64	-	mA
		IPRECHG[1:0]=01	-	128	-	
		IPRECHG[1:0]=10	-	192	-	
		IPRECHG[1:0]=11	-	256	-	
	Linear Mode, Battery Precharge Chage Current Range, V_{BAT} < V_{LOWV}, V_{VBUS}=5V	IPRECHG[1:0]=00	-	50	-	mA
		IPRECHG[1:0]=01	-	100	-	
		IPRECHG[1:0]=10	-	180	-	
		IPRECHG[1:0]=11	-	255	-	
I_{TERM_ACC}	Linear/Switch Mode Termination Current Regulation Accuracy	I_{TERM}=256mA, I_{CHG}=1024mA, T_A= 25°C	-22.5	-	22.5	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLO}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW7703D			Unit
				Min	Typ	Max	
BATTERY CHARGER (Cont.)							
	Linear Mode, or Switch Mode, R_{SNS}=100mΩ, Charge Current Value for Termination Detection Threshold	ITERM[1:0]=00		-	64	-	mA
		ITERM[1:0]=01		-	128	-	
		ITERM[1:0]=10		-	192	-	
		ITERM[1:0]=11		-	256	-	
	Termination Deglitch Time			-	125	-	ms
V_{BAT_SHORT}	Battery Short Voltage	V_{BAT} falling (into Battery Short State)		-	2	-	V
$V_{BAT\_SHORT\_HYS}$	Battery Short Voltage Hysteresis	V_{BAT} rising (Out of Battery Short State)		-	200	-	mV
I_{SHORT}	Battery Short Current	V_{BAT} < 2.0V (In Battery Short State)		-	32	-	mA
V_{RECHG}	Recharge Threshold Below V_{BAT_REG}	V_{BAT} falling, After Charge Termination, V_{BAT}=4.208V		70	100	150	mV
t_{RECHG}	Recharge Deglitch Time	V_{BAT} falling		-	125	-	ms
INPUT VOLTAGE/CURRENT REGULATION							
V_{INDPM_ACC}	Input Voltage Regulation Accuracy	VINDPM = 4.5V (Default)		-2	-	2	%
	Threshold at which DPM Loop Enabled	I^2C Selectable		4.4	-	4.7	V
	Input Current Limit	IVBUS [2:0]=000		50	-	150	mA
		IVBUS [2:0]=001		400	-	600	mA
		IVBUS [2:0]=010		750	-	900	mA
		IVBUS [2:0]=011		1080	-	1300	mA
		IVBUS [2:0]=100		1410	-	1700	mA
		IVBUS [2:0]=101		1740	-	2100	mA
		IVBUS [2:0]=110		2000	-	2500	mA
BATTERY OVER-VOLTAGE PROTECTION							
V_{BATOVP}	Battery Over-Voltage Threshold	V_{BAT} rising, as percentage of V_{BAT_REG}, V_{BAT}= 4.208V		-	106	-	%
V_{BATOVP_HYS}	Battery Over-Voltage Hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}, V_{BAT}= 4.208V		-	3	-	%
t_{BATOVP}	Battery Over-Voltage Deglitch Time To Disable Charge			-	1	-	μs
BATTERY NTC MONITOR							
R_{NTC_PU}	Pull-up resistor from thermistor to bypass	NTC= 10k (β=3380)		-	10	-	kΩ
	Accuracy	T_A= 25°C		-3	-	3	%
V_{LTH}	Low temp failure threshold	Temperature falling	TRANGE= 0/1 (0°C)	-	73.9	-	%
		Temperature rising		-	72.1	-	
V_{HTH}	High temp failure threshold	Temperature falling	TRANGE= 0 (45°C)	-	34.4	-	%
		Temperature rising		-	32.9	-	
		Temperature falling	TRANGE= 1 (60°C)	-	24.4	-	
		Temperature rising		-	23.3	-	

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLO}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW7703D			Unit
				Min	Typ	Max	
BATTERY NTC MONITOR (Cont.)							
V_{DIS}	Discharge temperature threshold	Temperature falling	TRANGE= 0 (55℃)	-	27.4	-	%
		Temperature rising		-	26.2	-	
		Temperature falling	TRANGE= 1 (70℃)	-	19.3	-	
		Temperature rising		-	18.4	-	
T_{DET}	Thermistor Detect Degritch Time			-	10	-	ms
THERMAL SHUTDOWN							
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature increasing		-	160	-	°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis			-	30	-	°C
OVER TEMPERATURE AUTO-DISCHARGE CIRCUIT							
V_{DISCH_ON}	Discharge turn-on threshold Voltage	Turn on discharging at high temp if battery voltage is above (DIS_EN= 1)		-	3.9	-	V
V_{DISCH_HYS}	Discharge Hysteresis	Discharge hysteresis when VBAT Drops; I^2C Selectable; DISOFF=1		-	0.1	-	V
		Discharge hysteresis when VBAT Drops; I^2C Selectable; DISOFF=0		-	0.2	-	V
R_{DISCH}	Automatic discharge resistor	Battery temp above discharge threshold ((V_{TS}≦V_{DIS})), RDIS=0		56	80	104	Ω
		Battery temp above discharge threshold ((V_{TS}≦V_{DIS})), RDIS=1		140	200	260	Ω
CHARGE OVER-CURRENT COMPARATOR							
I_{HSFET_OCP}	HSFET Over-Current Threshold			3	4	-	A
PWM OPERATION							
F_{SW}	PWM Switching Frequency			1.3	1.5	1.7	MHz
	PWM Switching Frequency Accuracy	-40 ~ 85°C		-10	-	10	%
I_{CHGOUT_LEAK}	CHGOUT Leakage Current	V_{SYS}=V_{CHGOUT}=5V, Charger is disable		-	-	1	μA
I/O PIN CHARACTERISTICS (SDA, SCL, /INT, ADD_SEL, CSN, CSP, WAKEUP0, WAKEUP1, WAKEUP2, PGOOD)							
V_{IL}	Input Low Voltage	Include SDA, SCL, /INT, WAKEUP0, WAKEUP1, WAKEUP2 Input Pins		-	-	0.4	V
V_{IH}	Input High Voltage	Include SDA, SCL, /INT, WAKEUP0, WAKEUP1, WAKEUP2 Input Pins		1.5	-	-	V
V_{O_LOW}	Output Low Saturation Voltage	Sink current=5mA Include PGOOD, /INT Pins		-	-	0.4	V
I_{BIAS_IO}	High Level Leakage Current	Pull up to 5V, Include SDA, SCL Input Pins		-	-	1	μA
		Pull up to 5V, Include WAKEUP0, WAKEUP1, WAKEUP2 Input Pins		-	50	-	μA
		Pull up to 5V, Include PGOOD and /INT Input Pins		-	-	0.2	μA
T_{INT_L}	/INT Pulled Low Time	/INT Pulled Low Time When Fault Event still Exists. The Period is 1ms		-	10	-	μs
f_{SCL}	SCL Clock Frequency			-	-	400	kHz

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{VBUS\_UVLO}<V_{VBUS}<V_{ACOV}$ and $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$, and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
PGOOD Definition (Relative with all DC/DC Converters, Load Switch and LDOs)						
	PGOOD Delay Time	Default, All VRs are regulated	-	16	-	ms
	WAKEUP0 Hard Reset Detect Time	RSTTMR_EN =0	-	8	-	sec
	VBUS POR OKAY to Wakupx Enable Delay Time		-	150	-	µs
	VBUS POR OKAY to VR Starts to Rise Up Delay Time	From Wakeupx Has Enabled First to DC1 Starts to Rise Up Period, No Battery	-	50	-	ms
	WAKEUP0/1/2 Deglitch Time	Minimum WAKEUPx Pulsed Width	500	-	-	µs
Timing Requirement						
	Precharge Timer, Thermal and DPM Loop Not Active. Selectable by I^2C	PCHRGT=0	-	30	-	min
		PCHRGT=1	-	60	-	min
	Charge Safety Timer, Thermal and DPM Loop Not Active. Selectable by I^2C		4	-	10	hr

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC1= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **BUCK1**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
$I_{Q\_NSW\_DC1}$	Consumption Current (No Switching Current)	VIN_DC1=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC1}$	Switching Current	VIN_DC1 = 5V, In Switching	-	5	-	mA
I_{SHUN_DC1}	Shutdown IQ	VIN_DC1 = 5V , In Shutdown		-	1	μA
V_{REF_DC1}	FB_DC1 Voltage	Selectable in I^2C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC1}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC1}=1V, I_{OUT_DC1}= 0.75A~2.5A	-	0.3	-	%/A
		V_{OUT_DC1} = 1V, I_{OUT_DC1} = 0.1A~2.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC1 = 2.7V to 5.5V, V_{OUT_DC1}=1V, I_{OUT_DC1} = 2.5A	-	0.4	-	%/V
I_{CL_DC1}	Current Limit	T_A=-40℃ ~ 85℃	3.8	4	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC1}	Switching Frequency	I_{OUT_DC1}=0A, Force PWM, T_A=-40℃ ~ 85℃	1350	1500	1650	KHz
		I_{OUT_DC1}=2.5A, T_A=-40℃ ~ 85℃	1275	1500	1725	KHz
D_{MAX_DC1}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC1}$	Minimum On Time		-	60	-	ns
T_{SS_DC1}	Soft Start	VIN_DC1=5V,V_{OUT_DC1}=1V, 0 to 95% of V_{OUT_DC1}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC1}$	High Side Ron	I_{OUT_DC1}=100mA	-	100	-	mΩ
$R_{DS(ON)\_L\_DC1}$	Low Side Ron	I_{OUT_DC1}=100mA	-	35	-	mΩ
R_{DIS_DC1}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	persentage of regulation voltage	60	70	80	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC2= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **BUCK2**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
$I_{Q\_NSW\_DC2}$	Consumption Current (No Switching Current)	VIN_DC2=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC2}$	Switching Current	VIN_DC2 = 5V, In Switching	-	5	-	mA
I_{SHUN_DC2}	Shutdown IQ	VIN_DC2 = 5V , In Shutdown		-	1	μA
V_{REF_DC2}	FB_DC2 Voltage	Selectable in I^2C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC2}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC2}=1.2V, I_{OUT_DC2}= 0.5A~1.5A	-	0.3	-	%/A
		V_{OUT_DC2} = 1.2V, I_{OUT_DC2}=0.1A~1.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC2=2.7V to 5.5V, V_{OUT_DC2}=1.2V, I_{OUT_DC2}=1.5A	-	0.4	-	%/V
I_{CL_DC2}	Current Limit	T_A=-40℃ ~ 85℃	2.2	3	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC2}	Switching Frequency	I_{OUT_DC2}=0A, Force PWM, T_A=-40℃ ~ 85℃	1350	1500	1650	KHz
		I_{OUT_DC2}=1.5A, T_A=-40℃ ~ 85℃	1275	1500	1725	KHz
D_{MAX_DC2}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC2}$	Minimum On Time		-	60	-	ns
T_{SS_DC2}	Soft Start	V_{OUT_DC2}=1.2V, 0 to 95% of V_{OUT_DC2}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC2}$	High Side Ron	I_{OUT_DC2}=100mA	-	130	-	mΩ
$R_{DS(ON)\_L\_DC2}$	Low Side Ron	I_{OUT_DC2}=100mA	-	65	-	mΩ
R_{DIS_DC2}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	persentage of regulation voltage	60	70	80	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC3= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **BUCK3**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
$I_{Q\_NSW\_DC3}$	Consumption Current (No Switching Current)	VIN_DC3=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC3}$	Switching Current	VIN_DC3 = 5V, In Switching	-	5	-	mA
I_{SHUN_DC3}	Shutdown IQ	VIN_DC3 = 5V , In Shutdown	-	-	1	μA
V_{REF_DC3}	FB_DC3 Voltage	Selectable in I^2C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC3}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC3}=3V, I_{OUT_DC3}= 0.25A~1A	-	0.3	-	%/A
		V_{OUT_DC3} = 1.8V, I_{OUT_DC3} = 10mA~1A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC3 = 2.7V to 5.5V, V_{OUT_DC3}=1.8V, I_{OUT_DC3} = 1A	-	0.4	-	%/V
I_{CL_DC3}	Current Limit	T_A=-40℃ ~ 85℃	1.75	2	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC3}	Switching Frequency	I_{OUT_DC3}=0A, Force PWM, T_A=-40℃ ~ 85℃	1350	1500	1650	KHz
		I_{OUT_DC3}=1A, T_A=-40℃ ~ 85℃	1275	1500	1725	KHz
D_{MAX_DC3}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC3}$	Minimum On Time		-	60	-	ns
T_{SS_DC3}	Soft Start	V_{OUT_DC3}=1.8V, 0 to 95% of V_{OUT_DC3}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC3}$	High Side Ron	I_{OUT_DC3}=100mA	-	210	-	mΩ
$R_{DS(ON)\_L\_DC3}$	Low Side Ron	I_{OUT_DC3}=100mA	-	105	-	mΩ
R_{DIS_DC3}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	persentage of regulation voltage	60	70	80	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VIN_DC4= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **BUCK4**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
$I_{Q\_NSW\_DC4}$	Consumption Current (No Switching Current)	VIN_DC4=5V, No Load, No Switching	-	40	-	μA
$I_{Q\_SW\_DC4}$	Switching Current	VIN_DC4 = 5V, In Switching	-	5	-	mA
I_{SHUN_DC4}	Shutdown IQ	VIN_DC4 = 5V , In Shutdown		-	1	μA
V_{REF_DC4}	FB_DC4 Voltage	Selectable in I^2C	0.555	-	0.66	V
		Feedback Voltage step	-	15	-	mV
		Voltage Accuracy, V_{FB_DC4}=0.6V	-2	-	2	%
	DC Load Regulation	V_{OUT_DC4}=3V, I_{OUT_DC4}= 0.5A~1.5A	-	0.3	-	%/A
		V_{OUT_DC4} = 3V, I_{OUT_DC4} = 0.1A~1.5A	-	0.6	-	%/A
	DC Line Regulation	VIN_DC4 = 2.7V to 5.5V, V_{OUT_DC4}=3V, I_{OUT_DC4} = 1.5A	-	0.4	-	%/V
I_{CL_DC4}	Current Limit	T_A=-40℃ ~ 85℃	2.2	3	-	A
	PSM Peak Current	PSM Inductor Current Peak Value	-	0.5	-	A
F_{SW_DC4}	Switching Frequency	VIN_DC4=2.7V to 5.5V, I_{OUT_DC4}=0A, Force PWM, T_A=-40℃ ~ 85℃	1350	1500	1650	KHz
		VIN_DC4=2.7V to 5.5V, I_{OUT_DC4}=1.5A, T_A=-40℃ ~ 85℃	1275	1500	1725	KHz
D_{MAX_DC4}	Maximum Duty Cycle		-	-	100	%
$T_{ON\_MIN\_DC4}$	Minimum On Time		-	60	-	ns
T_{SS_DC4}	Soft Start	VIN=5V,V_{OUT_DC4}=3V, 0 to 95% of V_{OUT_DC4}, No load	-	750	-	μs
$R_{DS(ON)\_H\_DC4}$	High Side Ron	VIN_DC4=2.7V, I_{OUT_DC4}=100mA	-	130	-	mΩ
$R_{DS(ON)\_L\_DC4}$	Low Side Ron	VIN_DC4=2.7V, I_{OUT_DC4}=100mA	-	65	-	mΩ
R_{DIS_DC4}	Output Discharge Resistor		-	250	-	Ω
	Output Voltage UVP	persentage of regulation voltage	60	70	80	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VSYS= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **RTCLDO**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
	RTCLDO Output Voltage	Adjustable by I^2C	1.5	-	3.05	V
I_{RTCLDO_Max}	RTCLDO Source Capability	V_{VIN_RTCLDO}=3.7V, V_{OUT_RTCLDO} =3.05V	-	-	10	mA
	DC Output Voltage Accuracy	I_{OUT_RTCLDO}=10mA, V_{VIN_RTCLDO}> V_{OUT_RTCLDO}+150mV, V_{OUT_RTCLDO}=3.05V	-3	-	3	%
	Load Regulation	I_{OUT_RTCLDO}=0mA~10mA, V_{VIN_RTCLDO}=3.7V, V_{OUT_RTCLDO} =3.05V	-3	-	3	%
	Line Regulation	V_{VIN_RTCLDO}=3.7V~5V, I_{OUT_RTCLDO}=10mA, V_{OUT_RTCLDO}=3.05V	-3	-	3	%
$V_{DROPOUT\_RTC}$	VSYS-VOUT_RTCLDO Dropout Voltage	I_{OUT_RTCLDO}=10mA, V_{OUT_RTCLDO}=3.05V, T_A=25℃	-	150	200	mV
		T_J= -40 ~125℃	-	200	265	mV
I_{CL_RTC}	Short Circuit Current Limit	$V_{OUT\_RTCLOD1}$ Short to GND, V_{VIN_RTCLDO}=5V	-	150	-	mA
$R_{DS(ON)\_RTC}$	R_LDORTC		-	10	-	Ω

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VINLDO1= 1.9V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **LDO1**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
	LDO1 Output Voltage Range	Output Adjustable, V_{FB_LDO1}=0.6V	0.6	-	3.3	V
	DC Output Voltage Accuracy	I_{LDO1}=10mA, $V_{VINLDO1}$ > V_{LDO1}+30mV,	-2	-	2	%
	Load Regulation	I_{LDO1}=0mA to 150mA, $V_{VINLDO1}$=1.9V, V_{LDO1} =1.0V	-1.5	-	1.5	%
	Line Regulation	$V_{VINLDO1}$=1.9V to 5V, I_{LDO1}=150mA, V_{LDO1}=1.0V	-1.5	-	1.5	%
	VINLDO1 POR Voltage Threshold	VINLDO1 Rising	0.9	1	1.1	V
	VINLDO1 POR Voltage Hysteresis	VINLDO1 Falling	-	0.2	-	V
$V_{DROPOUT\_LDO1}$	VINLDO1-VLDO1 Dropout Voltage	I_{LDO1}=150mA, $V_{VINLDO1}$=1.9V, T_A=25°C	-	-	650	mV
I_{CL_LDO1}	Short Circuit Current Limit	V_{LDO1} Short to GND, $V_{VINLDO1}$=5V	260	300	-	mA
	Output Voltage UVP	persentage of regulation voltage	40	50	60	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%
T_{SS_LDO1}	Soft Start Time	Time to Ramp V_{LDO1} from 5% to 95%, No Load	-	150	-	μs
R_{DIS_LDO1}	Discharge Resistor	Internal Discharge resistor when shutdown occur	100	375	500	Ω
$R_{DS(ON)\_LDO1}$	LDO1 $R_{DS(ON)}$		-	3	-	Ω
	PSRR	frequency=1kHz, , $V_{VINLDO1}$=1.9V, V_{LDO1}=1.0V loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over VINLDO2= 5V, T_J= -40 to 85°C, Typical values are at T_J=25°C.

· **LDO2**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
	LDO2 Output Voltage Range	Output Adjustable by I^2C	1.5	-	3.3	V
	DC Output Voltage Accuracy	I_{LDO2}=10mA, $V_{VINLDO2}$ > V_{LDO2}+20mV,	-2	-	2	%
	Load Regulation	I_{LDO2}=0mA to 300mA, $V_{VINLDO2}$=3.3V, V_{LDO2} =1.9V	-1.5	-	1.5	%
	Line Regulation	$V_{VINLDO2}$=3.3V to 5.5V, I_{LDO2}=300mA, V_{LDO2}=1.9V	-1	-	1	%
$V_{DROPOUT\_LDO2}$	VINLDO2-VLDO2 Dropout Voltage	I_{LDO2}=300mA, $V_{VINLDO2}$=3.3V, T_A=25℃	-	-	900	mV
I_{CL_LDO2}	Short Circuit Current Limit	V_{LOD2} Short to GND, $V_{VINLDO2}$=5V	350	450	-	mA
	Output Voltage UVP	persentage of regulation voltage	40	50	60	%
	Output Voltage OVP	persentage of regulation voltage	120	125	130	%
T_{SS_LDO2}	Soft Start Time	Time to Ramp V_{LDO2} from 5% to 95%, No Load	-	150	-	μs
R_{DIS_LDO2}	Discharge Resistor	Internal Discharge resistor when shutdown occur	100	375	500	Ω
$R_{DS(ON)\_LDO2}$	LDO2 $R_{DS(ON)}$		-	2	-	Ω
	PSRR	frequency=1kHz, $V_{VINLDO2}$=3.3V, V_{LDO2}=1.9V loading=10mA	-70	-	-	dB

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over T_J= -40 to 85°C, Typical values are at T_J=25°C.

External Load Switch, Use LS1/2_EN to be an enable trigger signal

· **LS1/2**

Symbol	Parameter	Test Conditions	APW7703D			Unit
			Min	Typ	Max	
V_{LDO_LS}	Internal LDO Voltage	Supply source from V_{SYS}, No Load	2.5	3	3.5	V
V_{OH}	Output High Voltage	LS_ENx Voltage High Range, ILS_ENx=0mA, supply source is the internal LDO output V_{LDO_LS}	2.5	3	3.5	V
V_{OL}	Output Low Voltage	LS_ENx Voltage Low Range	-	0	-	V
	V_{LDO_LS} - V_{LS_ENx} Dropout Voltage	I_{LS_ENx}=5mA, V_{SYS}=3.6V, T_A=25℃	-	150	300	mV
		T_J= -40 ~ 125℃	-	225	400	mV
R_{LDO_LS}	VSYS to V_{LDO_LS} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Source}	V_{LDO_LS} to V_{LS_ENx} $R_{DS(ON)}$		-	30	-	Ω
R_{LS_Sink}	Output Sink Capability		-	6	-	Ω
	Short Circuit Current Limit	V_{LS_ENx} Short to GND, V_{SYS}=3.6V	-	30	-	mA
	LS_ENx pin pulled low resistor		-	10	-	kΩ

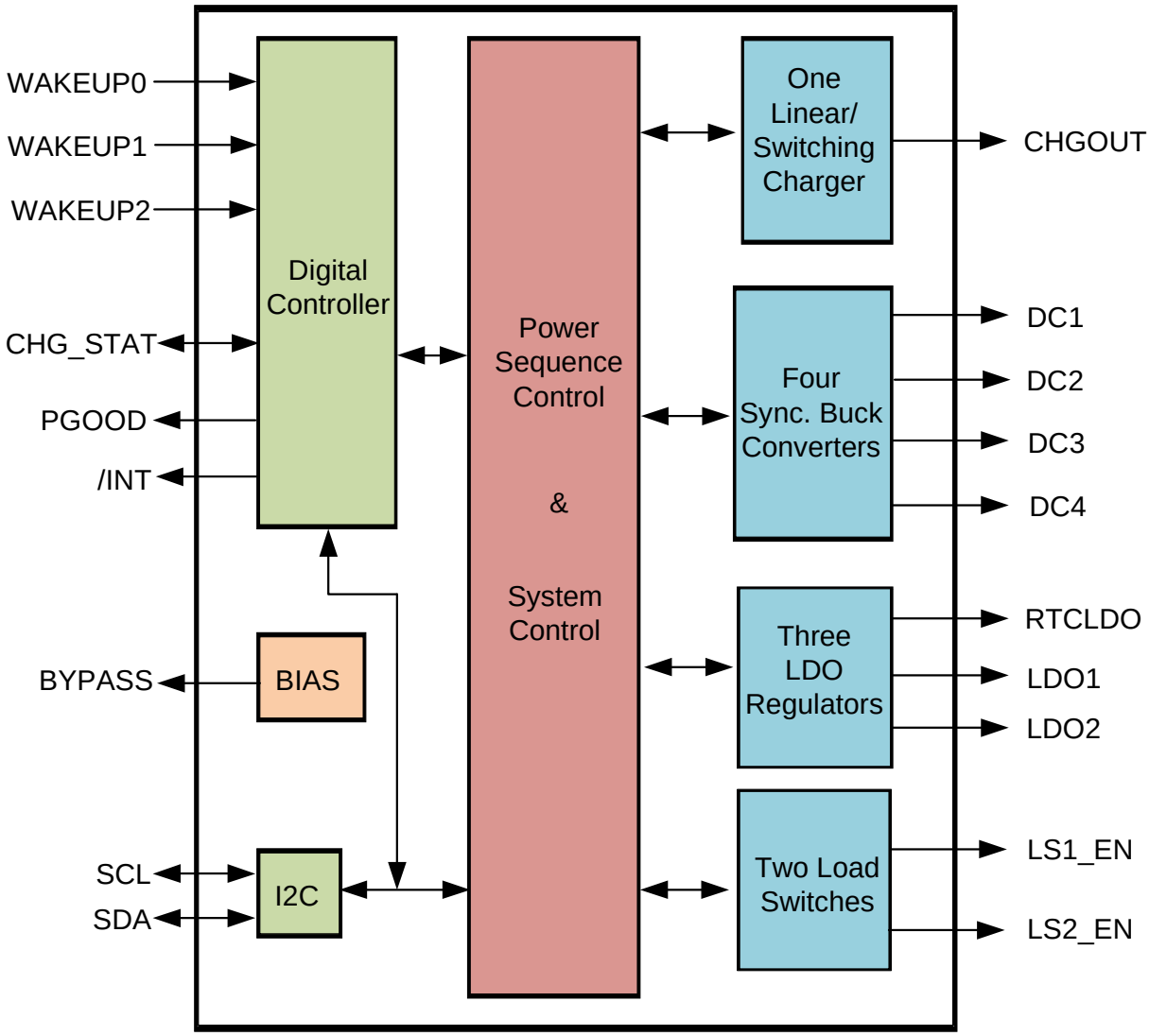
Pin Description

PIN		FUNCTION
NO.	NAME	
1	WAKEUP2	Input wake up pin to startup the PMIC with a power on event (pulse high)
2	WAKEUP1	Input wake up pin to startup the PMIC with a power on event (pulse high)
3	WAKEUP0	Push-Button input pin. When the pin signal is triggered from low to high, the device starts to power up.
4	TS	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from BYPASS to TS pin with 10kΩ. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor.
5	VBAT(CSN)	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between VBAT and VSYS. Connect a 10µF closely to the VBAT pin
6	CSP	Positive Input of current sensing Amplifier for charge terminal. A 0.1µF ceramic capacitor is placed from CSP to VBAT (CSN) to provide differential-mode filtering. An optional 0.1µF ceramic capacitor is placed from CSP pin to PGND for common-mode filtering.
7	BGATE	The pin drives the gate of an external P-channel MOSFET for the discharge path from battery to system.
8	CHGOUT	In switching mode, junction point of the Internal high-side MOSFET Source, output filter inductor and the cathode of the low-side Diode. In linear mode, connet the CHGOUT and VBAT (CSN) togather
9, 10	VSYS	System connection point. The external MOSFET is connected between VBAT and VSYS by BGATE Driver signal controled.
11, 12	VBUS	Charger input voltage. The internal MOSFET (RBFET) is connected between VBUS and VSYS with VBUS on source. Place a 10µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC.
13	LS2_EN	Load switch 2 output enable pin.
14	LX_DC4	DC4 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
15	VIN_DC4	DC4 PWM converter Input Pin.
16	FB_DC4	DC4 output feedback voltage pin.
17	FB_DC2	DC2 output feedback voltage pin.
18	VIN_DC2	DC2 PWM converter Input Pin.
19	LX_DC2	DC2 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
20	LS1_EN	Load switch 1 output enable pin.
21	VINLDO2	LDO2 input voltage pin.
22	LDO2	LDO2 output voltage pin.
23	VINLDO1	LDO1 input voltage pin.
24	LDO1	LDO1 output voltage pin.
25	FB_LDO1	LDO1 output feedback voltage pin. The LDO1 internal reference is 0.6V.
26	FB_DC1	DC1 output feedback voltage pin.
27	VIN_DC1	DC1 PWM converter Input Pin.
28	LX_DC1	DC1 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
29	PGND	Power ground connection for high-current power converter node. Internally, PGND is connected to the anode of the low side diode. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog AGND near the IC PGND pin.
30	LX_DC3	DC3 PWM Regulator LX Pin. Connect to external inductor for output LC filter.
31	VIN_DC3	DC3 PWM converter Input Pin.
32	FB_DC3	DC3 output feedback voltage pin.
33	RTCLDO	RTCLDO output voltage pin. The pin voltage is adjustable by I^2C.
34	BYPASS	Intenal bias voltage. It could be the source of resistor-divider for NTC circuit sensing.

Pin Description (Cont.)

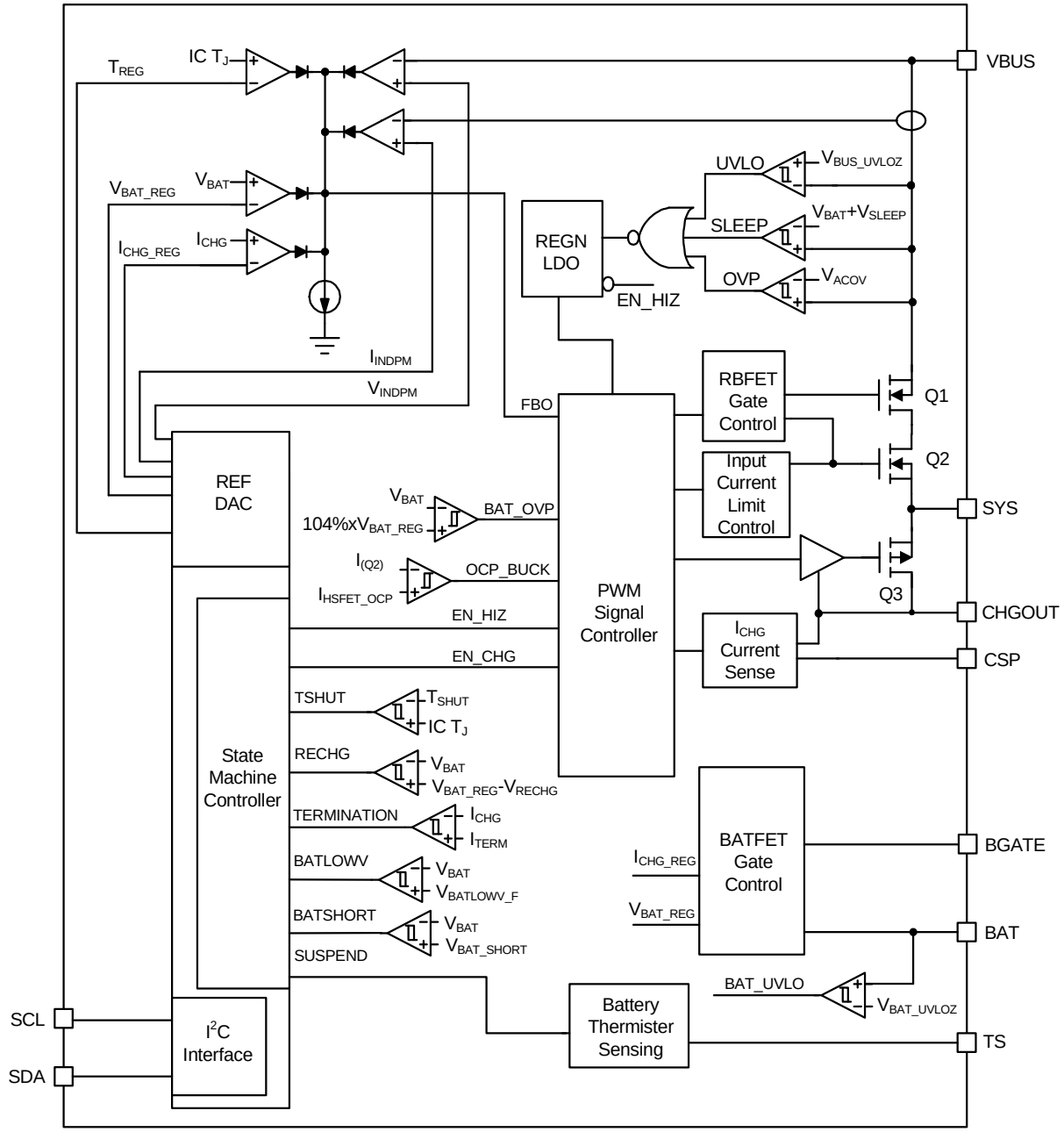
PIN		FUNCTION
NO.	NAME	
35	AGND	IC Analog ground.
36	PGOOD	Power Good Indicator. Pulled low when either buck converter output is out of regulation.
37	/INT	Open interrupt output. Connect the /INT to the pull up rail via 10kΩ resistor. The /INT pin sends active low, 10μs pulse to host to report charger device status and fault.
38	SDA	I^2C interface data.
39	SCL	I^2C interface clock.
40	CHG_STAT	CHG_STAT is an open drain output used to indicate the status of the various charger operations. When charge in progress, the CHG_STAT is pulled low. CHG_STAT can be used to drive a LED or communicate with a host processor.

Block Diagram



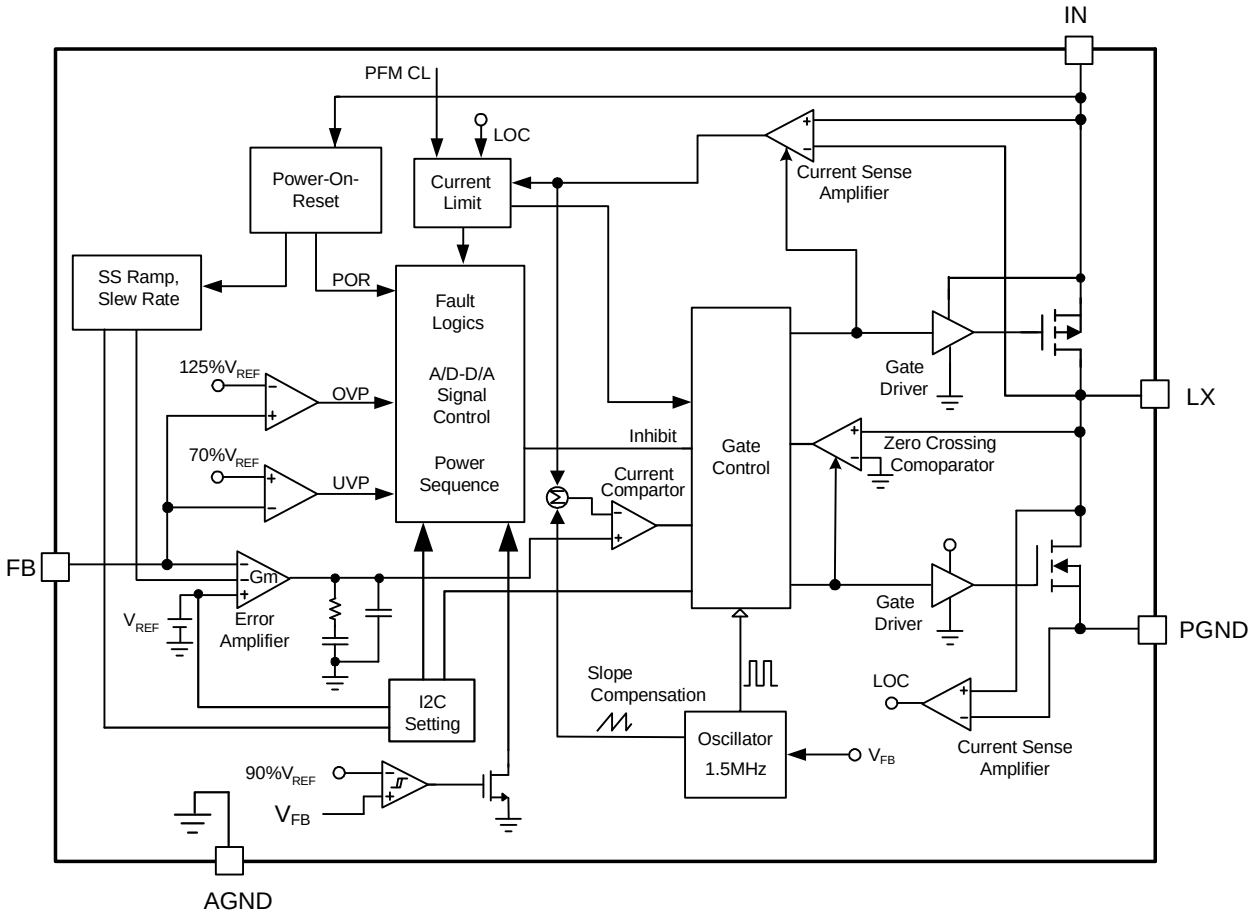
Block Diagram (Cont.)

Charger



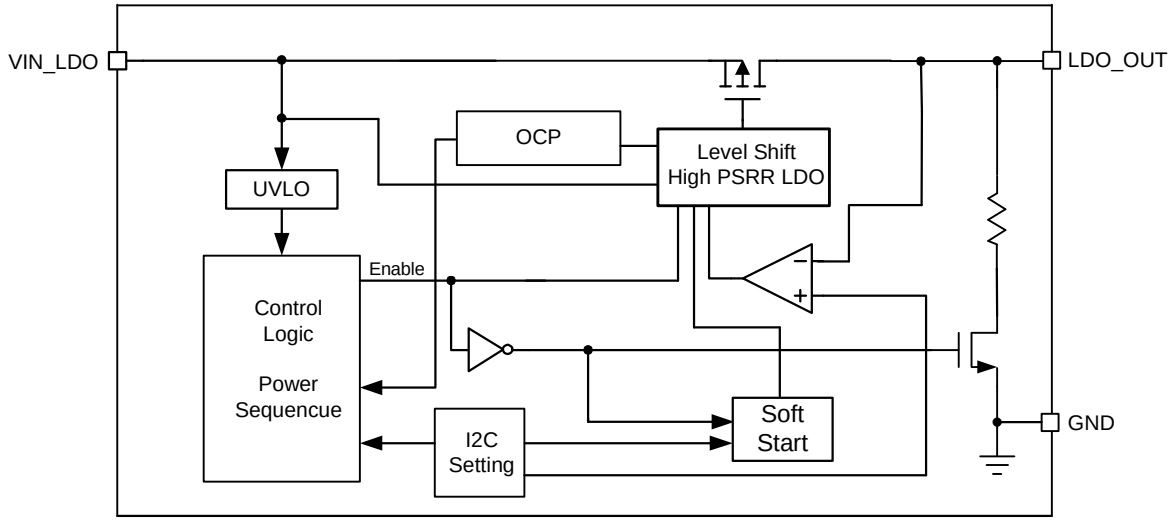
Block Diagram (Cont.)

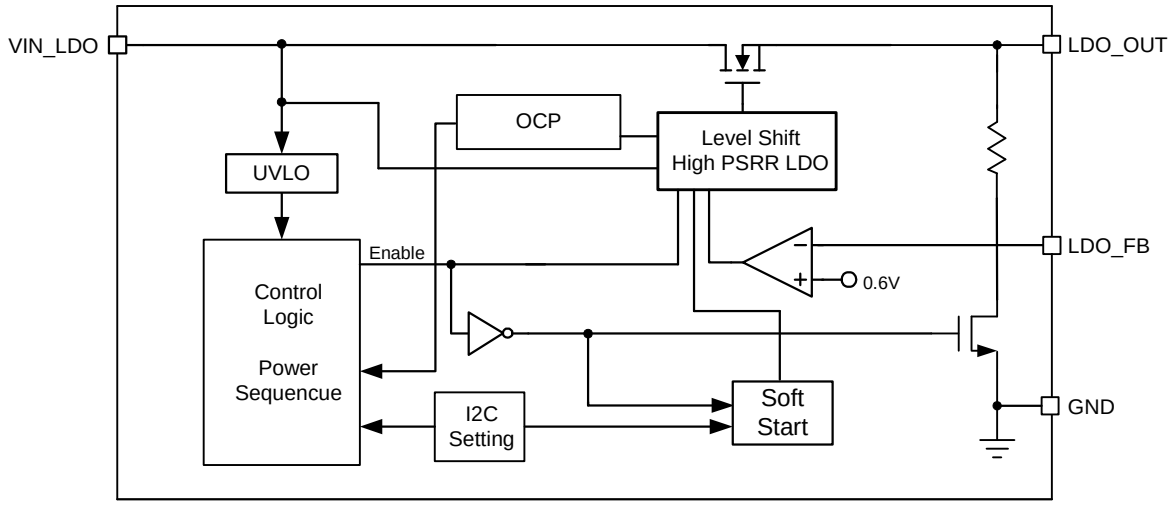
Buck Converter



Block Diagram (Cont.)

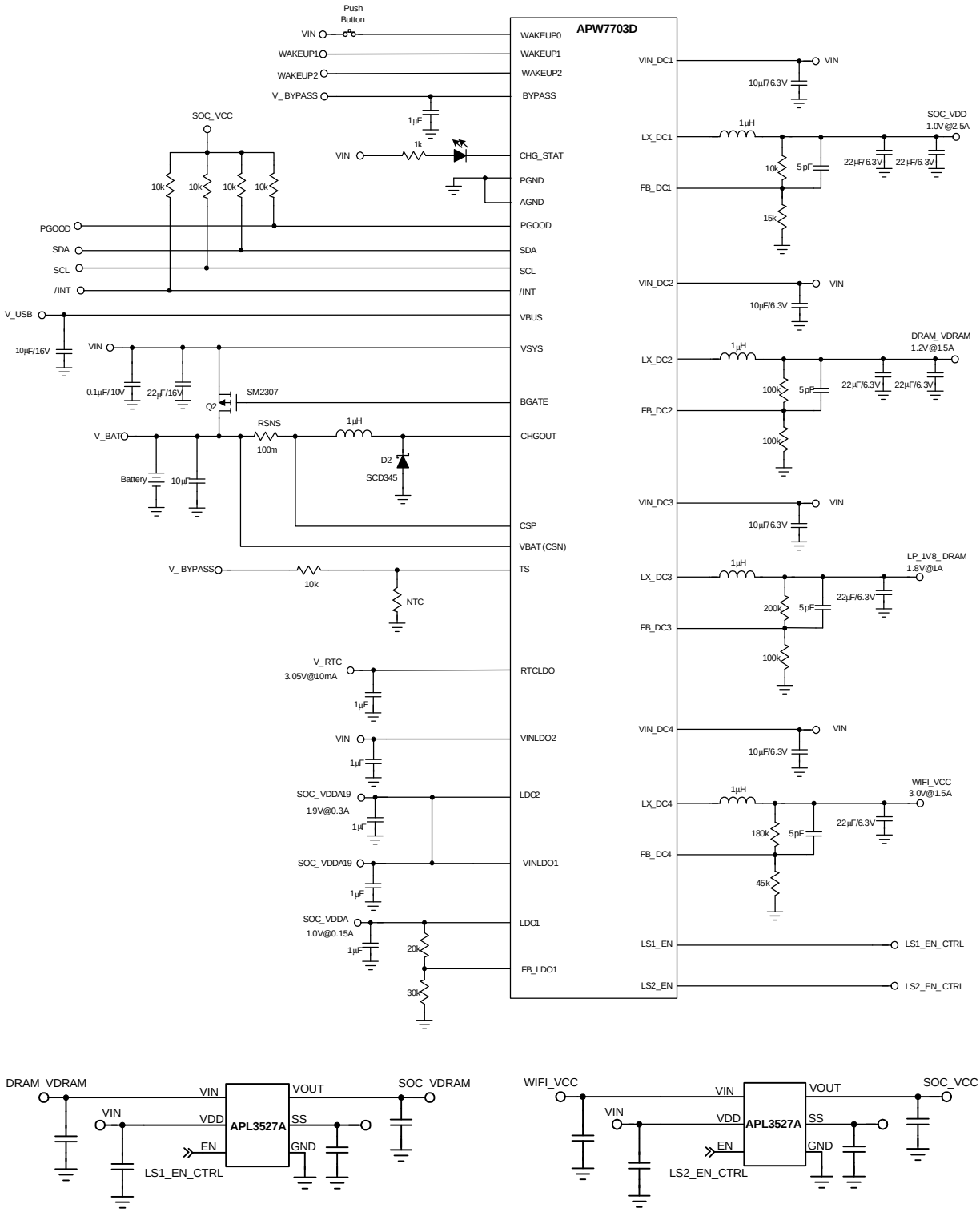
LDO





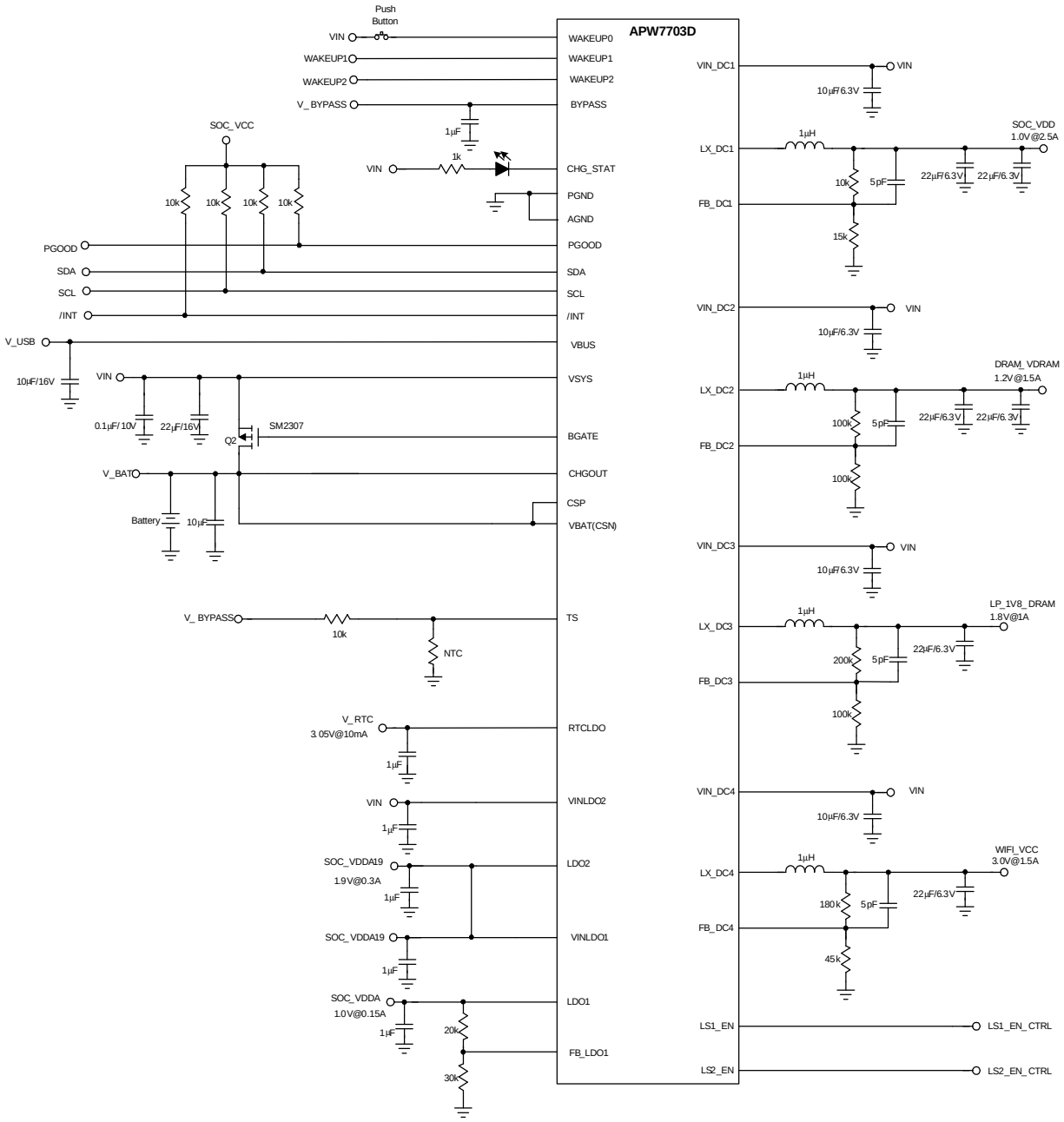
Typical Application Circuit

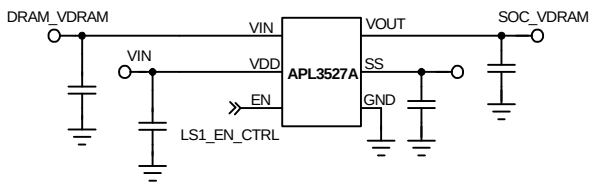
- **Switching Charger**

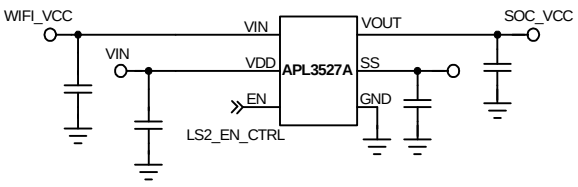


Typical Application Circuit

- **Linear Charger**

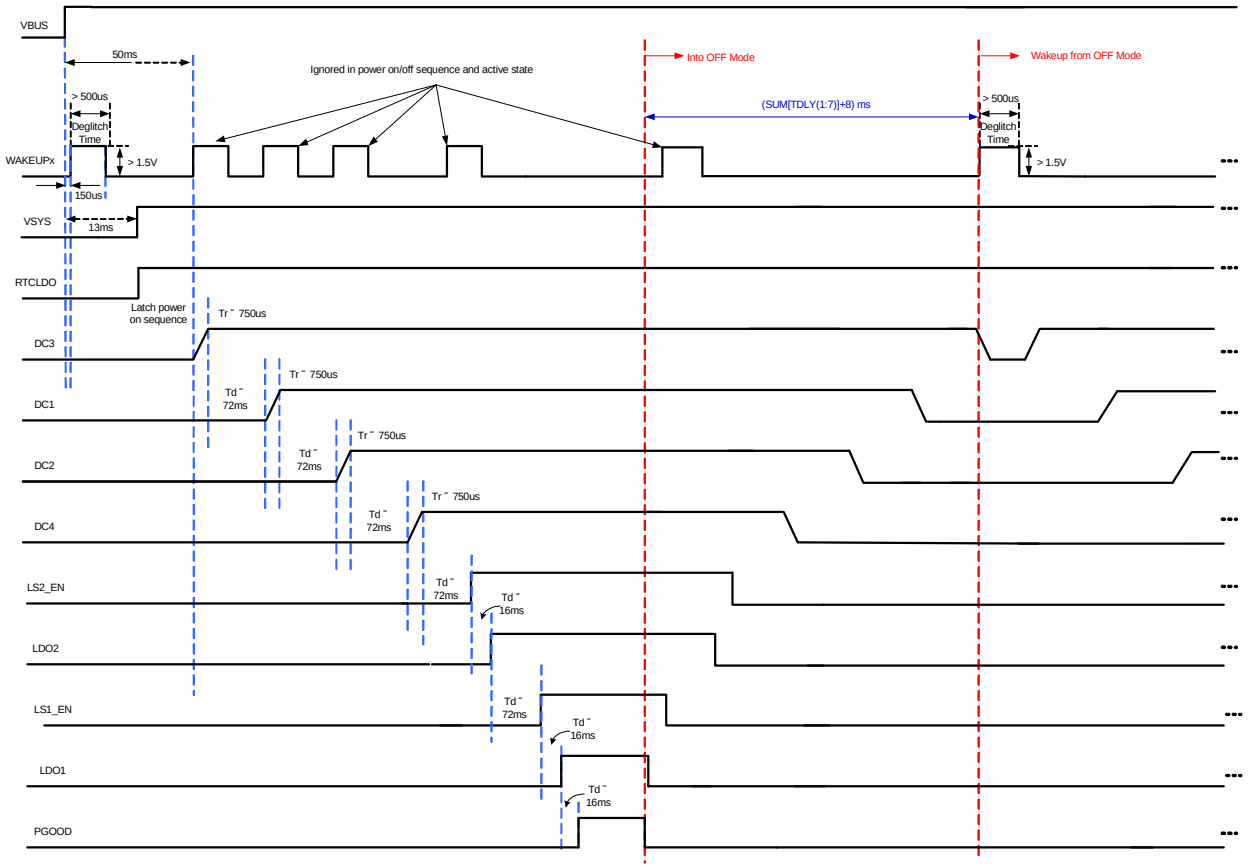






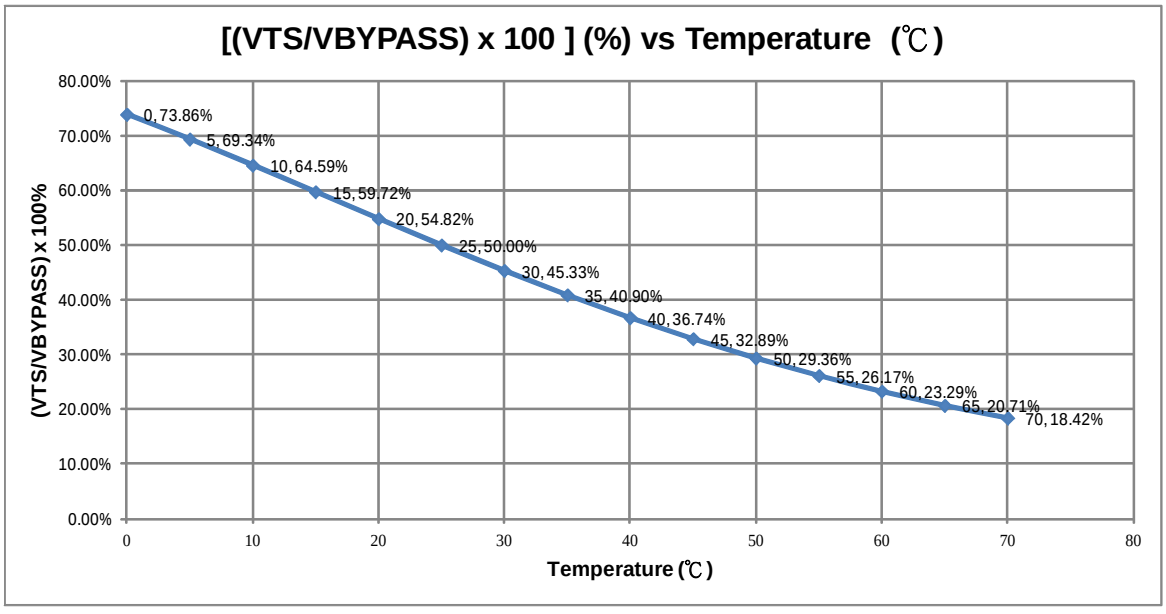
Power Sequence

No Battery, VBUS Power On



NTC Table and Curve

R_NTC : 10kΩ@25°C		
Beta (NTC)= 3380		
Temperature (℃)	R_NTC (Ohm)	Gamma (%, V_TS/V_BYPASS)
0	28255	73.86%
5	22614	69.34%
10	18243	64.59%
15	14826	59.72%
20	12136	54.82%
25	10000	50.00%
30	8293	45.33%
35	6919	40.90%
40	5807	36.74%
45	4900	32.89%
50	4157	29.36%
55	3544	26.17%
60	3036	23.29%
65	2612	20.71%
70	2258	18.42%



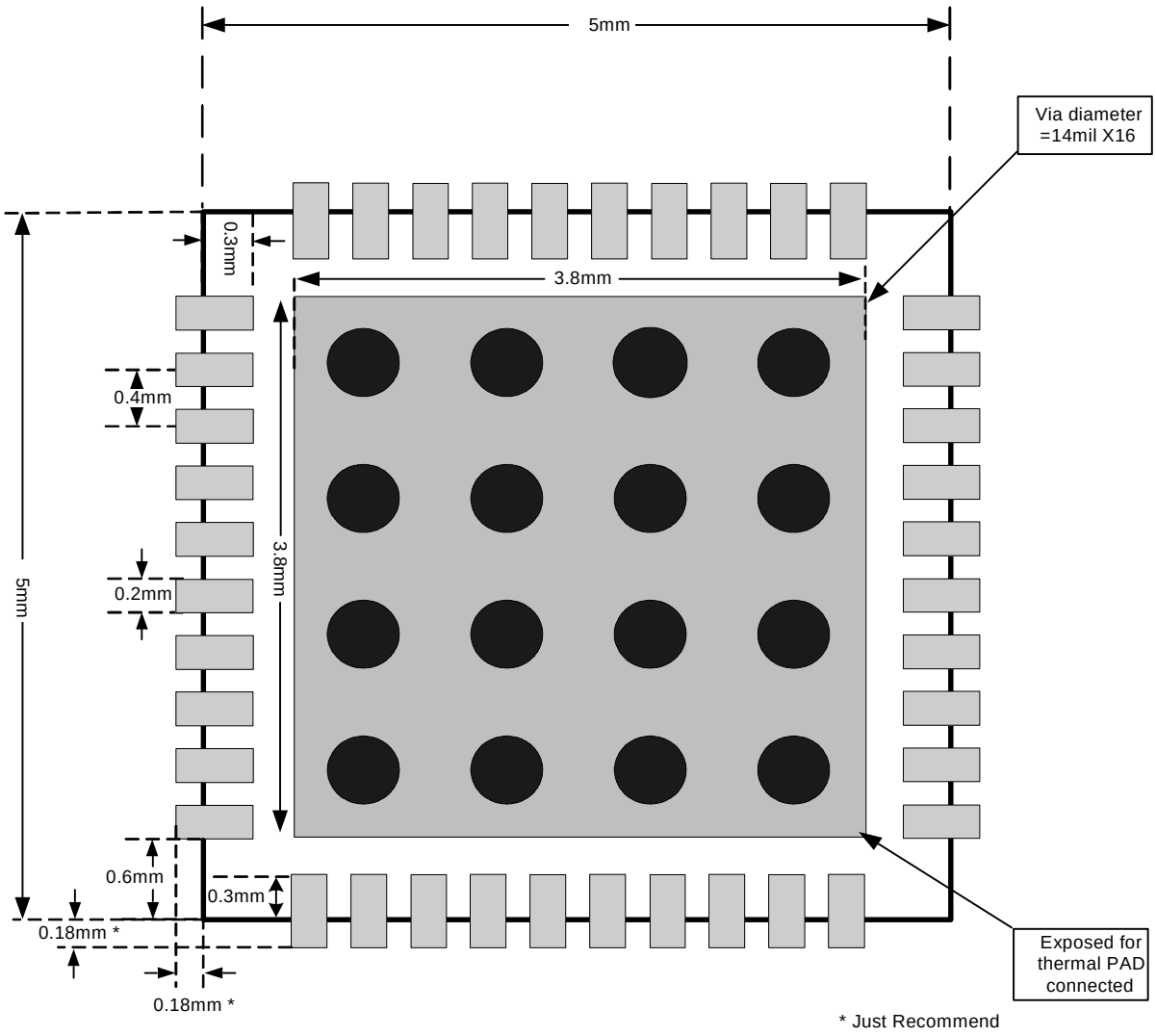
Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. Below are Layout consideration checklist and demoboard layout for your reference:

Signal Name	Pinouts Definition	Layout
Input Pins (VBUS, VSYS, VIN_DC1, VIN_DC2, VIN_DC3, VIN_DC4, VINLDO1, VINLDO2)	Charger and All VR's Power Souce Input Pins	Place the input capacitors on each power source input pins with low impedance to GND and low impedance to the each input pins. Noted that, because VSYS is the all VR's input power source, the VSYS terminal bulk capacitor is recommended to 22uF/16V and connects to VSYS terminal as close as possible
LX Pins (CHGOUT, LX_DC1, LX_DC2 LX_DC3, LX_DC4)	ALL VR's LX Pins	Keep the switching nodes away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes to inductors as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer. Ideally, route the LX pins to inductors on the top layer is recommended to avoid the switching nodes inteference.
RSNS	Charger Current Sence Resistor	The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) and do not route the sense leads through a high-current path
Feedback Pins (FB_DC1, FB_DC2, FB_DC3, FB_DC4, FB_LDO1)	ALL VR's output feedback voltage pin.	The pins are high impedance and sensible to noise from the switch node. Coupling from fast switching signals must be avoided. For the better stability, the forward capcitor 5pF from output to feedback is recommended and the feedback divider resistance is recommended as the application circuit.
Bypass pin	Intenal bias voltage. It could be the source of resistor-divider for NTC circuit sensing.	Connect the decoupling capacitor to bypass pin as close as possible. The small control signals should be routed away from the high current paths.
Ground (Thermal Pad, PGND, AGND)	IC's analog and power ground	Connect the IC's AGND and PGND pad to thermal pad directly. The thermal pad connects to other layer's ground plane through several vias.

Layout Consideration (Cont.)

Recommended Minimum Footprint



I²C Programming

I²C SERIAL CONTROL INTERFACE

The APW7703D DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports standard mode (100-kHz), fast mode (400-kHz) and the high-speed mode (up to 3.4Mbps in wire mode) data transfer rates for single byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum), the fast I²C bus operation (400 kHz maximum) and the high-speed mode (up to 3.4Mbps in wire mode). The DAP performs all I²C operations without I²C wait cycles.

General I²C Operation

The I²C bus uses two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus.

The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 1. The master generates the 7-bit slave address and the R/$\overline{W}$ bit—a zero indicates a transmission (WRITE), a “one” indicates a request for data (READ) to open communication with another device and then waits for an acknowledge condition. The APW7703D holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the high level for the bus.

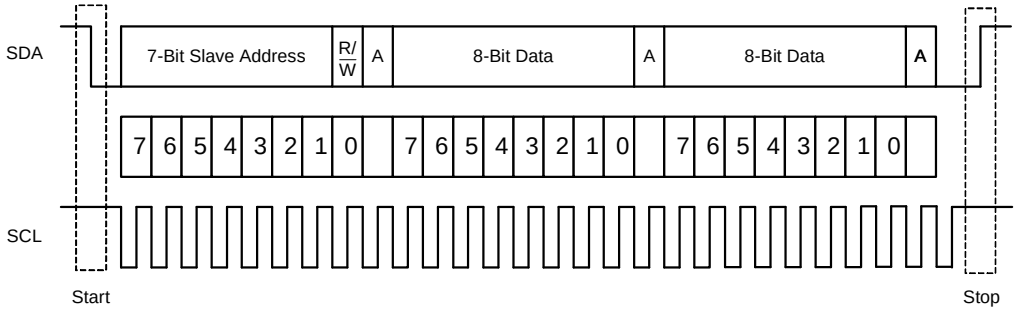


Figure 1. Typical I²C sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 1. The device 7-bit address is defined as “0100100” (24H).

I²C Programming (Cont.)

Single-Byte Transfer

The serial control interface supports single-byte R/$\overline{W}$ operations for sub-addresses 0x00 to 0xFF.
Supplying a sub-address for each sub-address transaction is referred to as random I²C addressing. The APW7703D also supports sequential I²C addressing. For write transactions, if a sub-address is issued followed by data for that sub-address and the 15 sub-addresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 sub-addresses is successfully received by the APW7703D. For I²C sequential write transactions, the sub-address then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many sub-addresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last sub-address, the data for the last sub-address is discarded. However, all other data written is accepted; only the incomplete data is discarded.

Single-Byte Write

As shown in Figure 2, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit determines the direction of the data transfer. For a write data transfer, the R/$\overline{W}$ bit will be a 0. After receiving the correct I²C device address and the R/$\overline{W}$ bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the APW7703D internal memory address being accessed. After receiving the address byte, the APW7703D again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the APW7703D again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

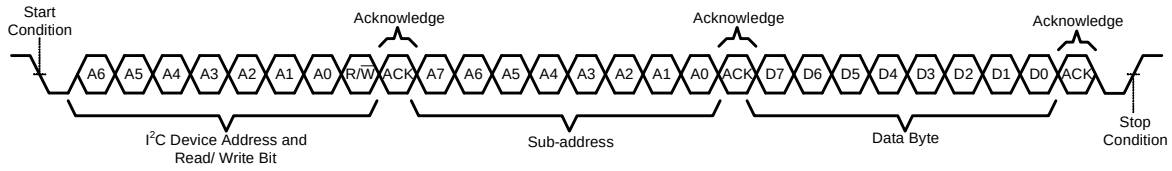


Figure 2. Single-Byte Write Transfer

I²C Programming (Cont.)

Single-Byte Read

As shown in Figure 3, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/$\overline{W}$ bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/$\overline{W}$ bit becomes a 0. After receiving the APW7703D address and the R/$\overline{W}$ bit, APW7703D responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the APW7703D address and the R/$\overline{W}$ bit again. This time the R/$\overline{W}$ bit becomes a 1, indicating a read transfer. After receiving the address and the R/$\overline{W}$ bit, the APW7703D again responds with an acknowledge bit. Next, the APW7703D transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

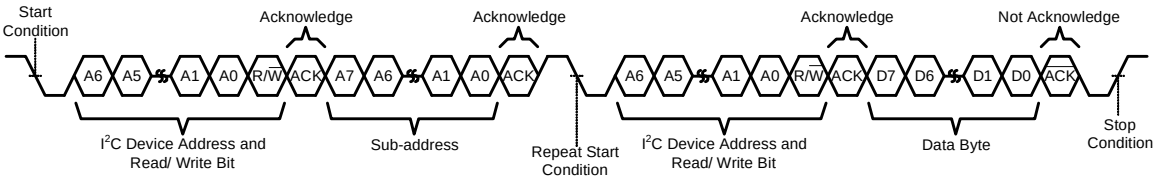


Figure 3. Single-Byte Read Transfer

I²C Programming (Cont.)

I2C Control Timing						
	SDA and SCL Leakage Current		-	0.01	1	μA
F_{I2C}	I2C Operating Frequency		-	-	100 400	KHz
T_{BUF}	I2C free time between stop and start condition	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
$T_{\_HD\_STA}$	Hold time after start condition	After this period, the first clock is generated SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
$T_{\_SU\_STA}$	Repeated start condition setup time	SCL=100KHz SCL=400KHz	4.7 0.6	- -	- -	μs
$T_{\_SU\_STO}$	Stop condition setup time	SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
$T_{\_HD\_DAT}$	Data hold time	SCL=100KHz SCL=400KHz	300 300	- -	- -	ns
$T_{\_SU\_DAT}$	Data setup time	SCL=100KHz SCL=400KHz	250 100	- -	- -	ns
$T_{\_LOW}$	Clock low period	SCL=100KHz SCL=400KHz	4.7 1.3	- -	- -	μs
$T_{\_HIGH}$	Clock high period	SCL=100KHz SCL=400KHz	4 0.6	- -	- -	μs
T_F	Fall time of I2C SDA	SCL=100KHz SCL=400KHz	20+0.1 C_b 20+0.1 C_b	- -	300 300	ns
T_F	Fall time of I2C SCL	SCL=100KHz SCL=400KHz	20+0.1 C_b 20+0.1 C_b	- -	300 300	ns
T_R	Rise time of I2C SDA	SCL=100KHz SCL=400KHz	- -	- -	1000 300	ns
T_R	Rise time of I2C SCL	SCL=100KHz SCL=400KHz	20+0.1 C_b 20+0.1 C_b	- -	300 300	ns
C_b	Capacitive Load for Each B μs Line	SCL=100KHz SCL=400KHz	- -	- -	400 400	pF

I²C Programming (Cont.)

Timing Diagram

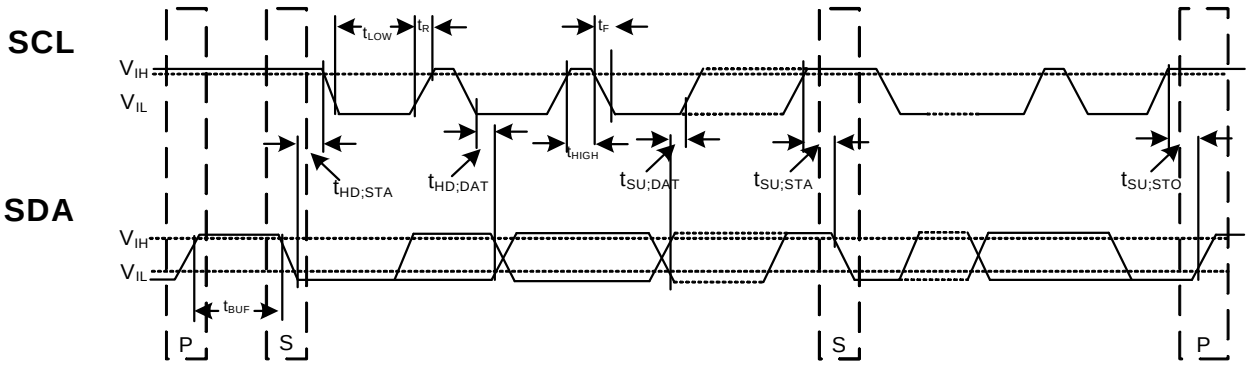


Figure 4: SMBus Common AC Specification

I²C Programming (Cont.)

Register Map

Register Address	Register Name	Read/Write/Read Only State	Bits								Default Value
			D7	D6	D5	D4	D3	D2	D1	D0	
00	CONTROL0	Read/Write	0	0	0	1	1	1	1	0	1E
01	CONTROL1	Read/Write	0	0	1	0	0	0	0	0	20
02	CONTROL2	Read/Write	0	1	0	1	0	0	0	0	50
03	CHGCONFIG0	Read/Write	1	0	1	1	0	1	0	1	B5
04	CHGCONFIG1	Read/Write	1	1	0	1	1	0	0	0	D8
05	CHGCONFIG2	Read/Write	1	1	1	0	0	0	1	1	E3
06	CHGCONFIG3	Read/Write	0	0	0	0	0	1	1	1	07
07	BUCKCONFIG0	Read/Write	0	0	1	1	0	0	1	1	33
08	BUCKCONFIG1	Read/Write	0	0	1	1	0	0	1	1	33
09	LDOCONFIG0	Read/Write	0	0	0	1	1	1	1	1	1F
0A	LDOCONFIG1	Read/Write	0	0	0	0	1	0	0	0	08
0B	TIME LAPSE2	Read/Write	1	0	1	0	1	0	1	0	AA
0C	TIME LAPSE1	Read/Write	1	0	1	0	1	0	1	0	AA
0D	TIME LAPSE0	Read/Write	1	0	1	0	1	0	1	0	AA
0E	SEQ0	Read/Write	0	0	0	1	0	0	1	0	12
0F	SEQ1	Read/Write	0	0	0	0	0	0	1	1	03
10	SEQ2	Read/Write	0	1	1	0	0	1	0	0	64
11	SEQ3	Read/Write	0	1	1	1	0	1	0	1	75
12	DLY0	Read/Write	1	1	1	1	1	1	1	1	FF
13	DLY1	Read/Write	1	1	1	1	1	1	1	1	FF
14	DLY2	Read/Write	0	0	0	1	1	1	1	1	1F
15	DLY3	Read/Write	0	0	0	1	0	0	0	1	11
16	INT MASK	Read/Write	1	0	0	0	0	0	0	0	80
17	CHIPID	ReadOnly	0	0	1	1	0	x	x	x	3x
19	INT FLAG	Read Only	0	0	0	0	0	0	0	0	00
1A	WAKEUP	Read Only	0	0	0	0	0	0	0	0	00

I²C Programming (Cont.)

REG00

Bit	7	6	5	4	3	2	1	0
Name	WDT_RST	RESERVED	OFF	RSTTMR_EN	USB_EN	IUSB		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	1	1	1	0

Name	Description
WDT_RST	Watchdog timer reset bit. Write "1" to reset the watchdog timer when WDT_EN bit is enabled. **0 – Read 0 as usual, write 1 no effect** 1 – Write 1 to reset the watchdog timer. (auto clear)
RESERVED	No Used
OFF	**0 – Normal staus** 1 –Trigger a power-down sequence. Note: When set this bit to 1 to trigger a power-down sequence. Bit is automatically reset to 0. During power down sequence, if the STBYON bit set to "1", the channel will still on.
RSTTMR_EN	Push-button(Wakeup0) reset function enable-disable bit 0 – Disabled **1 – Enabled**
USB_EN	USB power path enable 0 – USB power input is turned off (USB suspend mode) **1 – USB power input is turned on**
IUSB	USB input current limit 000 – 100mA 001 – 500mA 010 – 900mA 011 – 1300mA 100 – 1700mA 101 – 2100mA **110 – 2500mA** 111 – No Used

I²C Programming (Cont.)

REG01

Bit	7	6	5	4	3	2	1	0
Name	LBAT_ALM	VLBAT			TL_EN	RSTTMR	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	0	0	0	0	0

Name	Description
LBAT_ALM	Low battery alarm enable bit (When alarm is enabled, low battery will automatic power on in sequence when PMIC in OFF mode) **0 – Low battery alarm(3.5V) function disable** 1 – Low battery alarm(3.5V) function enable
VLBAT	Low battery alarm voltage threshold setting 000 –3.0V 001 –3.1V **010 –3.2V** 011 –3.3V 100 –3.4V 101 –3.5V 110 –3.6V 111 –3.7V
TL_EN	Time lapse function enabled bit **0 – time lapse function disable** 1 – time lapse function enable
RSTTMR	Push-button(Wakeup0) reset time constant **0 – 8s** 1 – 16s NOTE: Device enters RESET if wakeup0 is held high pulse width for >8s or >16s(default), depending on RSTTMR bit.
RESERVED	No Used

I²C Programming (Cont.)

REG02

Bit	7	6	5	4	3	2	1	0
Name	WDT_EN	WDTMR			RESERVED	RESERVED	RESERVED	RESERVED
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	0	1	0	0	0	0

Name	Description
WDT_EN	Watchdog timer function enabled bit **0 – watchdog timer function disable** 1 – watchdog timer function enable Note: When WDT_EN is enabled, write "1" to reset WDT_RST bit to reset watchdog timer, if watchdog timer is timeout, the PMIC will reset all registers and auto reboot.
WDTMR	Watchdog timer setting bit. 000 – 1s 001 – 2s 010 – 4s 011 – 8s 110 –16s **101 –32s** 110 – 64s 111 – 128s
RESERVED	No Used

I²C Programming (Cont.)

REG03

Bit	7	6	5	4	3	2	1	0
Name	TIMER		TMR_EN	CHG_MODE	RESERVED	TERM	RESERVED	CHG_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	1	0	1	0	1

Name	Description
TIMER	Charge safety timer setting (fast charge timer) 00 – 4h 01 – 6h **10 – 8h** 11 – 10h
TMR_EN	Safety timer enable 0 –Fast charge timer is disabled **1 –Fast charge timer is enabled**
CHG_MODE	Charger mode select 0 – Linear charger mode **1 – Switching charger mode**
RESERVED	No Used
TERM	Charge termination on/off 0 – current-based charge termination will not occur and the charger will always be on **1 – charge termination enabled, based on timers and termination current**
CHG_EN	Charger enable 0 – charger is disabled **1 – charger is enabled**

I²C Programming (Cont.)

REG04

Bit	7	6	5	4	3	2	1	0
Name	DYNTMR	VOREG				RDIS	DIS_EN	DISOFF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	0	1	1	0	0	0

Name	Description
DYNTMR	Dynamic timer function 0 – safety time is the normal setting value **1 – safety timer is 2 times of normal setting value if thermal loop or DPM loop is active (Default)**
VOREG	Charge voltage selection 0000 – 3.504V 0100 – 3.760V 1000 – 4.016V 1100 – 4.272V 0001 – 3.568V 0101 – 3.824V 1001 – 4.080V 1101 – 4.336V 0010 – 3.632V 0110 – 3.888V 1010 – 4.144V 1110 – 4.400V 0011 – 3.692V 0111 – 3.952V **1011 – 4.208V** 1111 – 4.464V
RDIS	Battery discharge Resistor **0 – 80Ω** 1 – 200 Ω
DIS_EN	Discharge enable **0 – battery is not discharged when temperature is above discharge threshold** 1 – battery is discharged temperature is above discharge threshold and Vbat > 3.9V
DISOFF	DISCHARGE-OFF threshold (battery is discharged until the battery voltage drops to): **0 – 3.7V** 1 – 3.8V

I²C Programming (Cont.)

REG05

Bit	7	6	5	4	3	2	1	0
Name	ICHG			PCHRGT	VPRECHG	RESERVED	IPRECHG	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	1	0	0	0	1	1

Name	Description
ICHG	Charge current setting Switching Mode, Rsns= 100mΩ; 000 – 128mA 001 – 256mA 010 – 384mA 011 – 512mA 100 – 640mA 101 – 768mA 110 – 896mA **111 – 1024mA** Switching Mode, Rsns= 68mΩ; 000 – 188mA 001 - 376mA 010 – 564mA 011 – 752mA 100 – 941mA 101 – 1129mA 110 –1317mA **111 – 1505mA** Linear Mode 000 - 100mA 001 - 255mA 010 - 440mA 011 - 640mA 100/101/110/111 - No Used
PCHRGT	Pre-charge time **0 – 30 min** 1 – 60 min
VPRECHG	Precharge voltage **0 – pre-charge to fast charge transition voltage is 2.8V** 1 – pre-charge to fast charge transition voltage is 3.0V
RESERVED	No Used
IPRECHG	Precharge current setting Switching Mode, Rsns= 100mΩ; 00 – 64mA 01 – 128mA 10 – 192mA **11 – 256mA** Switching Mode, Rsns= 68mΩ; 00 – 94mA 01 – 188mA 10 – 282mA **11 – 376mA** Linear Mode 00 - 50mA 01- 100mA 10- 180mA **11- 255mA**

I²C Programming (Cont.)

REG06

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	DPMTH		ITERM		TRANGE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	1	1	1

Name	Description
RESERVED	No Used
DPMTH	Power path DPM threshold **00 – 4.4V** 01 – 4.5V 10 – 4.6V 11 – 4.7V
ITERM	Termination current setting Linear Mode, Rsns= none or Switching Mode, Rsns= 100mΩ; 00 – 64mA 01 – 128mA 10 – 192mA **11 – 256mA** Switching Mode, Rsns= 68mΩ; 00 – 94mA 01 – 188mA 10 – 282mA **11 – 376mA**
TRANGE	Temperature range for battery charging (NTC) 0 – 0-45°C **1 – 0-60°C**

I²C Programming (Cont.)

REG07

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC1	VFB_DC1			STBYON_DC2	VFB_DC2		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1

Name	Description
STBYON_DC1	Off mode DC1 regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
VFB_DC1	VFB_DC1 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V
STBYON_DC2	Off mode DC2 regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
VFB_DC2	VFB_DC2 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V

I²C Programming (Cont.)

REG08

Bit	7	6	5	4	3	2	1	0
Name	STBYON_DC3	VFB_DC3			STBYON_DC4	VFB_DC4		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	1	1	0	0	1	1

Name	Description
STBYON_DC3	Off mode DC3 regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
VFB_DC3	VFB_DC3 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V
STBYON_DC4	Off mode DC4 regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
VFB_DC4	VFB_DC4 voltage setting 000 – 0.555V 001 – 0.570V 010 – 0.585V **011 – 0.600V** 100 – 0.615V 101 – 0.630V 110 – 0.645V 111 – 0.660V

I²C Programming (Cont.)

REG09

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	RTCLDO				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	1	1	1	1

Name	Description
RESERVED	No Used
RTCLDO	RTCLDO output voltage setting 00000 – 1.5V 00001 – 1.55V 00010 – 1.6V 00011 – 1.65V 00100 – 1.7V 00101 – 1.75V 00110 – 1.8V 00111 – 1.85V 01000 – 1.9V 01001 – 1.95V 01010 – 2.0V 01011 – 2.05V 01100 – 2.1V 01101 – 2.15V 01110 – 2.2V 01111 – 2.25V 10000 – 2.3V 10001 – 2.35V 10010 – 2.4V 10011 – 2.45V 10100 – 2.5V 10101 – 2.55V 10110 – 2.6V 10111 – 2.65V 11000 – 2.7V 11001 – 2.75V 11010 – 2.8V 11011 – 2.85V 11100 – 2.9V 11101 – 2.95V 11110 – 3.0V **11111 – 3.05V**

I²C Programming (Cont.)

REG0A

Bit	7	6	5	4	3	2	1	0
Name	STBYON_LDO1	STBYON_LDO2	RESERVED	LDO2				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	1	0	0	0

Name	Description
STBY_ON_LDO1	Standby mode regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
STBY_ON_LDO2	Standby mode regulator enabled bit **0 – power off as sequence** 1 – still enable in OFF mode
RESERVED	No Used
LDO2	LDO2 output voltage setting 0 0000 – 1.50V 0 0001 – 1.55V 0 0010 – 1.60V 0 0011 – 1.65V 0 0100 – 1.70V 0 0101 – 1.75V 0 0110 – 1.80V 0 0111 – 1.85V **0 1000 – 1.90V** 0 1001 – 1.95V 0 1010 – 2.00V 0 1011 – 2.05V 0 1100 – 2.10V 0 1101 – 2.15V 0 1110 – 2.20V 0 1111 – 2.25V 1 0000 – 2.30V 1 0001 – 2.35V 1 0010 – 2.40V 1 0011 – 2.45V 1 0100 – 2.50V 1 0101 – 2.55V 1 0110 – 2.60V 1 0111 – 2.65V 1 1000 – 2.70V 1 1001 – 2.75V 1 1010 – 2.80V 1 1011 – 2.85V 1 1100 – 2.90V 1 1101 – 2.95V 1 1110 – 3.00V 1 1111 – 3.05V

I²C Programming (Cont.)

REG0B

Bit	7	6	5	4	3	2	1	0
Name	T23	T22	T21	T20	T19	T18	T17	T16
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	0	1	0	1	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec **10101010 10101010 10101010 - 11184811 sec (129D 10H 53M 31S)** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

REG0C

Bit	7	6	5	4	3	2	1	0
Name	T15	T14	T13	T12	T11	T10	T09	T08
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	0	1	0	1	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec **10101010 10101010 10101010- 11184811 sec (129D 10H 53M 31S)** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

REG0D

Bit	7	6	5	4	3	2	1	0
Name	T07	T06	T05	T04	T03	T02	T01	T00
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	1	0	1	0	1	0
Name	Description							
T23~T0	Time lapse length setting in second 00000000 00000000 00000000 - 1sec **10101010 10101010 10101010- 11184811 sec (129D 10H 53M 31S)** …… 11111111 11111111 11111111 - 16777216sec (194D 4H 20M 16S)							

I²C Programming (Cont.)

REG0E

Bit	7	6	5	4	3	2	1	0
Name	DC1_SEQ				DC2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	1	0

Name	Description
DC1_SEQ	DC1 enable STROBE 0000 – enable at STROBE0 **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC2_SEQ	DC2 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG0F

Bit	7	6	5	4	3	2	1	0
Name	DC3_SEQ				DC4_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	1	1

Name	Description
DC3_SEQ	DC3 enable STROBE **0000 – enable at STROBE0** 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC4_SEQ	DC4 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG10

Bit	7	6	5	4	3	2	1	0
Name	LS1_EN_SEQ				LS2_EN_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	1	0	0	1	0	0

Name	Description
LS1_EN_SEQ	LS1_EN enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 **0110 – enable at STROBE6** 0111 – enable at STROBE7
LS2_EN_SEQ	LS2_EN enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 **0100 – enable at STROBE4** 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG11

Bit	7	6	5	4	3	2	1	0
Name	LDO1_SEQ				LDO2_SEQ			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	1	1	1	0	1	0	1

Name	Description
LDO1_SEQ	LDO1 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 **0111 – enable at STROBE7**
LDO2_SEQ	LDO2 enable STROBE 0000 – enable at STROBE0 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 **0101 – enable at STROBE5** 0110 – enable at STROBE6 0111 – enable at STROBE7

I²C Programming (Cont.)

REG12

Bit	7	6	5	4	3	2	1	0
Name	DLY1				DLY2			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	1	1	1	1	1	1
Name	Description							
DLY1	Delay 1 time (Between STROBE0 and STROBLE1) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms 0001 – 16ms 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms **1111 – 72ms**							
DLY2	Delay 2 time (Between STROBE1 and STROBLE2) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms 0001 – 16ms 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms **1111 – 72ms**							

REG13

Bit	7	6	5	4	3	2	1	0
Name	DLY3				DLY4			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	1	1	1	1	1	1	1
Name	Description							
DLY3	Delay 3 time (Between STROBE2 and STROBLE3) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms 0001 – 16ms 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms **1111 – 72ms**							
DLY4	Delay 4 time (Between STROBE3 and STROBLE4) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms 0001 – 16ms 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms **1111 – 72ms**							

I²C Programming (Cont.)

REG14

Bit	7	6	5	4	3	2	1	0
Name	DLY5				DLY6			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	1	1	1	1

Name	Description
DLY5	Delay 5 time (Between STROBE4 and STROBLE5) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms **0001 – 16ms** 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms 1111 – 72ms
DLY6	Delay 6 time (Between STROBE5 and STROBLE6) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms 0001 – 16ms 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms **1111 – 72ms**

REG15

Bit	7	6	5	4	3	2	1	0
Name	DLY7				PGDLY			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	1	0	0	0	1

Name	Description
DLY7	Delay 7 time (Between STROBE6 and STROBLE7) 0000 – 12ms 0100 – 28ms 1000 – 44ms 1100 – 60ms **0001 – 16ms** 0101 – 32ms 1001 – 48ms 1101 – 64ms 0010 – 20ms 0110 – 36ms 1010 – 52ms 1110 – 68ms 0011 – 24ms 0111 – 40ms 1011 – 56ms 1111 – 72ms
PGDLY	Power Good Delay time 0000 – 10ms 0100 – 40ms 1000 – 72ms 1100 – 104ms **0001 – 16ms** 0101 – 48ms 1001 – 80ms 1101 – 112ms 0010 – 24ms 0110 – 56ms 1010 – 88ms 1110 – 120ms 0011 – 32ms 0111 – 64ms 1011 – 96ms 1111 – 128ms Note PGDLY applies to PGOOD pin.

I²C Programming (Cont.)

REG16

Bit	7	6	5	4	3	2	1	0
Name	ISINKM	RESERVED	WKUPxM	LBATM	TEMPM	RESERVED	OVPM	USBM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1	0	0	0	0	0	0	0

Name	Description
ISINKM	Battery discharge current sink status change interrupt mask 0 – interrupt is issued when current sink status changes **1 – no interrupt is issued when current sink is either enabled or disabled**
RESERVED	No Used
WKUPxM	Wakeup status change interrupt mask **0 – interrupt is issued when wakeupx status changes (WAKEUPx changed low to high)** 1 – no interrupt is issued when wakeupx status changes
LBATM	Low battery detected status change interrupt mask **0 – interrupt is issued when low battery voltage is detected** 1 – no interrupt is issued when low battery voltage is detected
TEMPM	Chip temperature alarm status change interrupt mask **0 – interrupt is issued when chip temperature is over 130℃** 1 – no interrupt is issued when chip temperature is over 130℃
OVPM	USB power overvoltage status change interrupt mask **0 – interrupt is issued when USB input is overvoltage** 1 – no interrupt is issued when USB input is overvoltage
USBM	USB power status change interrupt mask **0 – interrupt is issued when power to USB input is applied or removed** 1 – no interrupt is issued when power to USB input is applied or removed

I²C Programming (Cont.)

REG17

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	CHIPID			RESERVED	REV		
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	1	1	0	x	x	x

Name	Description
RESERVED	No Used
CHIP ID	Chip ID **011 – APW7703D**
REV	Revision 000 – revision 1.0 001 – revision 1.1 010 – revision 1.2 011 – revision 1.3 … 111 - Future Use

I²C Programming (Cont.)

REG19

Bit	7	6	5	4	3	2	1	0
Name	ISINKI	RESERVED	RESERVED	WKUPxI	LBATI	TEMPI	OVPI	USBI
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Name	Description
ISINKI	Battery discharge status changed flag **0 – no discharge on battery** 1 – Battery current sink discharge has been enabled.
RESERVED	No Used
WKUPxI	Wakeupx status changed flag **0 – no change in status** 1 – wakeupx status change (WAKEUPx changed low to high) NOTE: Detail information is available in 0x1A register
LBATI	Low battery detected status changed flag **0 – no change in status** 1 – Low battery voltage is detected
TEMPI	Chip temperature alarm status changed flag **0 – no change in status** 1 – Chip temperature is over 130 ℃
OVPI	USB power overvoltage status changed flag **0 – no change in status** 1 – USB input is overvoltage
USBI	USB power status changed flag **0 – no change in status** 1 – USB power status change (power to USB pin has either been applied or removed) NOTE: Status information is available in STATUS register

I²C Programming (Cont.)

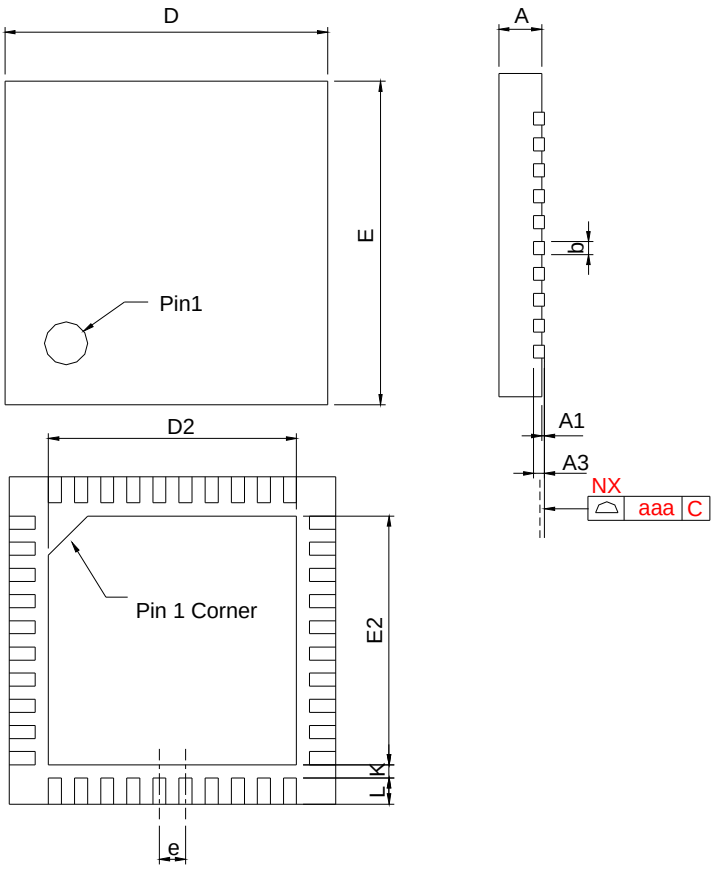
REG1A

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	WKUP0	WKUP1	WKUP2	RESERVED	RESERVED
Read/Write	R	R	R	R	R	R	R	R
Default Value	0	0	0	0	0	0	0	0

Name	Description
RESERVED	No Used
WKUP0	WAKEUP0 status changed bit. (Auto clear when readout) **0 – no change in WAKEUP0 status** 1 – WAKEUP0 status change
WKUP1	WAKEUP1 status changed bit. (Auto clear when readout) **0 – no change in WAKEUP1status** 1 – WAKEUP1 status change
WKUP2	WAKEUP2 status changed bit. (Auto clear when readout) **0 – no change in WAKEUP2 status** 1 – WAKEUP2 status change

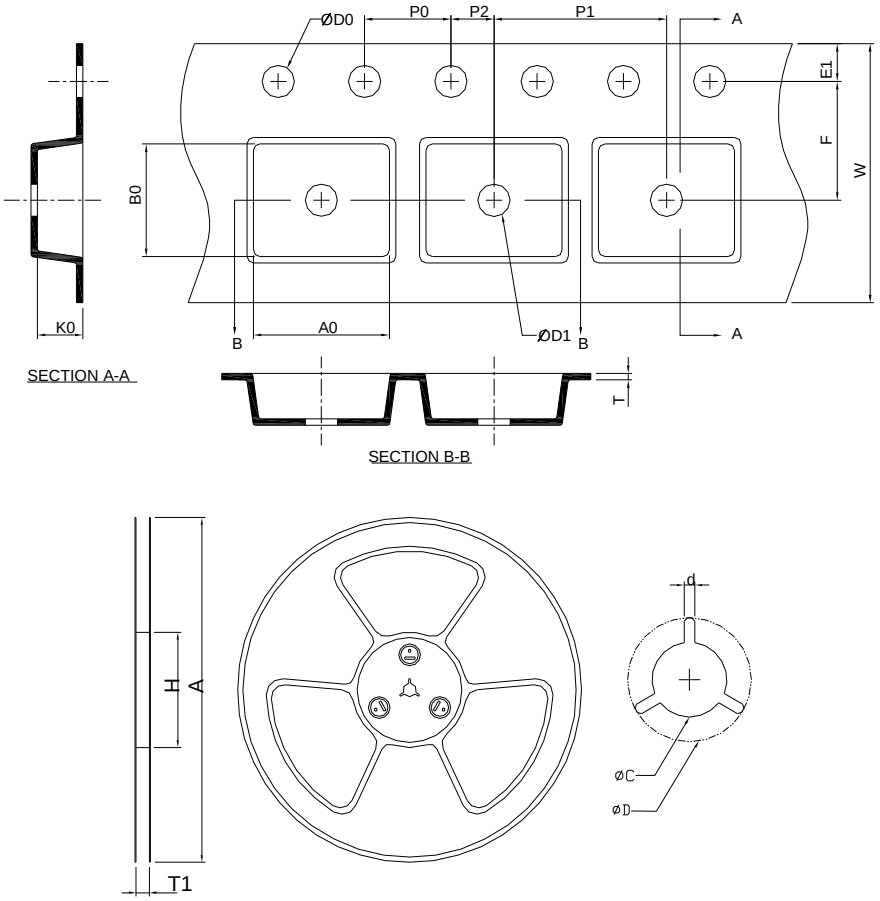
Package Information

TQFN5x5-40A



SYMBOL	TQFN5*5-40A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.70	3.90	0.146	0.154
E	4.90	5.10	0.193	0.201
E2	3.70	3.90	0.146	0.154
e	0.40 BSC		0.016 BSC	
L	0.30	0.40	0.012	0.016
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

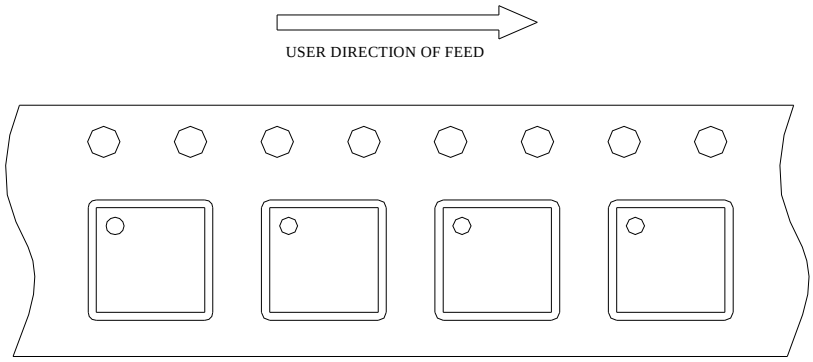
(mm)

Devices Per Unit

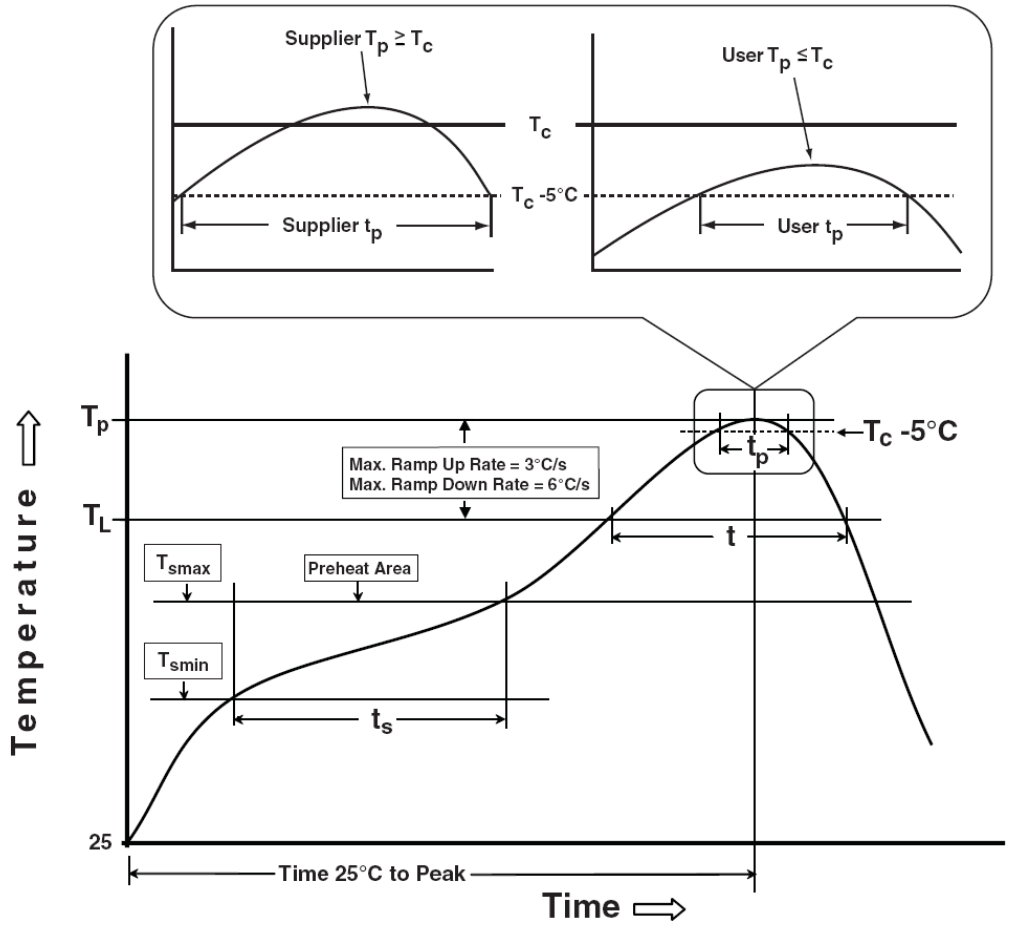
Package Type	Unit	Quantity
TQFN5x5-40A	Tape & Reel	2500

Taping Direction Information

TQFN5x5-40A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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