Wide Input 5.4V to 21V Power Management IC(PMIC) for High Performance Computing Applications

1. General Description

The APW8856 is a Power Management IC (PMIC) designed to provide complete Power Management solution for the Rest of the Platform Power (ROP) supplies for Intel Canon Lake(*) applications. The IC operates from a single supply voltage of 5.4V to 21V allowing it to be used in 2 Cell to 4 Cell battery applications. The APW8856 is designed to provide maximum number of regulators in the smallest available cost effective package. Included in the IC are; Four Switching Buck controllers for 5V and 3.3V system voltages as well as VDDQ and 1.05V, Six LDOs for variety of applications such as memory VTT and Vpp, One internal high frequency 3A Buck regulator typically used for 1.8V supply and One Dual Input Single output switch. The PWM controllers use the ANPEC cost effective external Power Blocks APW870x family for minimum pin interface with the PMIC, while providing output currents of up to 25A capability.

The IC is equipped with all the standard protection features such as over current, over voltage and internal under voltage lock out protection as well as thermal SD.

The serial interface is an I2C communication interface which allows supply sequencing as well as controlled margining of ramp up and ramp down of all supplies to optimize battery power consumption. The I2C interface also allows for adjustability of Soft Start, Forced PWM/Auto PFM/PWM, power sequencing as well output discharge and IRQ.

The IC is offered in a small TQFN, 5x5-40L package for best thermal performance while optimizing the cost.

(*)Intel Trade mark

2. Applications

- **High Performance Notebook and Ultra Notebook**
- **2 Cell Tablet Applications**
- **High Performance Digital Signage**

3. Key Features

■ Voltage Rail

- **Provide 4 Buck Single Phase PWM Controllers**
  - V5(V5VA_DS3) 5V, 6A continuous
  - V6(V3V3_DSW) 3.3V, 6A continuous
  - V10(VDDQ)1.1V/1.15V/1.2V/1.35V,7.4A continuous
  - V11(V105A) 1.05V, 10.5A continuous
- **Provide 1 Buck Single Phase PWM Converter**
  - V8(V1V8A) 1.8V, 2.5A continuous
- **Provide 6 LDO Outputs**
  - V9(V18U_25U) 2.5V, 0.7A continuous
  - V13(VTT) in tracking of 0.5*VDDQ voltage, 0.6A continuous
  - V14(VCC_RTC) 3V, 400μA
  - V17(VLDO_OUT) 2.8V/1.05V, 0.3A/90mA
  - V5VA_LDO 5V, 100mA
  - V3V3_LDO 3.3V, 100mA
- **Provide 4 Load Switches**
  - V9(V1.8U_2.5U) 1.8V, 0.7A continuous
  - V15(VDISO) 3.3V/1.8V switchover, 0.4A continuous
  - V16(VCCSTU) 1.05V, 190mA continuous

■ Power Management Controller

- **Support G3, S5/S4, S3, S0, DS5, DS4, DS3, non-DS3 and Connected Standby state**
- **POK Signal for VR power state: VDDQ_POK, RSM_RST#_POK and V3V3_DSW_POK**
- **Support Several Memory Types: DDR3L, DDR4, LPDDR3, LPDDR4, DDR4RS, DDR4E, 3DXPoint**

■ Communication Interface

- **I2C Interface for SoC Access**
- **Support Bit Rate 0.4MBit/s and 1MBit/s**

■ Built in Current limit, Over Voltage protection and Over temperature protection

■ TQFN5x5-40 Package.

4. Ordering and Marking Information

APW8856 □□□□□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- Product Code

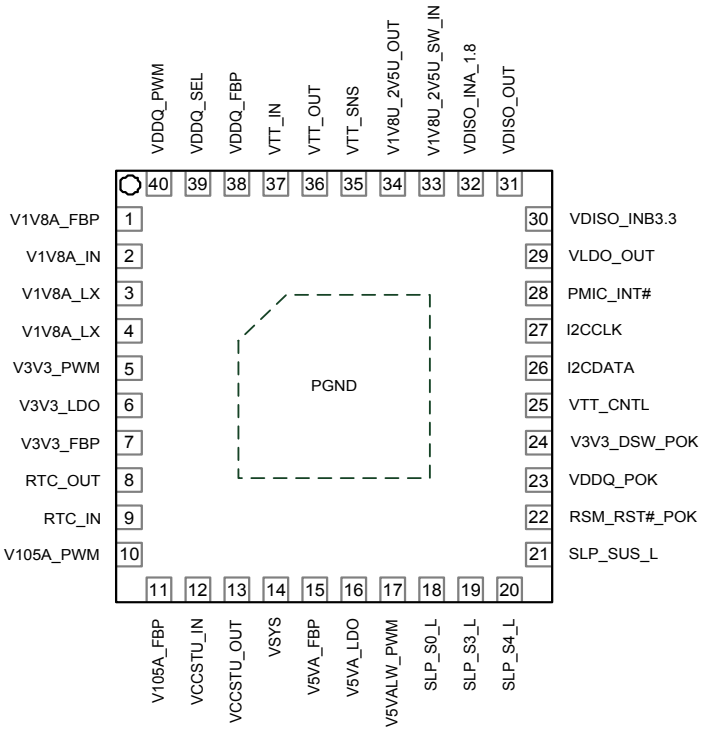
Product Code
Omited or -01, -02, -03, -04, -05, -06, -07,-08 or A, see below table for details
Package Code
QB : TQFN 5x5-40
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW8856QBI :	APW8856 XXXXX	X - Date Code	APW8856-01QBI :	01 APW8856 XXXXX	X - Date Code
APW8856-02QBI :	02 APW8856 XXXXX	X - Date Code	APW8856-03QBI :	03 APW8856 XXXXX	X - Date Code
APW8856-04QBI :	04 APW8856 XXXXX	X - Date Code	APW8856-05QBI :	05 APW8856 XXXXX	X - Date Code
APW8856-06QBI :	06 APW8856 XXXXX	X - Date Code	APW8856-07QBI :	07 APW8856 XXXXX	X - Date Code
APW8856AQBI :	A APW8856 XXXXX	X - Date Code	APW8856-08QBI :	08 APW8856 XXXXX	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Part Number	Description
APW8856QBI	1. Support DS4/5 but not support DS3 2. VCCSTU’s enable input is controlled by SLP_S4_L. 3. VLDO_OUT enable input is controlled by ANDed of (SLP_S3_L, SLP_S0_L) 4. VLDO_OUT output is 2.8V 5. VSYS<5.3V to shutdown, support 2S battery 6. Softstart time of V3V3_DSW, V5VA_DS3, V1V8A , V105A and VDDQ power rails are 1.25ms 7. VTT off behavior is non-tracking discharge
APW8856-01QBI	Identical with APW8856QBI except for that power sequence is referred to “Not support DS3/DS4/DS5”
APW8856-02QBI	Identical with APW8856QBI except for that power sequence is referred to “Support DS3/DS4/DS5”
APW8856-03QBI	Identical with APW8856QBI except for that VCCSTU’s enable input is controlled by (SLP_S3_L) or (SLP_S3_L and SLP_S0_L)
APW8856-04QBI	Identical with APW8856QBI except for that VLDO_OUT enable input is controlled by SLP_S4_L
APW8856-05QBI	Identical with APW8856QBI except for that softstart time of V3V3_DSW and V5VA_DS3 is 20ms, V1V8A and V105A is 10ms and VDDQ is 1.25ms
APW8856-06QBI	Identical with APW8856QBI except for that VTT off behavior is tracking-discharge of half VDDQ
APW8856-07QBI	Identical with APW8856QBI except for that VLDO_OUT output is 1.05V
APW8856-08QBI	Identical with APW8856QBI except for: 1. APW8856-08 power sequence (refer to timing chart) 2. VLDO_OUT (V17) output is 1.05V 3. The delay time between V5VA_DS3 POK and V105A softstart beginning is 0ms 4. VDISO_OUT is disable
APW8856AQBI	Identical with APW8856QBI except for [VSYS<5.2V IC shutdown] function is disabled in order to support 1S battery (VSYS>3.6V IC enabled) and V5VA_DS3 PWM controller is disabled..

5. Pin Configuration



6. Absolute Maximum Ratings (Note 1)

Pin or Symbol	Parameter	Rating	Unit
VSYS	VSYS to DGND	-0.3~28	V
V1V8A_LX, V1V8A_IN,	V1V8A_LX to PGND V1V8A_IN to PGND	-0.3 to 6.5	V
V5VA_FBP, V3V3_FBP,VTT_SNS	V5VA_FBP, V3V3_FBP,VTT_SNS to GND	-0.3 to 6.5	V
V5VA_PWM, V3V3_PWM, VDDQ_ PWM, V105A_PWM	V5VA_PWM, V3V3_PWM, VDDQ_PWM, V105A_PWM to PGND	-0.3 to 6.5	V
All Other Pins	All Other Pins to GND	-0.3 to 6.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under“recommended operating conditions”is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)		°C/W

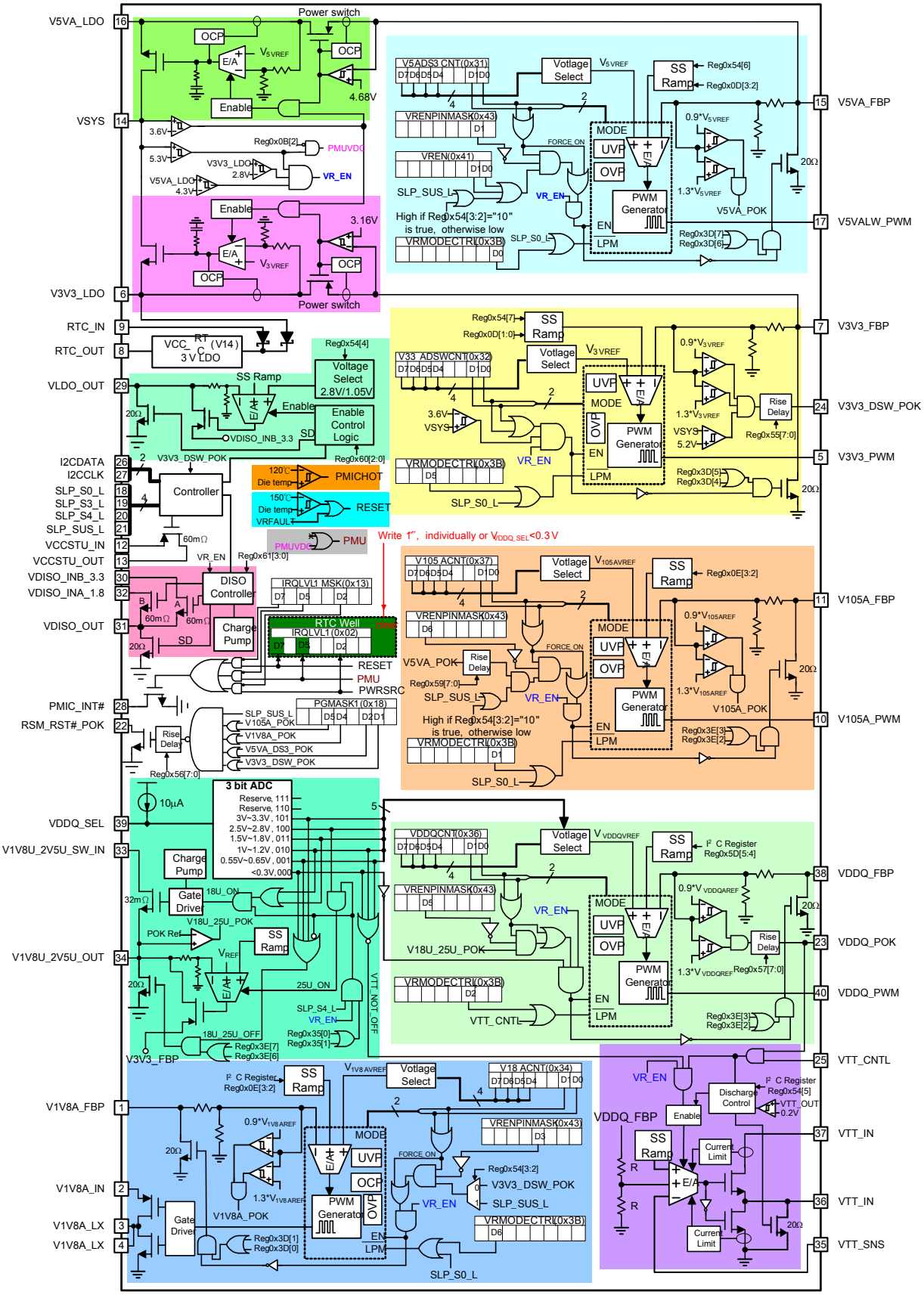
Note 2: θ_{JA} is measured with the component mounted on a JESD-51-7 high effective thermal conductivity test board in free air.

8. Recommended Operation Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VSYS}	System Rail From Battery Management Unit	5.4 ~ 21	V
V_{V1V8A_IN}	V1V8A Regulator Input Voltage	3 ~ 5.5	V
$V_{SLP\_S0\_L}$	SLP_S0_L Input Low Voltage	0 ~ 0.4	V
$V_{SLP\_S0\_L}$	SLP_S0_L Input High Voltage	1.2~ 3.3	V
$V_{SLP\_S3\_L}$	SLP_S3_L Input Low Voltage	0 ~ 0.4	V
$V_{SLP\_S3\_L}$	SLP_S3_L Input High Voltage	1.2~ 3.3	V
$V_{SLP\_S4\_L}$	SLP_S4_L Input Low Voltage	0 ~ 0.4	V
$V_{SLP\_S4\_L}$	SLP_S4_L Input High Voltage	1.2~ 3.3	V
V_{VTT_CNTL}	VTT_CNTL Input Low Voltage	0 ~ 0.4	V
V_{VTT_CNTL}	VTT_CNTL Input High Voltage	1.0~ 3.3	V
$V_{RSM\_RST\#\_POK}$	RSM_RST#_POK Pull High Voltage	3.3 ~ 5.5	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

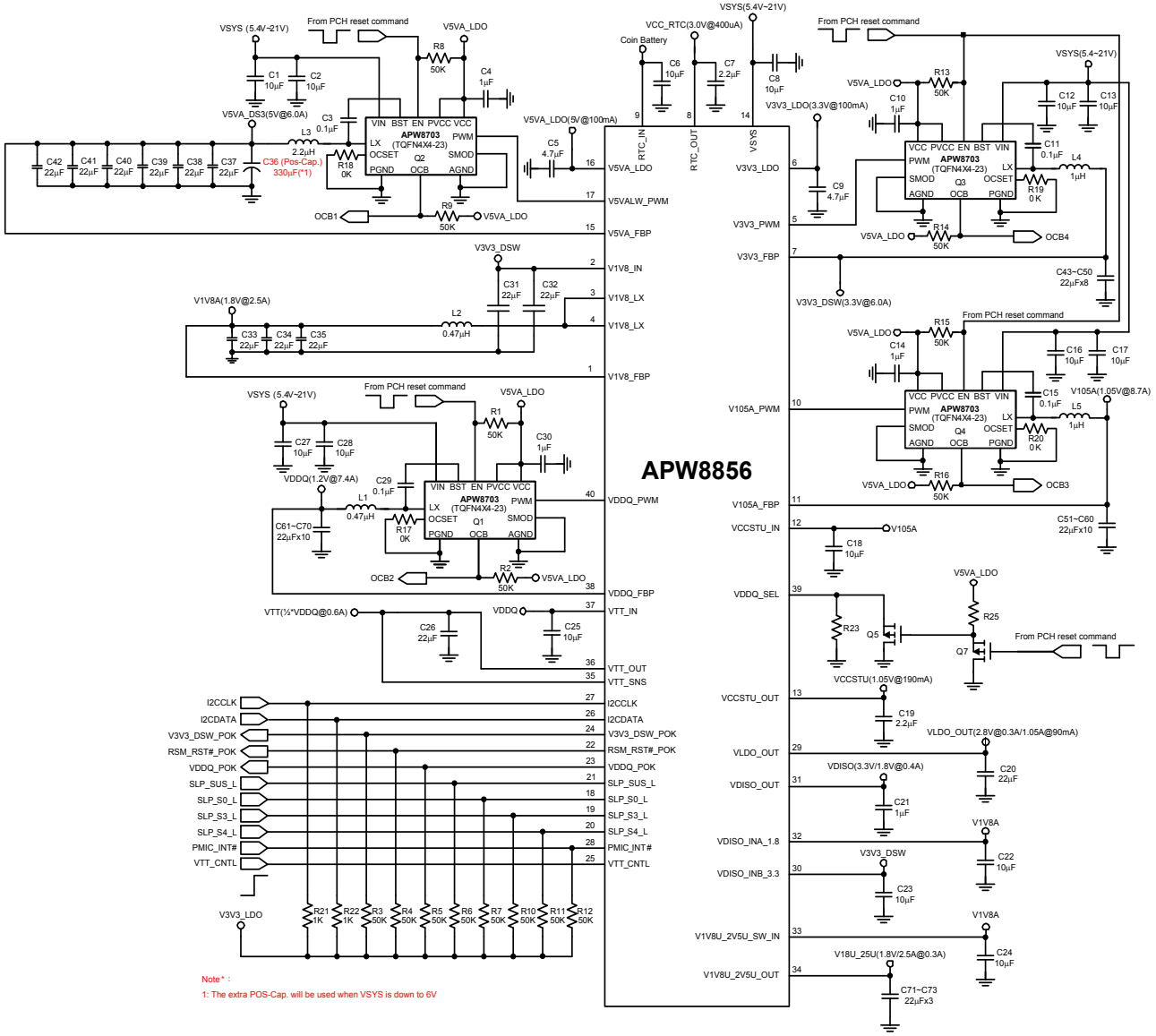
Note 3: Refer to the typical application circuit

9. Block Diagram

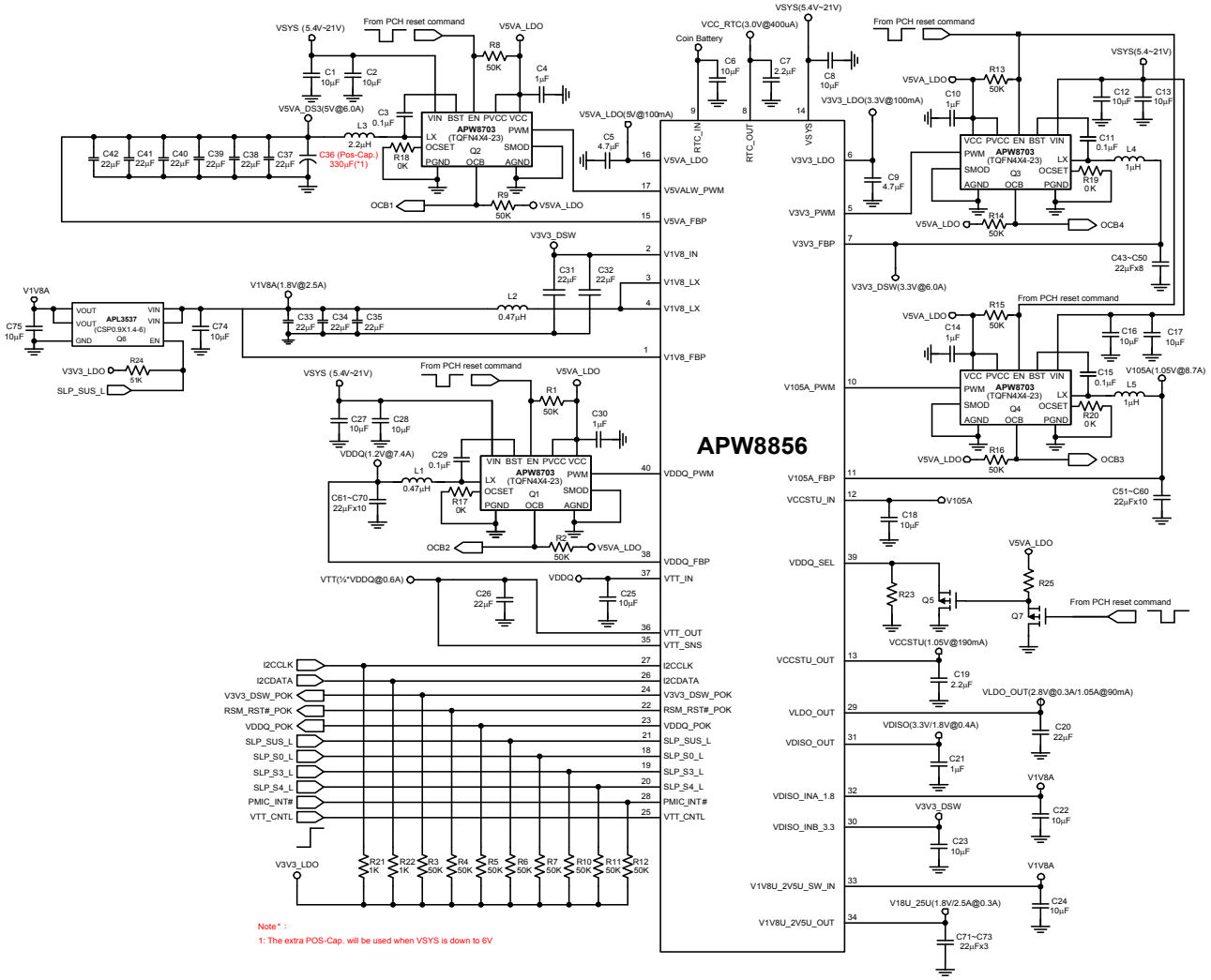


10. Typical Application Circuit

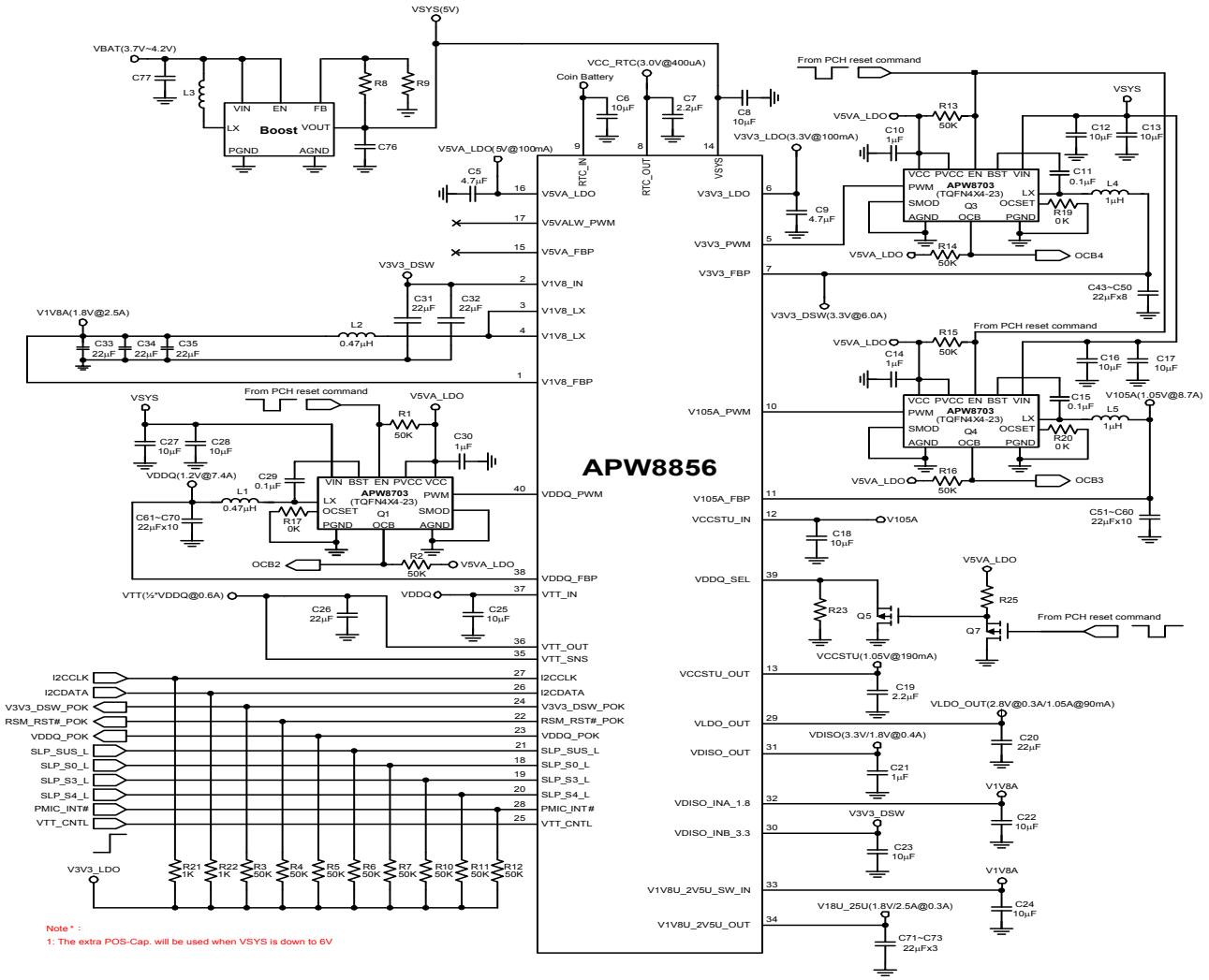
10.1 Typical Application Circuit, not support DS3



10.2 Typical Application Circuit, support DS3



10.3 Typical Application Circuit, support 1S battery



10.4 Bill of Materials of Typical Application Circuit, not support DS3

Designator	Quantity	Value	Description	Package Reference	Part Number	MFR
C3, C11, C15, C29	4	0.1μF	Cap, Ceramic, 10V, X7R, 20%	0603	LLL185R71A104MA01#	Murata
C4, C10, C14, C21, C30	5	1μF	Cap, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J105KA01#	Murata
C7, C19	2	2.2μF	Cap, Ceramic, 6.3V, X7R, 10%	0603	GCM185R60J225KE26#	Murata
C8, C9	2	4.7μF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM319R61A475KA01#	Murata
C6, C18, C22, C23, C24, C25	6	10μF	Cap, Ceramic, 6.3V, X5R, 10%	1206	GRM319R60J106KE19#	Murata
C1, C2, C8, C12, C13, C16, C17, C27, C28	9	10μF	Cap, Ceramic, 35V, X5R, 10%	1206	GRM31CR6YA106KA12#	Murata
C20, C26, C33, C34, C35, C51~60, C61~70	25	22μF	Cap, Ceramic, 6.3V, X5R, 20%	0805	MC05MTX6V3226	Viking
C31, C32, C71, C72, C73	5	22μF	Cap, Ceramic, 10V, X7R, 10%	1206	MC06KTB100226	Viking
C37~42, C43~50	14	22μF	Cap, Ceramic, 25V, X7R, 10%	1210	MC10KTB250106	Viking
C36	1	330μF	POSCAP,6.3V, 20%,15mOhm	D3L	6TPE330MFL	Panasonic
L3	1	2.2μH	Inductor, SMD, Molding, 12mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPC0603H-2R2MG-13M8-D	TAI_ECH
L4	1	1.0μH	Inductor, SMD, Molding, 6.9±15%mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPC0603H-1R0MG-6M9-D	TAI_ECH
L1,L2, L5	3	0.47μH	Inductor, SMD, Molding, 3.4mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPA0603S-R47MN-D	TAI_ECH
R23	1	NA	RES, 5%	0402		
R1,R2,R3,R4,R5, R6,R7,R8,R9,R10, R11,R12,R13,R14, R15,R16	16	50kOhm	RES, 5%	0402		
R21, R22	2	1kOhm	RES, 5%	0402		
R17,R18,R19,R20	4	0Ohm	RES, 5%	0402		
Q5, Q7	2	-	PNP BJT transistor	SOT-23		
Q1, Q2, Q3, Q4	4	-	Power Stage	TQFN4x4-23	APW8703	ANPEC
U1	1	-	PMIC	TDFN5x-40	APW8856	ANPEC

10.5 Bill of Materials of Typical Application Circuit, support DS3

Designator	Quantity	Value	Description	Package Reference	Part Number	MFR
C3, C11, C15, C29	4	0.1μF	Cap, Ceramic, 10V, X7R, 20%	0603	LLL185R71A104MA01#	Murata
C4, C10, C14, C21, C30	5	1μF	Cap, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J105KA01#	Murata
C7, C19	2	2.2μF	Cap, Ceramic, 6.3V, X7R, 10%	0603	GCM185R60J225KE26#	Murata
C8, C9	2	4.7μF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM319R61A475KA01#	Murata
C6, C18, C22, C23, C24, C25, C74, C75	6	10μF	Cap, Ceramic, 6.3V, X5R, 10%	1206	GRM319R60J106KE19#	Murata
C1, C2, C8, C12, C13, C16, C17, C27, C28	9	10μF	Cap, Ceramic, 35V, X5R, 10%	1206	GRM31CR6YA106KA12#	Murata
C20, C26, C33, C34, C35, C51~60, C61~70	25	22μF	Cap, Ceramic, 6.3V, X5R, 20%	0805	MC05MTX6V3226	Viking
C31, C32, C71, C72, C73	5	22μF	Cap, Ceramic, 10V, X7R, 10%	1206	MC06KTB100226	Viking
C37~42, C43~50	14	22μF	Cap, Ceramic, 25V, X7R, 10%	1210	MC10KTB250106	Viking
C36	1	330μF	POSCAP, 6.3V, 20%,15mOhm	D3L	6TPE330MFL	Panasonic
L3	1	2.2μH	Inductor, SMD, Molding, 12mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPC0603H-2R2MG-13M8-D	TAI_TECH
L4	1	1.0μH	Inductor, SMD, Molding, 6.9±15%mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPC0603H-1R0MG-6M9-D	TAI_TECH
L1,L2, L5	3	0.47μH	Inductor, SMD, Molding, 3.4mOhm	0630, 7.3mm x 6.6mm x 2.8mm	TMPA0603S-R47MN-D	TAI_TECH
R23	1	NA	RES, 5%	0402		
R1,R2,R3,R4,R5, R6,R7,R8,R9,R10, R11,R12,R13,R14, R15,R16	16	50kOhm	RES, 5%	0402		
R21, R22	2	1kOhm	RES, 5%	0402		
R17,R18,R19,R20	4	0Ohm	RES, 5%	0402		
Q6	1	-	Load switch	SOT-23	APL3537	ANPEC
Q5, Q7	2	-	PNP BJT transistor	SOT-23		
Q1, Q2, Q3, Q4	4	-	Power Stage	TQFN4x4-23	APW8703	ANPEC
U1	1	-	PMIC	TDFN5x-40	APW8856	ANPEC

11. Pin Description

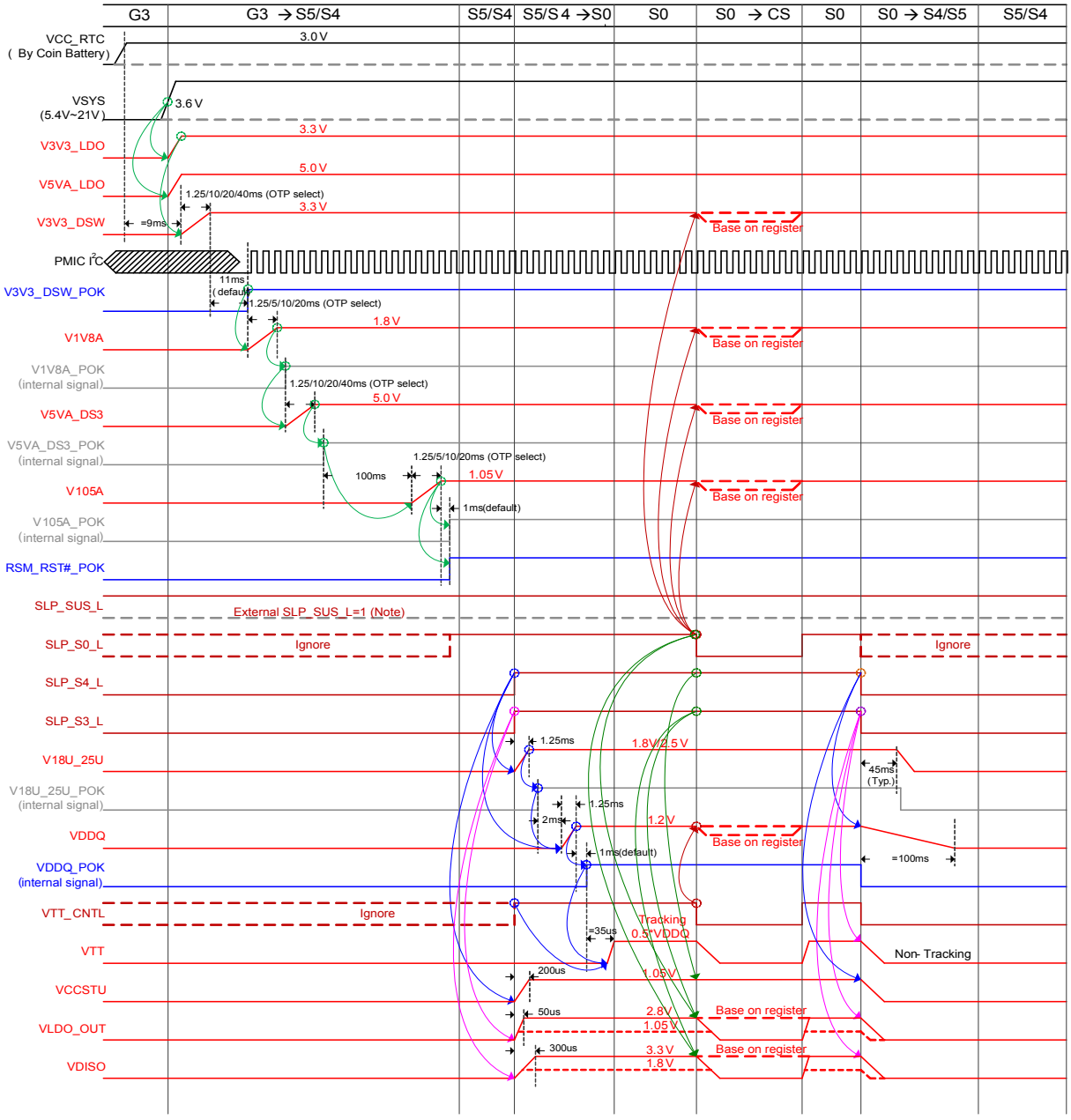
PIN		FUNCTION
NO.	NAME	
1	V1V8A_FBP	This pin provides the feedback for the 1.8V switching regulator. Connect this pin to the output of the 1.8V switching regulator output.
2	V1V8A_IN	V1V8A PWM regulator input pin.
3	V1V8A_LX	V1V8A PWM regulator LX Pin. Connect to external inductor for output LC filter.
4	V1V8A_LX	V1V8A PWM regulator LX Pin. Connect to external inductor for output LC filter.
5	V3V3_PWM	V3V3 PWM signal output pin. Connect to external power stage's PWM input pin.
6	V3V3_LDO	V3V3_LDO output pin
7	V3V3_FBP	This pin provides the feedback for the 3.3V PWM controller as well as supplying input power to the 3.3V LDO ,as well as the V9 internal 2.5VLDO regulator. Connect this pin to the output of the 3.3V switching regulator via a trace capable of carrying at least 1A with less than 30mV drop.
8	RTC_OUT	RTC output voltage pin.
9	RTC_IN	RTC input voltage pin. Provide a coin battery power into this pin to enable LDO_RTC output.
10	V105A_PWM	V105A PWM signal output pin. Connect to external power stage's PWM input pin.
11	V105A_FBP	V105A output voltage feedback pin.
12	VCCSTU_IN	VCCSTU LDO input Pin.
13	VCCSTU_OUT	VCCSTU LDO output Pin.
14	VSYS	IC power input pin.
15	V5VA_FBP	This pin provides the feedback for the V5VA_DS3 PWM controller as well as supplying input power to the V5VA_LDO. Connect this pin to the power plane of V5VA_DS3 switching regulator via a trace capable of carrying at least 100mA with less than 10mV drop.
16	V5VA_LDO	V5VA_LDO output pin
17	V5VALW_PWM	V5VA PWM signal output pin. Connect to external power stage's PWM input pin.
18	SLP_S0_L	Input pin for receiving command to enter low power mode (LPM). L: Enter low power mode; V5VA_DS3, V3V3_DSW, V1V8A and V105A power rails are shut off. H: Exit LPM mode.
19	SLP_S3_L	L: Disable V3.3S, V1.8S. H: Enable these power rails.
20	SLP_S4_L	L: S3 state and disable VDDQ & V2.5U. H: Enable these power rails.
21	SLP_SUS_L	L: suspend state and disable all system ALW rails H: Enable all system ALW rails
22	RSM_RST#_POK	Power good indicator. Connect a resistor from RSM_RST#_POK to a pull-high voltage.
23	VDDQ_POK	Power good indicator. Connect a resistor from VDDQ_POK to a pull-high voltage.
24	V3V3_DSW_POK	Power good indicator. Connect a resistor from V3V3_DSW_POK to a pull-high voltage.
25	VTT_CNTL	VTT LDO enable.
26	I2CDATA	I2C data connection pin.
27	I2CCLK	I2C clock signal pin.
28	PMIC_INT#	PMIC_INT_L is an open drain output. This pin is used to alert (low active) the Embedded control (EC) when a fault condition occurs as defined in Function Description, Interrupt and Mask.
29	VLDO_OUT	LDO output pin.
30	VDISO_INB_3.3	VDISO 3.3V power input pin, as well as the power input of VLDO_OUT LDO regulator. Please connect this pin to V3V3_DSW's output if VDISO_OUT and/or VLDO_OUT are used.
31	VDISO_OUT	VDISO output pin.
32	VDISO_INA_1.8	VDISO 1.8V input Pin.
33	V1V8U_2V5U_SW_IN	Power input pin for V1.8U switch.

11. Pin Description (Cont.)

PIN		FUNCTION
NO.	NAME	
34	V1V8U_2V5U_OUT	Output pin of 2.5V-LDO or 1.8V load switch.
35	VTT_SNS	VTT output voltage feedback pin.
36	VTT_OUT	VTT sink/source LDO output pin.
37	VTT_IN	VTT sink/source LDO input pin.
38	VDDQ_FBP	VDDQ Positive Output Feedback Pin. Connect to VR5's output voltage.
39	VDDQ_SEL	VDDQ output select pin. Connect a 1% resistor from this pin to GND per Table 5 to select appropriate output voltage.
40	VDDQ_PWM	VDDQ PWM signal output pin. Connect to external power stage's PWM input pin.
Exposed Pad	PGND	IC Power Ground.

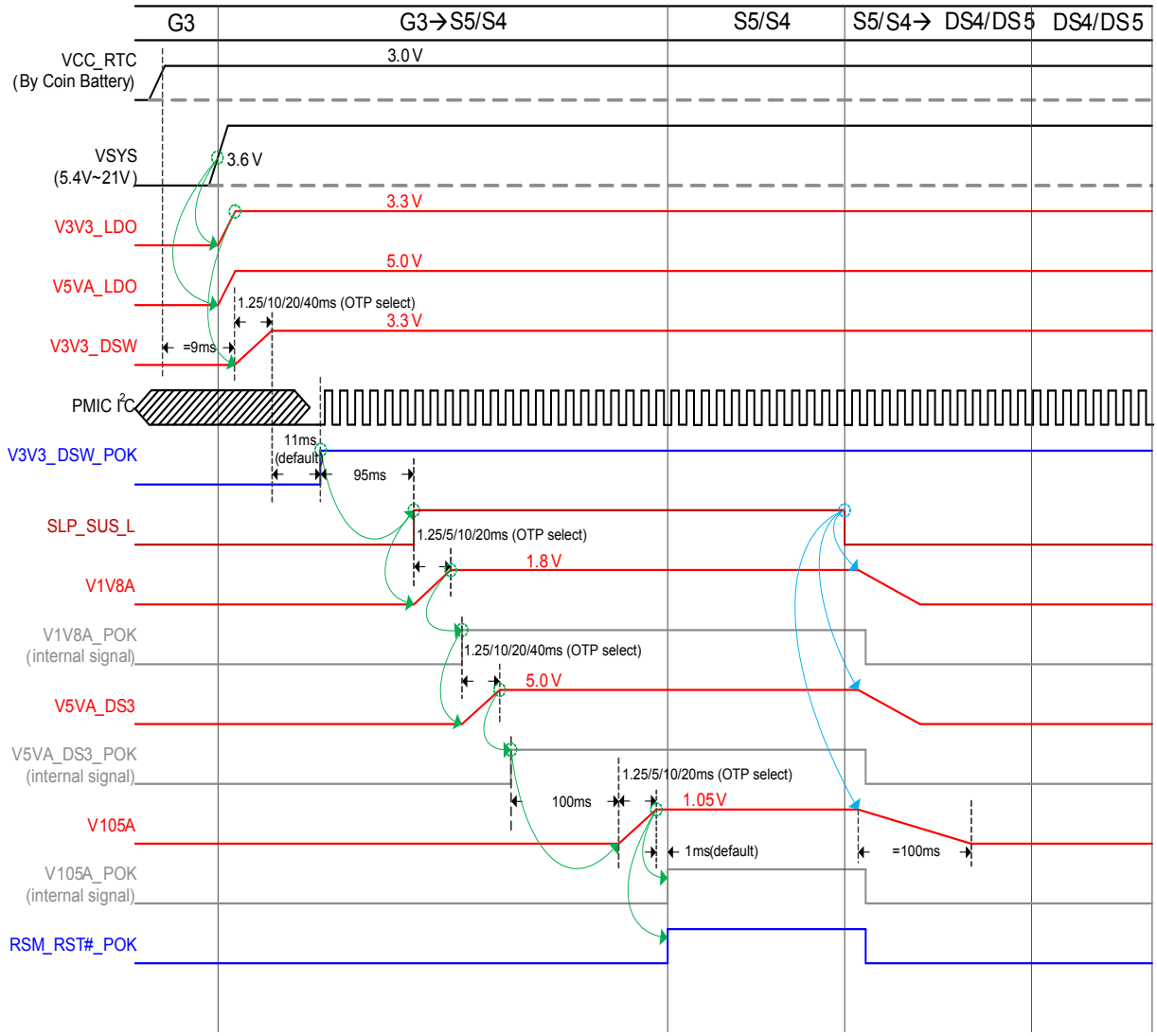
12. Power Sequence

12.1 Not support DS3/DS4/DS5

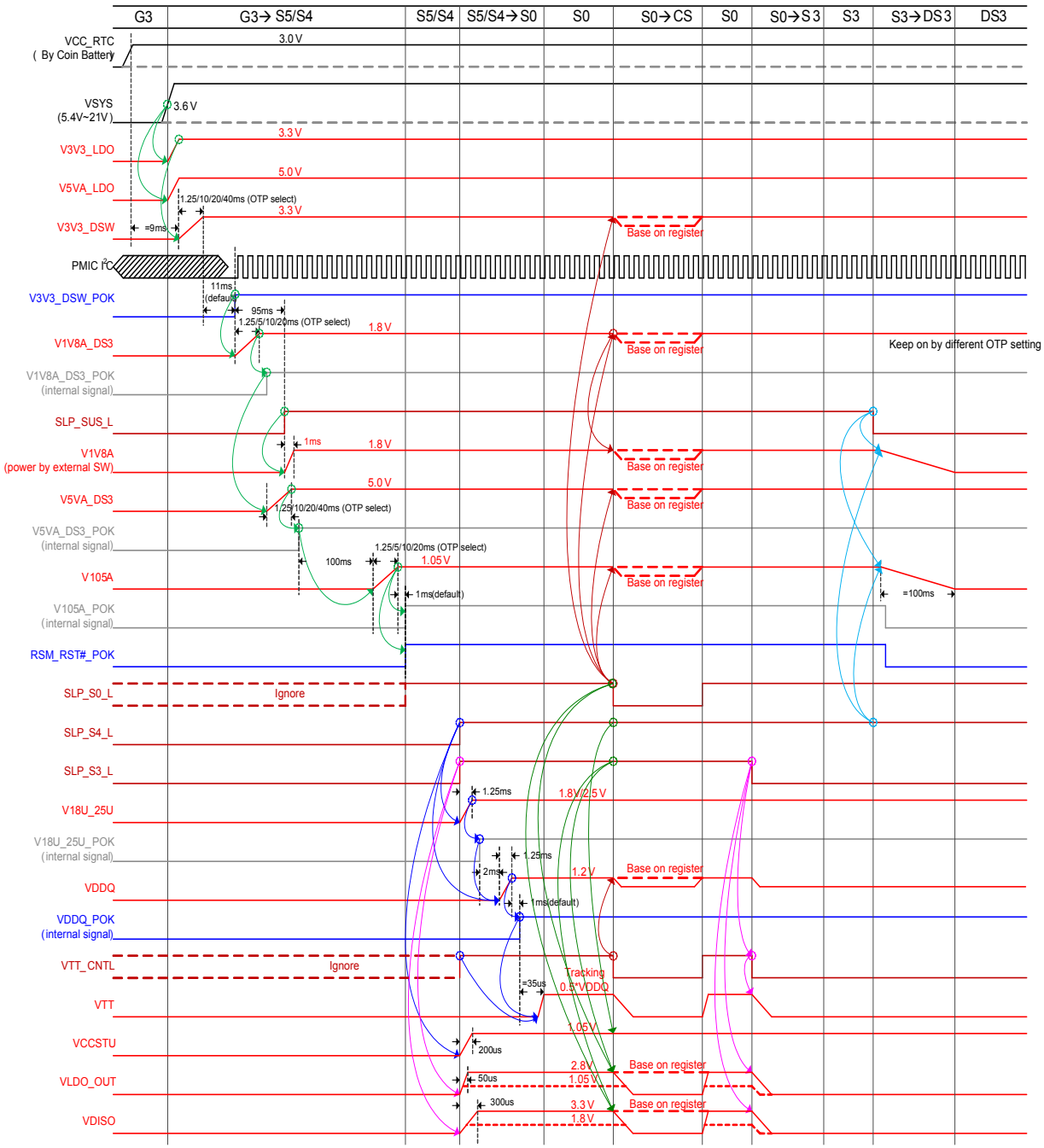


Note: SLP_SUS_L must be externally pulled high.

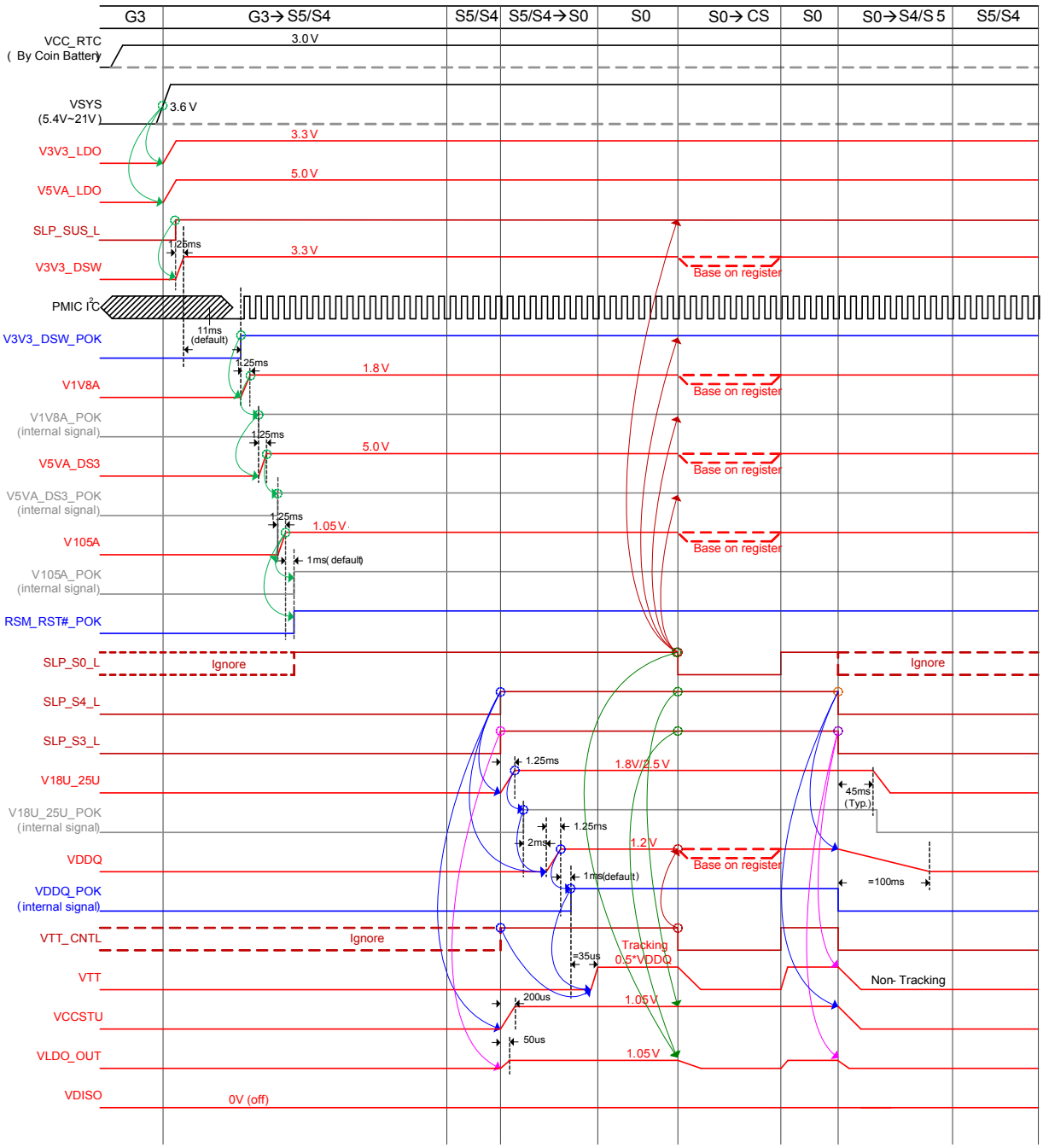
12.2 Support DS4/DS5, not support DS3



12.3 Support DS3



12.4 APW8856-08



13. Electrical Characteristics

13.1 Regulator Table

Table 1. PWM Controllers V5, V6, V10, V11

Symbol	Parameter	V5(V5A_DS3)	V6(V3.3A_DSW)	V10(VDDQ)	V11(V105A)	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	5	3.3	1.1/1.15/1.2/1.35 (selected by VDDQ_ SEL)	1.05	V
	Output Voltage Shift Range	-4% ~ +3%	-4% ~ +3%	-4% ~ +3%	-4% ~ +3%	
I_{OUT}	Continuous Output Current	–	–	–	–	A
I_{PEAK}	Peak Output Current	6	6	7.4	8.7	A
C_{IN}	Input Capacitor	>2 x 10	>2 x 10	>2x 10	>2x 10	µF
C_{OUT}	Output Capacitor	>6 x 22 +330 (for V_{VSYS} ≤6V)	>8 x 22	>10 x 22	>10 x 22	µF
ESR	Output Capacitor ESR	6	6	6	6	mΩ
L	Output Inductor	2.2	1.0	0.47	0.47	µH
DCR	Output Inductor DCR	<10	<10	<10	<10	mΩ

Table 2. PWM Converter V8

Symbol	Parameter	V8(V1V8A)	Unit
V_{IN}	Input Voltage	$V_{V3.3A\_DSW}$	V
V_{OUT}	Default Output Voltage	1.8	V
	Output Voltage Range	1.45~2.25	
I_{OUT}	Continuous Output Current	2	A
I_{PEAK}	Peak Output Current	2.5	A
C_{IN}	Input Capacitor	>2x 22	µF
C_{OUT}	Output Capacitor	>3 x 22	µF
ESR	Output Capacitor ESR	6	mΩ
L	Output Inductor	0.47	µH
DCR	Output Inductor DCR	<15	mΩ

Table 3. LDO Regulators V9(V25U), V14, V17 and Load Switches V9(18U), V15, V5A_DDO, V3V3_LDO

Symbol	Parameter	V9 (V18U_25U)	V13 (VTT)	V14 (VCC_RTC)	V17 (VLDO_OUT)	V5VA_LDO	V3V3_LDO	V15 (VDISO)	V16 (VCCSTU)	Unit
V_{IN}	Input Voltage	V_{V1V8A} / V_{V3V3_DSW}	V_{VDDQ}	V_{RTC_IN} (Coin Battery)	$V_{V3.3A\_DSW}$	V_{VSYS}	V_{VSYS}	$V_{V3.3A\_DSW}$/ $V_{V1.8A}$	V_{V105A}	V
V_{OUT}	Default Output Voltage	1.8/2.5	1/2*VDDQ	3.0	2.8	5	3.3	3.3	1.05	V
	Output Voltage Range	1.8/2.5 (VDDQ_SEL)			1.05/2.8 (OTP select)			3.3/1.8 (OTP select)		
I_{OUT}	Continuous Output Current	0.7/0.3	0.6	0.0004	0.3/0.09	0.1	0.1	0.4	0.09	A
C_{IN}	Input Capacitor	10	10	1	–	10	10	10	10	µF
C_{OUT}	Output Capacitor	3x 22	22	2.2	22	4.7	4.7	2.2	2.2	µF

13.2 [V5] V5VA_DS3 Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, V_{V5VA_DS3} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V5)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
V_DC(1%)	Output Voltage Accuracy	T_A= 25°C, V_{OUT}=5V	-35	-	35	mV
	Output Voltage Load Regulation	V_{VSYS} =8.4V, I_{OUT}=1A to 6A (-1mV/A)	–	5	–	mV
	Output Voltage Line Regulation	V_{VSYS} =8.4V to 21V, I_{OUT}=1A (0.4mV/V)	–	5	–	mV
	Output Voltage Temperature Regulation	V_{VSYS} =8.4V, I_{OUT}=1A, T_A= -40~85°C (| 0.2 | mV/10°C)	–	5	–	mV
V_AC(4%)	Load Transient Drop Voltage	tr=200ns, I_{OUT}=1.8A to 6A, Refer to the typical circuit	–	–	-200	mV
	Load Transient Overshoot Voltage	tf=200ns, I_{OUT}=6A to 1.8A, Refer to the typical circuit	–	–	200	mV
	Output Step Ramp Rate	DAC select in active mode	–	10	60	mV/μs
		Exit Connected Standby Mode	–	10	60	mV/μs
	Delay Time	From VR Enable assertion to the start of VR ramp	–	0	–	ms
	Soft-start Ramp Time	V_{OUT} 0%~100%	–	20	–	ms
	Soft-start Ramp Time Accuracy		-10	–	10	%
	Output Discharge Resistance		–	15	20	Ω
	Feedback Leakage Current	V_{V5VA_FBP} = 5.5V	–	–	80	μA
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{VSYS} =8.4V, V_{OUT}=5V, fsw=0.6MHz	540	600	660	kHz
		V_{VSYS} =8.4~20V, V_{OUT}=5V, fsw=0.6MHz	–	–	5	%
	Switching Frequency for high duty	V_{VSYS} =5.4V, V_{OUT}= 5.15V	–	180	200	kHz
	Minimum Off Time	V_{VSYS} =5.4~21V	–	200	230	ns
	Minimum Controllable On Time	V_{VSYS} =5.4~21V	–	100	130	ns
	PWM Sink Resistance	V_{V5VA_LDO} =5V	–	15	20	Ω
	PWM Source Resistance	V_{V5VA_LDO} =5V	–	15	20	Ω
	PWM Leakage Current	V_{V5VA_PWM}=5.5V	–		100	nA
PROTECTION						
	Under-voltage Protection (UVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V	65	70	75	%
	UVP Debounce TIme		-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Over-voltage Protection (OVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V	125	130	135	%
	OVP Debounce TIme			2	-	μs
5V LDO REGULATOR						
V_{SYS_5VEN}	VSYS Threshold to Enable V5VA_LDO	V_{VSYS} Rising	3.5	3.6	3.7	V
		Hysteresis	0.1	0.15	0.2	V
$V_{V5VA\_LDO\_POR}$	V5VA_LDO Power-on-reset (POR) Threshold	V_{V5VA_LDO} Rising, enable other VRs	4.15	4.3	4.45	V
		Hysteresis	0.1	0.15	0.2	V
	LDO Output Voltage	V_{VSYS} =5.4~21V, V_{V5VA_FBP}=0V, I_{OUT}=100mA	4.9	5	5.1	V
	LDO Dropout Voltage	I_{OUT}=100mA, V_{V5VA_LDO}=5V	-	-	0.4	V
	LDO Current Limit	T_A= 25°C	150	200	250	mA

13.2 [V5] V5VA_DS3 Electrical Characteristics (Cont.)

These specifications apply over V_{VSYS} = 8.4V, V_{V5VA_DS3} = 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V5)			Unit
			Min	Typ	Max	
	LDO over temperature protection	The first phase, junction temperature	-	120	-	℃
	Thermal Protection	The second phase, junction temperature	-	150	-	℃
	LDO Discharge Resistance		-	15	20	Ω
	LDO Power-on Delay	V_{VSYS}>V_{SYS_POR} to 5V_LDO soft-start starting	-	20	-	μs
V_{THBYP_5V}	Bypass Threshold	V5VA_DS3 Voltage Rising	-	4.68	-	V
		Hysteresis	-	100	-	mV
	Response time	From reaching target threshold to switch turning on	-	-	1	μs
	Bypass Switch On Resistance		-	1.5	3	Ω
	LDO Soft-start Time	C_{OUT}=4.7μF, V_{OUT}=5V	-	100	-	μs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM	-	-	50	μA
		VDC=8.4V, V_{OUT}=5V, I_{OUT}=1mA, CS mode, total power loss	-	0.814	-	mW
		VDC=8.4V, V_{OUT}=5V, I_{OUT}=6A, All combined PCB trace resistance less than 10mOhm	-	90	-	%

13.3 [V6] V3V3_DSW Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, V_{V3V3_DSW} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V6)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
V_DC(1%)	Output Voltage Accuracy	T_A = 25°C, V_{OUT}=3.3V	-20	-	20	mV
	Output Voltage Load Regulation	V_{VSYS} =8.4V, I_{OUT}=1.3A to 6A (-1mV/A)	-	5	-	mV
	Output Voltage Line Regulation	V_{VSYS} =8.4V to 21V, I_{OUT}=1.3A (0.4mV/V)	-	5	-	mV
	Output Voltage Temperature Regulation	V_{VSYS} =8.4V, I_{OUT}=1A, T_A= -40~85°C (| 0.2 | mV/10°C)	-	3	-	mV
V_AC(4%)	Load Transient Drop Voltage	tr=200ns, I_{OUT}=1.8A to 6A, Refer to the typical circuit	-	-	-130	mV
	Load Transient Overshoot Voltage	tf=200ns, I_{OUT}=6A to 1.8A, Refer to the typical circuit	-	-	130	mV
	Output Step Ramp Rate	DAC select in active mode	-	3.3	6.6	mV/μs
		Exit Connected Standby Mode	-	3.3	6.6	mV/μs
	Delay Time	From VR Enable assertion to the start of VR ramp	–	0	–	ms
	Soft-start Ramp Time	V_{OUT} 0%~100%	–	20	–	ms
	Soft-start Ramp Time Accuracy		-10	–	10	%
	Output Discharge Resistance		-	15	20	Ω
	Feedback Leakage Current	V_{V3V3_FBP} = 5.5V	-	-	100	μA
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{VSYS} =8.4V, V_{OUT}=3.3V, fsw=0.6MHz	540	600	660	kHz
		V_{VSYS} =8.4~21V, V_{OUT}=3.3V, fsw=0.6MHz	-	-	5	%
	Minimum Off Time	V_{VSYS} =5.4~21V	-	200	230	ns
	Minimum Controllable On Time	V_{VSYS} =5.4~21V	-	100	130	ns

13.3 [V6] V3V3_DSW Electrical Characteristics (Cont.)

These specifications apply over V_{VSYS} = 8.4V, V_{V3V3_DSW} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V6)			Unit
			Min	Typ	Max	
PWM GATE DRIVER (CONT.)						
	PWM Sink Resistance	V_{V5VA_LDO} =5V	-	15	20	Ω
	PWM Source Resistance	V_{V5VA_LDO} =5V	-	15	20	Ω
	PWM Leakage Current	V_{V3V_PWM}=5.5V	-	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V	65	70	75	%
	UVP Debounce TIme		-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Over-voltage Protection (OVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V	125	130	135	%
	OVP Debounce TIme		-	2	-	μs
3.3V LDO REGULATOR						
V_{SYS_UVLO}	VSYS Threshold to Enable V3V3_LDO	V_{VSYS} Rising, enable 3.3V_LDO	3.5	3.6	3.7	V
		Hysteresis	0.1	0.15	0.2	V
$V_{3V3\_LDO\_POR}$	3.3V_LDO Power-on-reset (POR) Threshold	V_{V3V3_LDO} Rising, enable other VRs	2.9	3	3.1	V
		Hysteresis	0.1	0.15	0.2	V
	LDO Output Voltage	V_{VSYS} =5.4~21V, $V_{V3.3A\_FBP}$=0V, I_{OUT}=100mA	3.234	3.3	3.366	V
	LDO Dropout Voltage	I_{OUT}=100mA, $V_{V3.3A\_LDO}$=3.3V	-	-	0.4	V
	LDO Current Limit	T_A = 25°C	150	200	250	mA
	LDO over temperature protection	The first phase, junction temperature	-	120	-	℃
		The second phase, junction temperature	-	150	-	℃
	LDO Discharge Resistance		-	15	20	Ω
	LDO Power-on Delay	V_{SYS}>V_{SYS_POR} to 3V_LDO soft-start starting	-	20	-	μs
V_{THBYP_3V}	Bypass Threshold	V3V3_DSW Voltage Rising	-	3.16	-	V
		Hysteresis	-	100	-	mV
	Response time	From reaching target threshold to switch turning on	-	-	1	μs
	Bypass Switch On Resistance		-	1.5	3	Ω
	LDO Soft-start Time	C_{OUT}=4.7μF, V_{OUT}=3.3V	-	100	-	μs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM	-	25	-	μA
		VDC=8.4V, V_{OUT}=3.3V, I_{OUT}=7mA, CS mode, total power loss	-	2.285	-	mW
		VDC=8.4V, V_{OUT}=3.3V, I_{OUT}=6A, All combined PCB trace resistance less than 10mOhm	-	90	-	%

13.4 [V8] V1V8A Electrical Characteristics

These specifications apply over V_{V1V8_IN} = V_{V3V3_DSW} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V8)			Unit
			Min	Typ	Max	
PWM CONTROLLER						
	Switching Frequency	V_{V1V8_IN} =3.3V, I_{OUT}=500mA, Setting to 2MHz	1.8	2	2.2	MHz
		Accuracy for 4 choices	-10	-	10	%
	Maximum Duty Cycle		100	-	-	%
	Minimum Controllable On Time		-	60	80	ns
	High-side MOSFET On Resistance	V_{V1V8_IN}=3.3V	-	55	-	mΩ
	Low-side MOSFET On Resistance	V_{V1V8_IN}=3.3V	-	40	-	mΩ
	Input Leakage Current	V8 is off, $V_{V1.8A\_IN}$=5.5V	-	-	1	μA
	LX Leakage Current	$V_{V1.8A\_LX}$ =5.5V, V_{V1V8_IN}=5.5V	-	-	1	μA
	Zero Current Offset		-5	-	5	mV
	PFM Current Limit	V_{IN}=3.3V, V_{OUT}=1.8V, fsw=2MHz	-	0.5	-	A
PWM OUTPUT VOLTEGE						
V_DC(1%)	Output Voltage Accuracy	T_A= 25°C, V_{OUT}=1.8V	-14	-	14	mV
	Output Voltage Load Regulation	V_{V1V8_IN} =3.3V, I_{OUT}=0.5A to 2.5A (-1mV/A)	-	2	-	mV
	Output Voltage Line Regulation	V_{V1V8_IN} =3.3V to 5V, I_{OUT}=0.5A (0.4mV/V)	-	0.7	-	mV
	Output Voltage Temperature Regulation	V_{V1V8_IN} =3.3V, I_{OUT}=0.5A, T_A= -40~85°C (｜ 0.2 ｜ mV/10°C)	-	1.3	-	mV
V_AC(4%)	Load Transient Drop Voltage	tr=200ns, I_{OUT}=0.75A to 2.5A, Refer to the typical circuit	-	-	-72	mV
	Load Transient Overshoot Voltage	tf=200ns, I_{OUT}=2.5A to 0.75A, Refer to the typical circuit	-	-	72	mV
	Output Step Ramp Rate	DAC select in active mode	-	18	60	mv/μs
		Exit Connected Standby Mode	-	18	60	mv/μs
	Delay Time	From VR Enable assertion to the start of VR ramp	–	0	–	ms
	Soft-start Ramp Time	V_{OUT} 0%~100%	–	10	–	ms
	Soft-start Ramp Time Accuracy		-10	–	10	%
	Output Discharge Resistance		-	15	20	Ω
	Feedback Leakage Current	V_{V1V8_FBP} = 5.5V	-	-	20	μA
PROTECTION						
	Under-voltage Protection (UVP)	V_{V1V8_IN} =3.3V	65	70	75	%
	UVP Debounce TIme		-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Over-voltage Protection (OVP)	V_{V1V8_IN} =3.3V	125	130	135	%
	OVP Debounce TIme			2	-	μs
I_{OCP3}	High-side MOSFET Over-current- Protection(OCP)	V_{V1V8_IN} =3.3V	3.5	4	4.5	A
	OCP Debounce TIme		-	2	-	μs

13.4 [V8] V1V8A Electrical Characteristics (Cont.)

These specifications apply over V_{V1V8_IN} = V_{V3V3_DSW} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V8)			Unit
			Min	Typ	Max	
PROTECTION (cont.)						
	Thermal Shutdown Protection	The first phase, junction temperature Rising	-	120	-	°C
		Hysteresis	-	20	-	°C
		The second phase, junction temperature Rising	-	150	-	°C
		Hysteresis	-	50	-	°C
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM	-	25	-	μA
		V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=2mA, CS mode, total power loss	-	0.552	-	mW
		V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=2.5A, All combined PCB trace resistance less than 10mOhm	-	90	-	%

13.5 [V9] V18U_25U Electrical Characteristics

These specifications apply over V18U_25U_IN = 3.3V, V18U_25U_OUT = 2.5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V9)			Unit`
			Min	Typ	Max	
REGULATOR OUTPUT						
	Output Voltage Accuracy	$V_{V18U\_25U\_IN}$ = 3.3V, $V_{V18U\_25U\_OUT}$ =2.5 V, T_A= 25°C	-12.5	-	12.5	mV
	Output Voltage Load/ Temperature Regulation	IOUT=4.5mA to 1000mA, T_A= -40~85°C	-	12.5	-	mV
	Output Load Transient Drop Voltage	tr=200ns, I_{OUT}=4.5mA to 1000mA, Refer to the typical circuit	-	-	-100	mV
	Output Load Transient Overshoot Voltage	tf=200ns, I_{OUT}=4.5mA to 1000mA, Refer to the typical circuit	-	-	100	mV
	Dropout Voltage	I_{OUT}=700mA	-	300	-	mV
	Output Discharge Resistance		-	15	20	Ω
	Output Noise	f=100 to 100kHz	-	100	-	μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	40	-	-	dB
T_{SS}	Soft-Start Time	Total time (delay+Ramp)	-	1.25	-	ms
	Current Limit		-	1.2	-	A
	Under Voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Output Voltage Soft-start	Total time (delay+Ramp)	0.9	1	1.1	ms
SWITCH OUTPUT						
	Switch On Resistance	Powered by V1V8A_FBP internally, I_{OUT}=1A	-	32	45	mΩ
t_{SS}	Soft-Start Time	Total time (delay+Ramp)	-	100	-	μs
	Over Current-Protection		-	3	-	A
`	Input Leakage Current	Loss from V1V8A_FBP	-	-	1	μA

13.6 [V10] VDDQ Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, V_{VDDQ} = 1.2V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(V10) Min	Typ	Max	Unit
PWM OUTPUT VOLTAGE							
V_DC(2%)	Output Voltage Accuracy	T_A = 25°C, V_{VDDQ} =1.1V		-7	-	7	mV
		T_A= 25°C, V_{VDDQ} =1.15V		-8	-	8	
		T_A= 25°C, V_{VDDQ} =1.2V		-9	-	9	mV
		T_A = 25°C, V_{VDDQ} =1.35V		-12	-	12	mV
	Output Voltage Load Regulation	V_{VSYS} =8.4V, I_{OUT}=0.7A to 7.4A (-1mV/A)		-	7	-	mV
	Output Voltage Line Regulation	V_{VSYS} =8.4V to 21V, I_{OUT}=1A (0.4mV/V)		-	5	-	mV
	Output Voltage Temperature Regulation	V_{VSYS} =8.4V, I_{OUT}=1A, T_A= -40~85°C (｜ 0.2 ｜ mV/10°C)		-	3	-	mV
	Feedback Leakage Current	$V_{VDDP\_ALW\_FBP}$ = 5.5V		-	-	100	nA
V_AC(3%)	Load Transient Drop / Overshoot Voltage	tr=tf=200ns, I_{OUT}=2.2A to 7.4A to 2.2A, Refer to the typical circuit	V_{VDDQ} =1.1V	-33	-	33	mV
			V_{VDDQ} =1.15V	-34.5	-	34.5	mV
			V_{VDDQ} =1.2V	-36	-	36	mV
			V_{VDDQ} =1.35V	-40	-	40	mV
	Output Step Ramp Rate	DAC select in active mode		-	-	60	mv/μs
		Exit Connected Standby Mode		-	-	35	μs
	Output Voltage Soft-start	Delay time, from enable command (1.8U_2.5U internal POK) to start ramping up		1.8	2	2.2	ms
		Ramp time		1.125	1.25	1.375	ms
	Output Discharge Resistance			-	15	20	Ω
	Feedback Leakage Current	V_{VDDQ_FBP} = 5.5V		-	-	120	μA
PWM GATE DRIVER							
	Switching Frequency Accuracy	V_{VSYS} =8.4V, V_{OUT}=5V, fsw=0.5MHz		450	500	550	kHz
		V_{VSYS} =8.4~21V, V_{OUT}=5V, fsw=0.5MHz		-	-	5	%
	Minimum Off Time	V_{VSYS} =5.4~21V		-	200	230	ns
	Minimum Controllable On Time	V_{VSYS} =5.4~21V		-	60	80	ns
	PWM Sink Resistance	V_{V5VA_LDO} =5V		-	15	20	Ω
	PWM Source Resistance	V_{V5VA_LDO} =5V		-	15	20	Ω
	PWM Leakage Current	V_{V5VA_PWM}=5.5V		-	-	100	nA
PROTECTION							
	Under-voltage Protection (UVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V		65	70	75	%
	UVP Debounce TIme			-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%		-	0.5	-	ms
	Over-voltage Protection (OVP)	V_{VSYS} =5.4~20V, V_{V5VA_LDO} =5V		125	130	135	%
	OVP Debounce TIme			-	2	-	μs

13.6 [V10] VDDQ Electrical Characteristics (Cont.)

These specifications apply over V_{VSYS} = 8.4V, V_{VDDQ} = 1.2V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V10)			Unit
			Min	Typ	Max	
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM	-	25	-	μA
		V_{VSYS} =8.4V, V_{VDDQ} =1.2V, I_{OUT}=8mA, CS mode, total power loss	-	2.708	-	mW
		V_{VSYS} =8.4V, V_{VDDQ} =1.2V, I_{OUT}=7.4A, All combined PCB trace resistance less than 10mOhm	-	86	-	%

13.7 [V11] V105A Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, V_{V105A} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V11)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
V_DC(2%)	Output Voltage Accuracy	T_A= 25°C, V_{V105A} =1.05V	-6	-	6	mV
	Output Voltage Load Regulation	V_{VSYS} =8.4V, I_{OUT}=1.5A to 10.5A (-1mV/A)	-	9	-	mV
	Output Voltage Line Regulation	V_{VSYS} =8.4V to 21V, I_{OUT}=1A (0.4mV/V)	-	5	-	mV
	Output Voltage Temperature Regulation	V_{VSYS} =8.4V, I_{OUT}=1.5A, T_A= -40~85°C (｜ 0.2 ｜ mV/10°C)	-	1	-	mV
V_AC(3%)	Load Transient Drop Voltage	tr=200ns, I_{OUT}=3.2A to 10.5A, Refer to the typical circuit	-	-	-31.5	mV
	Load Transient Overshoot Voltage	tf=200ns, I_{OUT}=10.5A to 3.2A, Refer to the typical circuit	-	-	31.5	mV
	Output Step Ramp Rate	DAC select in active mode	-	-	-	
		Exit Connected Standby Mode	-	-	-	
	Delay Time	from enable command to start ramping up (OTP adjustable)	-	100	-	ms
	Soft-start Ramp Time	V_{OUT} 0%~100%	–	10	–	ms
	Soft-start Ramp Time Accuracy		-10	–	10	%
	Output Discharge Resistance		-	15	20	Ω
	Feedback Leakage Current	V_{V105A_FBP} = 5.5V	-	-	120	μA
PWM GATE DRIVER						
	Switching Frequency Accuracy	V_{VSYS} =8.4V, V_{V105A} =1.05V, fsw=0.5MHz	450	500	550	kHz
		V_{VSYS} =8.4~21V, V_{V105A} =1.05V, fsw=0.5MHz	-	-	5	%
	Switching Frequency for low duty	V_{VSYS} =21V, V_{OUT}=0.95V	270	300	330	kHz
	Minimum Off Time	V_{VSYS} =5.4~21V	-	200	230	ns
	Minimum Controllable On Time	V_{VSYS} =5.4~21V	-	100	130	ns
	PWM Sink Resistance	V_{V5VA_LDO} =5V	-	15	20	Ω
	PWM Source Resistance	V_{V5VA_LDO} =5V	-	15	20	Ω
	PWM Leakage Current	V_{V105A_PWM}=5.5V	-	-	100	nA

13.7 [V11] V105A Electrical Characteristics (Cont.)

These specifications apply over V_{VSYS} = 8.4V, V_{V105A} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V11)			Unit
			Min	Typ	Max	
PROTECTION						
	Under-voltage Protection (UVP)	V_{VSYS} =5.4~21V, V_{V5VA_LDO} =5V	65	70	75	%
	UVP Debounce TIme		-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Over-voltage Protection (OVP)	V_{VSYS} =5.4~21V, V_{V5VA_LDO} =5V	125	130	135	%
	OVP Debounce TIme		-	2	-	μs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM	-	25	-	μA
		V_{VSYS} =8.4V, V_{V105A} =1.05V, I_{OUT}=16mA, CS mode, total power loss	-	4.2	-	mW
		V_{VSYS} =8.4V, V_{V105A} =1.05V, I_{OUT}=10.5A, All combined PCB trace resistance less than 10mOhm	-	75	-	%

13.8 [V13] VTT Electrical Characteristics

These specifications apply over V_{VTT_IN} = 1.2V, V_{VTT_OUT} = 0.6V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(V13)			Unit
				Min	Typ	Max	
SUPPLY CURRENT							
I_Q	Quiescent Current	I_{OUT} =0mA		-	25	30	μA
I_{SD}	Shutdown Current	I_{OUT} =0mA		-	-	1	μA
R_{DIS}	Output Discharge Resistance	During shutdown, the output voltage force 1V.		-	15	20	Ω
	Output Step Ramp Rate	Exit Connected Standby Mode		-	-	35	μs
T_{SS}	Soft-Start Time	Total time (delay+Ramp)		-	-	35	μs
OUTPUT VOLTAGE							
V_{OUT}	Output Voltage Range	0mA < I_{OUT} <600mA, T_A= -40~85°C, V_{VDDQ}=1.1V		522	550	578	mV
		0mA < I_{OUT} <600mA, T_A= -40~85°C, V_{VDDQ} =1.15V		546	575	604	mV
		0mA < I_{OUT} <600mA, T_A= -40~85°C, V_{VDDQ} =1.2V		570	600	630	mV
		0mA < I_{OUT} <600mA, T_A= -40~85°C, V_{VDDQ} =1.35V		641	675	709	mV
V_{TRAN}	AC Output Transient Voltage	Output voltage set to any voltage. I_{OUT} =27mA to 100mA to 27mA, t_R = t_F = 0.1μs		-	-	-	mV
PSRR	Ripple Rejection	C_{OUT} =4.7μF, I_{OUT} =100mA	f =1kHz	-	70	-	dB
			f =10kHz	-	63	-	dB
			f =100kHz	-	35	-	dB
V_{NOISE}	Output Noise	f =10 to 100kHz, C_{OUT} =4.7μF, I_{OUT} =100mA.		-	100	-	μV_{RMS}

13.8 [V13] VTT Electrical Characteristics (Cont.)

These specifications apply over V_{VTT_IN} = 1.2V, V_{VTT_OUT} = 0.6V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(V13)			Unit
				Min	Typ	Max	
DROPOUT VOLTAGE							
V_{DROP}	Dropout Voltage	V_{VTT_OUT} = 1.2V, I_{OUT} = 100mA	T_J = 25°C	–	-	-	mV
			T_J = -40 to 85°C	–	-	-	mV
Current Limit Protection							
I_{LIM}	Current-Limit Level	Source and Sink, T_J = -40 to 85°C		0.9	1.25	-	A
	Under-voltage Protection (UVP)	V_{IN} =1.1~1.35V		65	70	75	%
	UVP Debounce TIme			-	2	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%		-	50	-	μs

13.9 [V14] VCC_RTC Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{RTC_IN} =3.3V, T_A = -40 to 85°C. Typical values are at T_A =25°C.

Symbol	Parameter	Test Conditions	APW8856(V14)			Unit
			Min	Typ	Max	
OUTPUT VOLTAGE						
	Output Voltage	V_{RTC_IN}=3.3V, 0mA < I_{OUT} <0.4mA	-	3	-	V
	Line Regulation	V_{RTC_IN} =3.3 to 5.25V, V_{RTC_IN} =3V, I_{OUT} =10μA	-	0.01	-	%/V
	Load Regulation	I_{OUT} =0 to 10mA	-	0.05	-	%
$I_{OUT(MAX)}$	Maximum Output Current		-	-	0.4	mA
	Input leakage current	V_{RTC_IN} =5V	-	-	1	μA
	Output leakage current	V_{RTC_OUT} =5V	-	-	1	μA

13.10 [V17]VLDO_OUT Electrical Characteristics

These specifications apply over V_{IN} = V3V3_FBP = 3.3V, VLDO_OUT= 1.05V/2.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(V17)			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_Q	Quiescent Current	I_{OUT} =0mA	–	25	30	μA
I_{SD}	Shutdown Current	I_{OUT} =0mA	–	–	1	μA
R_{DIS}	Output Discharge Resistance	During shutdown, the output voltage force 1V.	–	15	20	Ω
	Output Step Ramp Rate	DAC select in active mode	-	-	-	μs
t_{SS}	Soft-Start Time	C_{OUT}=4.7μF, Vout=2.8V and 1.05V	-	50	65	μs

13.10 [V17]VLDO_OUT Electrical Characteristics (Cont.)

These specifications apply over V_{IN} = V3V3_FBP = 3.3V, VLDO_OUT= 1.05V/2.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(V17) Min	Typ	Max	Unit
OUTPUT VOLTAGE							
V_{OUT}	Output Voltage accuracy for high level	0mA < I_{OUT} <300mA, T_A= -40~85°C		2660	2800	2940	mV
	Output Voltage accuracy for low level	0mA < I_{OUT} <90mA, T_A= -40~85°C		1020	1050	1080	mV
V_{TRAN}	AC Output Transient Voltage for high level	Output voltage set to any voltage. I_{OUT} =90mA to 300mA to 27mA, t_R = t_F = 0.1μs		-	-	-	mV
	AC Output Transient Voltage for low level	Output voltage set to any voltage. I_{OUT} =90mA to 300mA to 27mA, t_R = t_F = 0.1μs		-	-	-	mV
PSRR	Ripple Rejection	C_{OUT} =4.7μF, I_{OUT} =100mA.	f =1kHz	-	70	-	dB
			f =10kHz	-	63	-	dB
			f =100kHz	-	35	-	dB
V_{NOISE}	Output Noise	f =10 to 100kHz, C_{OUT} =4.7μF, I_{OUT} =100mA.		-	100	-	μV_{RMS}
DROPOUT VOLTAGE							
V_{DROP}	Dropout Voltage	I_{OUT} = 300mA	V_{OUT} = 2.8V, T_J = 25°C	-	30	-	mV
			V_{OUT} = XXV, T_J = 25°C	-	-	-	mV
Current Limit Protection							
I_{LIM}	Current-Limit Level	T_J = -40 to 85°C		1	1.25	1.5	A
	Under-voltage Protection (UVP)	V_{IN} =1.1~1.35V		65	70	75	%
	UVP Debounce TIme			-	2	-	ms
	UVP enable delay time	Extend time when regulate voltage reach 100%		-	50	-	μs

13.11 VCCSTU Power Load Switch Electrical Characteristics

These specifications apply over V_{IN} = V_{V105A} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856 Min	Typ	Max	Unit
SUPPLY CURRENT							
I_Q	Quiescent Current	I_{OUT} =0mA		–	20	25	μA
	Input Leakage Current	Shutdown Condition		–	–	1	μA
	Output Leakage Current	Shutdown Condition, VOUT=5.5V		–	–	1	μA
DROPOUT VOLTAGE							
$R_{DS(ON)}$	Power Switch On Resistance	V_{IN} =1.05V, I_{OUT} = 190mA	T_J= 25°C	–	60	65	mΩ
R_{DIS}	VOUT Discharge Resistance	During shutdown, the output voltage force 1V.		–	15	20	Ω
t_{SS}	Soft-Start Time			–	200	–	μs
	Over Current-Protection			1	3	-	A

13.12 VDISO Power Load Switch Electrical Characteristics

These specifications apply over VIN = 3.3V/1.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(V17)			Unit
				Min	Typ	Max	
SUPPLY CURRENT							
I_Q	Quiescent Current	I_{OUT} =0mA		–	50	60	μA
	Input Leakage Current	Shutdown Condition		–	–	1	μA
	Output Leakage Current	Shutdown Condition		–	–	1	μA
DROPOUT VOLTAGE							
$R_{DS(ON)}$	Power Switch On Resistance	V_{IN} = 3.3V, I_{OUT} = 400mA	T_J= 25°C	–	–	60	mΩ
		V_{IN} = 1.8V, I_{OUT} = 400mA	T_J= 25°C	–	–	60	mΩ
R_{DIS}	VOUT Discharge Resistance	During shutdown, the output voltage force 1V.		–	15	20	Ω
t_{SS}	Soft-Start Time			–	300	350	μs
	Over Current-Protection			1.5	3	–	A

13.13 VSYS & POK & Logic Control Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8856(POK)			Unit
			Min	Typ	Max	
VSYS POR						
V_{VSYS_POR}	VSYS Power On Reset Threshold	V_{VSYS} Rising	-	5.3	5.37	V
V_{VSYS_SD}	VSYS Emergency Shutdown Threshold	V_{VSYS} Falling	-	5.2	-	V
VSYS SUPPLY CURRENT						
	VSYS Supply Current	V_{VSYS}=19V, SLP_SUS_L=Low, V5VA_LDO, V3V3_LDO(switchover), LDO_RTC and V3.3_DSW are alive	-	110	-	μA
		VSYS=19V, S0 state, all VR are on, PWM VRs are no switching	-	TBD	-	μA
POK						
	POK Threshold	Internal POK of VRs in from Lower (POK goes high)	87	90	93	%
		Internal POK de-assertion (POK goes low)	125	130	135	%
			84	87	90	%
	POK Enable Blanking Time	From VRs rise to 90% of their set point to POK goes High	-	1000	-	μs
	POK Disable Blanking Time	From VRs fall to 87% or rise to 130% of their set point to POK goes Low	10	20	25	μs
	V3V3_DSW_POK Enable Blanking Time	From all ANDed gate condition meet to POK goes high (Default, OTP adjustable)	10	-	-	ms
	RSM_RST#_POK Enable Blanking Time	From all ANDed gate condition meet to POK goes high (Default, OTP adjustable)	-	1	-	ms

13.13 VSYS & POK & Logic Control Electrical Characteristics

These specifications apply over V_{VSYS} = 8.4V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8856(POK)			Unit
				Min	Typ	Max	
	VDDQ_POK Enable Blanking Time	From all ANDed gate condition meet to POK goes high (Default, OTP adjustable)		-	1	-	ms
	External POK Leakage Current	$V_{V3V3\_DSW\_POK}$ / $V_{RSM\_RST\#\_POK}$ / V_{VDDQ_POK} = 5V		-	0.1	1	μA
	External POK Low Voltage	$I_{V3V3\_DSW\_POK}$ / $I_{RSM\_RST\#\_POK}$ / I_{VDDQ_POK} =4mA, sink		-	0.5	1	V
PMIC_INT_L							
	Leakage Current	$V_{PMIC\_INT\_L}$ = 5V		-	0.1	1	μA
	Low Voltage	I_{sink} =4mA		-	0.5	1	V
SLP_S0_L / SLP_S3_L / SLP_S4_L / VTT_CNTL							
	Input Logic Threshold	SLP_S0_L, SLP_S3_L, SLP_S4_L	voltage rising	-	-	1.2	V
		VTT_CNTL		-	-	1.0	V
		SLP_S0_L, SLP_S3_L, SLP_S4_L, VTT_CNTL	voltage falling	0.4	-	-	V
	Leakage Current	Voltage=5V		-	-	1	μA
t_{DCTL}	debounce time			-	2	-	μs
VDDQ_SEL							
	Input Logic Threshold 1			-	-	0.3	V
	Input Logic Threshold 2			0.55	-	0.65	V
	Input Logic Threshold 3			1.0	-	1.2	V
	Input Logic Threshold 4			1.5	-	1.8	V
	Input Logic Threshold 5			2.5	-	2.8	V
	Input Logic Threshold 6			3	-	3.3	V
	Output setting current	-40~85°C		9	10	11	μA

13.14 I2C Electrical Characteristics

Timing characteristics for I2C Interface signals over recommended operating conditions (unless otherwise noted).

Symbol	Parameter	Fast Speed Plus		Fast Speed		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Frequency, SCL	-	1	-	0.4	MHz
$t_{W(H)}$	Pulse Duration, SCL High	260	-	600	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low	500	-	1300	-	ns
t_r	Rise Time, SCL and SDA	-	120	20+0.1 C_L(pF)	300	ns
tf	Fall Time, SCL and SDA	-	120	20+0.1 C_L(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	-	-	100	-	ns
t_{hold1}	Hold Time, SCL to SDA	-	-	0	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition	500	-	1300	-	ns
t_{setup2}	Setup Time, SCL to Start Condition	-	-	600	-	ns
t_{hold2}	Hold Time, Start condition to SCL	-	-	600	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition	-	-	600	-	ns
C_L	Load Capacitance for Each Bus Line	-	-	-	400	pF
C_{PAR}	Pin to GND Parasitic Capacitance, I2CCLK pin or I2CDATA pin of APW8856 (Note 4)	-	13	-	13	pF

Note 4: Guaranteed by design, not tested in production.

14. Register Description

14.1 Register Map

Register Name	Register Address	Bits								Read/Write/Read Only State	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
VENDORID	0x00	1	0	1	0	1	1	0	0	R	0xAC
REVID	0x01	0	0	0	0	1	0	0	0	R	0x08
IRQLVL1	0x02	0	0	0	0	0	0	0	0	R	0x00
PWRSRCINT	0x04	0	0	0	0	0	0	0	0	R/W	0x00
PMUINT	0x05	0	0	0	0	0	0	0	0	R/W	0x00
RESETIRQ1	0x08	0	0	0	0	0	0	0	0	R/W	0x00
RESETIRQ2	0x09	0	0	0	0	0	0	0	0	R/W	0x00
MPMUINT	0x0B	0	0	0	1	1	1	1	1	R/W	0x1F
MPWRSRCINT	0x0C	0	0	1	1	1	1	1	1	R/W	0x3F
SOFTSTART1	0x0D	0	0	0	0	1	0	1	0	R/W	0x0A
SOFTSTART2	0x0E	0	0	1	0	1	0	1	0	R/W	0x2A
RESETIRQ1MASK	0x11	0	0	1	1	0	0	0	0	R/W	0x30
RESETIRQ2MASK	0x12	0	0	0	0	0	0	1	0	R/W	0x02
IRQLVL1MSK	0x13	1	0	1	1	0	1	1	1	R/W	0xB7
PWRSTAT1	0x16	0	0	0	0	0	0	0	0	R/W	0x00
PWRSTAT2	0x17	0	0	0	0	0	0	0	0	R/W	0x00
PGMASK1	0x18	0	0	0	0	0	0	0	0	R/W	0x00
PGMASK2	0x19	0	0	0	0	0	0	0	0	R/W	0x00
V5VADS3CNT	0x31	0	0	1	0	1	0	1	0	R/W	0x2A
V3V3DSWCNT	0x32	0	0	1	0	1	0	1	0	R/W	0x2A
V1V8ACNT	0x34	0	0	1	0	1	0	1	0	R/W	0x2A
V18U25UCNT	0x35	0	0	1	0	1	0	1	0	R/W	0x2A
VDDQCNT	0x36	0	0	1	1	1	0	1	0	R/W	0x3A
V105ACNT	0x37	0	0	0	0	1	0	1	0	R/W	0x0A
VRMODECTRL	0x3B	0	1	1	1	1	1	1	1	R/W	0x1F
DISCHGCNT2	0x3D	0	1	0	1	0	1	0	1	R/W	0x55
DISCHGCNT3	0x3E	0	1	0	1	0	1	0	1	R/W	0x55
VREN	0x41	0	0	0	0	0	0	0	0	R/W	0x00
REGLOCK	0x42	0	0	0	0	0	0	0	0	R/W	0x00
VRENPINMASK	0x43	0	0	0	0	0	0	0	0	R/W	0x00
SDWNCTRL	0x49	0	0	0	0	0	0	0	0	R/W	0x00
-	0x54	0	0	0	0	0	0	0	0	R/W	0x00
V3P3A_DSW_POK BLANKING TIME	0x55	0	1	0	1	0	1	0	1	R/W	0x55
RSM_RST#_POK BLANKING TIME	0x56	0	1	1	1	1	1	0	0	R/W	0x7C
VDDQ_POK BLANKING TIME	0x57	0	0	1	0	0	0	0	0	R/W	0x20
VR_PG BLANKING TIME	0x58	0	0	0	1	0	0	1	1	R/W	0x13
V5VA_DS3_PG to V1P05 EN DELAY TIME	0x59	0	1	1	0	0	0	1	1	R/W	0x63

14.1 Register Map (Cont.)

Register Name	Register Address	Bits								Read/Write/Read Only State	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
VDDQ_PG FALLING to V9 EN DELAY TIME	0x5A	0	0	1	0	1	1	0	1	R/W	0x2D
V18U_25U_PG to VDDQ_EN DELAY TIME	0x5B	0	0	1	1	1	1	1	1	R/W	0x3F
VDDQ_SEL TO LOW DEBOUNCE TIME	0x5C	1	1	1	0	1	0	1	0	R/W	0xEA
-	0x5D	0	0	0	0	0	1	1	1	R/W	0x07
-	0x5E	0	0	0	0	0	0	0	0	R/W	0x00
-	0x5F	0	0	0	0	0	0	0	0	R/W	0x00
-	0x60	0	0	1	1	0	0	1	0	R/W	0x32
-	0x61	0	0	0	1	1	0	1	0	R/W	0x1A
-	0x62	0	0	0	0	0	0	0	0	R	0x00
-	0x63	0	0	0	0	0	0	0	0	R	0x00
-	0x64	0	0	0	0	0	0	0	0	R	0x00

14.2 Vendor ID Register Table

Address	0x00							
Field Name	**VENDORID [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VENDORID [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power On Default	1	0	1	0	1	1	0	0
Bit Name	**Bit Definition**							
VENDORID [7:0]	Vendor ID functions the same as SVID Vendor ID. Vendor ID is assigned by Intel. This register is mandatory and the VR must return the assigned vendor ID.							

14.3 Rev ID Register Table

Address	0x01							
Field Name	**REVID [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MAJREV[3:0]				PREMIUMVOLUME	MINREV[2:0]		
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	1	0	0	0
Bit Name	**Bit Definition**							
MAJREV[3:0]	-							
PREMIUMVOLUME	Indicate PMIC follows Premium or Volume register map 0 = premium register map 1 = volume register map							
MINREV[2:0]	Minor Revision ID (from OTP)							

14.4 IRQLVL1 Register Table

Address	0x02							
Field Name	**IRQLVL1 [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RESET	-	PMU	-	-	PWRSRC	-	-
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RESET	0 = Reset IRQ not asserted 1 = Reset IRQ asserted							
PMU	0 = PMU IRQ not asserted 1 = PMU IRQ asserted							
PWRSRC	0 = PWRSRC IRQ not asserted 1 = PWRSRC IRQ asserted							

14.5 PWRSRCINT Register Table

Address	0x04							
Field Name	**PWRSRCINT [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	PMICHOT	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
PMICHOT	PMIC Internal Temperature Interrupt 0 = No interrupt pending 1 = PMIC Temperature Hot							

14.6 PMUINT Register Table

Address	0x05							
Field Name	**PMUINT [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	PMUVDC	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
PMUVDC	Power monitor unit VDC voltage interrupt 0 = No interrupt pending 1 = VDC voltage below threshold limit							

14.7 RESETIRQ1 Register Table

Address	0x08							
Field Name	RESETIRQ1 [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	VRFAULT	-	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VRFAULT	Power monitor unit VDC voltage interrupt 0 = VR fault has not forced an Emergency Reset 1 = VR fault has forced an Emergency Reset							

14.8 RESETIRQ2 Register Table

Address	0x09							
Field Name	RESETIRQ2 [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved						CRITTEMP	Reserved
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
CRITTEMP	0 = PMIC Critical Temperature not reached 1 = PMIC Critical Temperature reached, forcing Emergency Reset							

14.9 MPMUNIT Register Table

Address	0x0B							
Field Name	MPMUINT							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name						MPMUVDC		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	1	1	1
Bit Name	**Bit Definition**							
MPMUVDC	Power monitor unit VDC voltage interrupt mask 0 = Not Masked, 1 = Masked							

14.10 PWRSRCINT Register Table

Address	0x0C							
Field Name	MPWRSRCINT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	MPMICHOT	-	-	-
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	1	1	1	1
Bit Name	**Bit Definition**							
MPMICHOT	0 = Not Masked 1 = Masked							

14.11 SOFTSTART1 Register Table

Address	0x0D							
Field Name	SOFTSTART1 [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	V5ADS3SST		V33ADSWSST	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	0	1	0
Bit Name	**Bit Definition**							
V5ADS3SST[1:0]	V5A_DS3 soft-start time select. 2'b00 = 1.25ms 2'b01 = 10ms 2'b10 = 20ms 2'b11 = 40ms							
V33ADSWSST[1:0]	V33A_DSW soft-start time select. 2'b00 = 1.25ms 2'b01 = 10ms 2'b10 = 20ms 2'b11 = 40ms							

14.12 SOFTSTART2 Register Table

Address	0x0E							
Field Name	SOFTSTART2 [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-		V105ASST		V18ASST	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
V105ASST[1:0]	V105A soft-start time select. 2'b00 = 1.25ms 2'b01 = 5ms 2'b10 = 10ms 2'b11 = 20ms							

14.12 SOFTSTART2 Register Table (Cont.)

Address	0x0E
V18ASST[1:0]	V18A soft-start time select. 2'b00 = 1.25ms 2'b01 = 5ms 2'b10 = 10ms 2'b11 = 20ms

14.13 RESETIRQ1MASK Register Table

Address	0x11							
Field Name	RESETIRQ1MASK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	MVRFAULT	-	-	-	-
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	0	0	0	0
Bit Name	**Bit Definition**							
MVRFAULT	0 : VR fault IRQ unmasked 1 : VR fault IRQ masked							

14.14 RESETIRQ2MASK Register Table

Address	0x12							
Field Name	RESETIRQ2MASK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	MCRITTEMP	-
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	1	0
Bit Name	**Bit Definition**							
MCRITTEMP	0 = APW8856 Critical Temperature IRQ unmasked 1 = APW8856 Critical Temperature IRQ masked							

14.15 IRQLVL1MSK Register Table

Address	0x13							
Field Name	IRQLVL1MSK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MRESET	-	MPMU	-	-	MPWRSRC	-	-
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	1	0	1	1	0	1	1	1
Bit Name	**Bit Definition**							
MRESET	0 = Reset IRQ unmasked 1 = Reset IRQ masked							
MPMU	0 = PMU IRQ unmasked 1 = PMU IRQ masked							
MPWRSRC	0 = Power source unmasked 1 = Power source masked							

14.16 PWRSTAT1 Register Table

Address	0x16							
Field Name	PWRSTAT1							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	V5VA_ DS3_ FAULT	V3V3_ DSW_ FAULT	-	V18A_ FAULT	V18U_25U_ FAULT	VDDQ_ FAULT	VTT_ FAULT
Read/Writ	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
V5VA_DS3_FAULT	V5A_DS3 power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							
V3V3_DSW_FAULT	V33A_DSW power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							
V18A_FAULT	V18A power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							
V18U_25U_FAULT	V18U_25U power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							
VDDQ_FAULT	VDDQ power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							
VTT_FAULT	VTT power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							

14.17 PWRSTAT2 Register Table

Address	0x17							
Field Name	PWRSTAT2							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	V105A_ FAULT	-
Read/Writ	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
V105A_FAULT	V105A power fault indicator. 0 = VR functioning normally 1 = VR fault Cleared by host writing a 1 to this bit, writing 0 has no effect.							

14.18 PGMASK1 Register Table

Address	0x18							
Field Name	PGMASK1							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	MV105APG	MV18APG	-	MV5VADS3PG	MV3V3DSWPG	-
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
MV105APG	V105A_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							
MV18APG	V18A_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							
MV5VADS3PG	V5VA_DS3_PG power good Mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							
MV3V3DSWPG	V3V3_DSW_PG power good Mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							

14.19 PGMASK2 Register Table

Address	0x19							
Field Name	PGMASK2							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	V18U25UPG	MVDDQPG	-	-
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							

14.19 GMASK2 Register Table(Cont.)

Address	0x19
V18U25UPG	V18U_25U_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.
MVDDQPG	VDDQ_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.

14.20 V5VADS3CNT Register Table

Address	0x31							
Field Name	V5VADS3CNT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V5VADS3LVSEL [1:0]		V5VADS3VSEL [1:0]		AOACCNTV5VADS3 [1:0]		CTLV5VADS3 [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
V5VADS3LVSEL[1:0]	V5VA_DS3 low power mode output voltage set point.. 00 = disabled – voltage stays at value set by V5ADS3VSEL[1:0] bits. 01 = Vnominal - 4%(4.8V) 10 = Vnominal - 3%(4.85V) 11 = Vnominal - 2%(4.9V)							
V5VADS3VSEL[1:0]	V5VA_DS3 output voltage. 00 = Vnominal + 3%(5.15V) 01 = Vnominal + 2%(5.10V) 10 = Vnominal + 0%(5.0V) 11 = Vnominal - 2%(4.9V)							
AOACCNTV5VADS3[1:0]	V5VA_DS3 fast lower power mode exist field. 00 = fast-change mode disable. No effect on bit D[1:0] 01 = bits D[1:0] set to 01 at rising edge of SLP_S0_L 10 = bits D[1:0] set to 10 at rising edge of SLP_S0_L 11 = bits D[1:0] set to 11 at rising edge of SLP_S0_L							
CTLV5VADS3[1:0]	V5VA_DS3 VR operating mode control field. 00 = VR OFF 01 = PFM 10 = AUTO/ FORCED PWM 11 = FORCED PWM							

14.21 V3V3DSWCNT Register Table

Address	0x32							
Field Name	V3V3DSWCNT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V3V3DSWLVSEL [1:0]		V3V3DSWVSEL [1:0]		AOACCNTV3V3DSW [1:0]		CTLV3V3DSW [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
V3V3DSWLVSEL[1:0]	V3V3_DSW lower power mode output voltage set point. 00 = disabled – voltage stays at value set by V3V3DSWVSEL[1:0] bits. 01 = Vnom - 4% (3.168V) 10 = Vnom - 3% (3.201V) 11 = Vnom - 2% (3.234V)							
V3V3DSWVSEL[1:0]	V3V3_DSW nominal output voltage 00 = Vnom + 3% (3.399V) 01 = Vnom + 2% (3.366V) 10 = Vnom + 0% (3.3V) 11 = Vnom - 2% (3.234V)							
AOACCNTV3V3DSW[1:0]	V3V3_DSW VR fast low power mode exit field. 00: fast-change mode disable. No effect on bits D[1:0]. 01: bits D[1:0] set to 01 at rising edge of SLP_S0_L. 10: bits D[1:0] set to 10 at rising edge of SLP_S0_L. 11: bits D[1:0] set to 11 at rising edge of SLP_S0_L.							
CTLV3V3DSW[1:0]	V3V3_DSW VR operating mode control field. 00 = VR OFF 01 = PFM 10 = AUTO/FORCED PWM 11 = FORCED PWM							

14.22 V1V8ACNT Register Table

Address	0x34							
Field Name	V1V8ACNT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V18ALVSEL [1:0]		V18AVSEL [1:0]		AOACCNTV18A [1:0]		CTLV18A [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
V1V8ALVSEL [1:0]	V1V8A low power mode output voltage set point. 00 = disabled – voltage stays at value set by V18AVSEL [1:0] bits. 01 = Vnom - 4% (1.728) 10 = Vnom - 3% (1.746) 11 = Vnom - 2% (1.764)							
V1V8AVSEL [1:0]	V1V8A output voltage 00 = Vnom +3% (1.854) 01 = Vnom +2% (1.836) 10 = Vnom +0% (1.8V) 11 = Vnom -2% (1.764)							

14.22 V1V8ACNT Register Table(Cont.)

Address	0x34
Bit Name	**Bit Definition**
AOACCNTV1V8A [1:0]	V1V8A VR fast low power mode exist field 00 = fast-change mode disable. No effect on bits D[1:0]. 01 = bits D[1:0] set to 01 at rising edge of SLP_S0_L. 10 = bits D[1:0] set to 10 at rising edge of SLP_S0_L. 11 = bits D[1:0] set to 11 at rising edge of SLP_S0_L.
CTLV1V8A [1:0]	V1V8A VR operating mode control field 00 = VR OFF 01 = PFM 10 = AUTO/FORCED PWM 11 = FORCED PWM

14.23 V18U25UCNT Register Table

Address	0x35							
Field Name	**V18U25UCNT [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-		V18U25UVSEL [1:0]		AOACCNTV18U25U [1:0]		CTLV18U25U [1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
V18U25UVSEL[1:0]	V18U_25U output voltage. 00 = Vnom + 3% 01 = Vnom +2% 10 = Vnom +0% 11 = Vnom -2%							
AOACCNTV18U25U[1:0]	V18U_25U VR fast lower power mode exist field. 00 = fast-change mode disable. No effect on bit D[1:0]. 01 = bits D[1:0] set to 01 at rising edge of SLP_S0_L. 10 = bits D[1:0] set to 10 at rising edge of SLP_S0_L. 11 = bits D[1:0] set to 11 at rising edge of SLP_S0_L.							
CTLV18U25U[1:0]	V18U_25U VR operating mode control field. 00 = VR OFF 01 = ON 10 = ON 11 = ON							

14.24 VDDQCNT Register Table

Address	0x36							
Field Name	VDDQCNT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQLVSEL	VDDQVSEL[2:0]			AOACCNTVDDQ		CTLVDDQ	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	1	0	1	0
Bit Name	**Bit Definition**							
VDDQLVSEL	VDDQ low power mode output voltage set point. 0 = disabled – voltage stays at value set by VDDQVSEL[2:0] bits. 1 = Vnom - 3%							
VDDQVSEL[2:0]	VDDQ nominal output voltage 000 = Vnom +3% 001 = Vnom +2% 010 = Vnom +1% 011 = Vnom +0% (set by VDDQSEL pin) 100 = Vnom -1% 101 = Vnom -2% 110 = Vnom -3% 111 = Vnom -4%							
AOACCNTVDDQ[1:0]	VDDQ VR fast lower power mode exist field. 00: fast-change mode disable. No effect on bits D[1:0]. 01: bits D[1:0] set to 01 at rising edge of SLP_S0_L. 10: bits D[1:0] set to 10 at rising edge of SLP_S0_L. 11: bits D[1:0] set to 11 at rising edge of SLP_S0_L.							
CTLVDDQ[1:0]	VDDQ VR operating mode control field 00 = VR OFF 01 = PFM 10 = AUTO/FORCED PWM 11 = FORCED PWM							

14.25 V105ACNT Register Table

Address	0x37							
Field Name	V105ACNT [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V105ALVSEL[1:0]		V105AVSEL[1:0]		AOACCNTV105A[1:0]		CTLV105A[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	0	1	0
Bit Name	**Bit Definition**							
V105ALVSEL[1:0]	V105A low power mode output voltage set point. 00 = disabled – voltage stays at value set by the V105AVSEL[1:0] bits. 01 = 850mV 10 = 900mV 11 = 950mV							
V105AVSEL[1:0]	V105A output voltage 00 = Vnom (1.05V) 01 = Vnom -50mV (1.00V) 10 = Vnom -75mV (0.975V) 11 = Vnom -100mV (0.950V)							

14.25 V105ACNT Register Table (Cont.)

Address	0x37
Bit Name	**Bit Definition**
AOACCNTV105A[1:0]	V105A VR fast low power mode exit field. Changes the 00: fast-change mode disable. No effect on bits D[1:0]. 01: bits D[1:0] set to 01 at rising edge of SLP_S0_L. 10: bits D[1:0] set to 10 at rising edge of SLP_S0_L. 11: bits D[1:0] set to 11 at rising edge of SLP_S0_L.
CTLV105A[1:0]	V105A VR operating mode control field. 00 = VR OFF 01 = PFM 10 = AUTO/FORCED PWM 11 = FORCED PWM

14.26 VRMODECTRL Register Table

Address	0x3B							
Field Name	**VRMODECTRL [7:0]**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	V1V8A_ LPM	V3V3DSW_ LPM	-	-	VDDQ_ LPM	V105A_ LPM	V5VADS3_ LPM
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	1	1	1	1	1
Bit Name	**Bit Definition**							
V1V8A_LPM	0 = V1V8A enters Low Power mode when SLP_S0_L pin is in low logic state. 1 = V1V8A never enters Low Power mode.							
V3V3DSW_LPM	0 = V3V3_DSW enters Low Power mode when SLP_S0_L is in low logic state. 1 = V3V3_DSW never enters Low Power mode.							
VDDQ_LPM	0 = VDDQ enters Low Power mode when VTT_CNTL pin is in low logic state. 1 = VDDQ never enters Low Power mode.							
V105A_LPM	0 = V105A enters Low Power mode when SLP_S0_L is in low logic state. 1 = V105A never enters Low Power mode.							
V5VADS3_LPM	0 = V5VA_DS3 enters Low Power mode when SLP_S0_L is in low ligic state. 1 = V5VA_DS3 never enters Low Power mode.							
CTLV105A[1:0]	V105A VR operating mode control field. 00 = VR OFF 01 = PFM 10 = AUTO/FORCED PWM 11 = FORCED PWM							

14.27 DISCHGCNT2 Register Table

Address	0x3D							
Field Name	DISCHGCNT2							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V5VADS3DISCHG		V3V3DSWDISCHG				V1V8ADISCHG	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	1	0	1	0	1
Bit Name	**Bit Definition**							
V5VADS3DISCHG	V5VA_DS3 Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							
V3V3DSWDISCHG	V3V3_DSW Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							
V1V8ADISCHG	V1V8A Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							

14.28 DISCHGCNT3 Register Table

Address	0x3E							
Field Name	DISCHGCNT3							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V18U25UDISCHG		VDDQDISCHG		V105ADISCHG		-	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	1	0	1	0	1
Bit Name	**Bit Definition**							
V18U25UDISCHG	V18U_25U Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							
VDDQDISCHG	VDDQ Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							
V105ADISCHG	V105A Discharge Resistance 00 = function disabled (R > 1k) 01 = 20 Ω 10 = 20 Ω 11 = 20 Ω							

14.29 VREN Register Table

Address	0x41							
Field Name	VREN							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	EC_SLP_S4_L	EC_DS4
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
EC_SLP_S4_L	EC_SLP_S4# (known as SLP_S4_L on CRB) 0 = Disable 1 = Enable							
EC_DS4	0 = Disable 1 = Enable							

14.30 REGLOCK Register Table

Address	0x42							
Field Name	REGLOCK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	-	-	-	-	-	-	CNTLOCK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
CNTLOCK	V*CNT register Lock bit. Set and cleared by host. 0 = All V*CNT registers are unlocked. 1 = All V*CNT registers are locked NOTE: AOACCTLV* bits are copied to CTLV* bits when exiting connected standby (SLP_S0_L de-asserted) even when CNTLOCK is set(1).							

14.31 VRENPINMASK Register Table

Address	0x43							
Field Name	VRENPINMASK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	MV105AEN	MVDDQEN	MV18U25UEN	MV18AEN	-	MV5ADS3EN	-
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
MV105AEN	V105A Enable Pin Mask 0 = VR enable pin controls VR enable and disabling. 1 = VR enable pin masked; CTLV105A[1:0] bits in V105ACNT register control VR enable and disabling.							
MVDDQEN	VDDQ Enable Pin Mask 0 = VR enable pin controls VR enable and disabling. 1 = VR enable pin masked; CTLVDDQ[1:0] bits in VDDQCNT register control VR enable and disabling.							

14.31 VRENPINMASK Register Table (Cont.)

Address	0x43
Bit Name	**Bit Definition**
MV18U25UEN	V18U_25UA Enable Pin Mask 0 = VR enable pin controls VR enable and disabling. 1 = VR enable pin masked; CTLV18U25U[1:0] bits in V18U25UCNT register control VR enable and disabling.
MV18AEN	V18A Enable Pin Mask 0 = VR enable pin controls VR enable and disabling. 1 = VR enable pin masked; CTLV1V8A [1:0] bits in V1V8ACNT register control VR enable and disabling.
MV5ADS3EN	V5A_DS3 Enable Pin Mask 0 = VR enable pin controls VR enable and disabling. 1 = VR enable pin masked; CTLV5VADS3[1:0] bits in V5VADS3CNT register control VR enable and disabling.

14.32 SDWNCTRL Register Table

Address	0x49							
Field Name	**SDWNCTRL**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD							SDWN
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
SDWN	Master to force APW8856 to emergency shutdown 0 = No action performed 1 = force emergency shutdown If Master sets SDWN bit to 1 to force emergency shutdown, the PMIC needs to self-clear by writing a zero to the SDWN bit prior to the PMIC shutting down.							

14.33 0x54 Register Table

Address	0x54							
Field Name	**-**							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V3V3DSW_SST80MS	V5VADS3_SST80MS	VTT_TRACK_MODE	VLDO_OUT_SEL	PSEQ_SET[1:0]		SLAVEADDR[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
V3V3DSW_SST80MS	0: V3V3_DSW soft-start clock double disable (default) 1: V3V3_DSW soft-start clock double enable							
V5VADS3_SST80MS	0: V5VA_DS3 soft-start clock double disable (default) 1: V5VA_DS3 soft-start clock doubl enable							
VTT_TRACK_MODE	1'b0 : discharge non_tracking (default) 1'b1 : discharge trackin							
VLDO_OUT_SEL	0: VOUT = 2.8V (default) 1: VOUT = 1.05V							

14.33 0x54 Register Table (Cont.)

Address	0x54
Bit Name	**Bit Definition**
PSEQ_SET	2'b00: support DSX (default) 2'b01: support DS4/DS5 ,not supportDS3 2'b10: not support DS3/DS4/DS5 => internal SLP_SUS_L = 1 2'b11: support DSX
SLAVEADDR	2'b00: 7'h34 (default) 2'b01: 7'h32 2'b10: 7'h30 2'b11: reg0xE4[6:0] : I2C_SLAVE_ID[6:0]

14.34 0x55 Register Table

Address	0x55							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V3P3A_DSW_POK_BLK[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	1	0	1	0	1
Bit Name	**Bit Definition**							
V3P3A_DSW_POK_BLK[7:0]	default 11ms 0 : Disable , others V3P3A_DSW_POK BLANKING TIME = (V3P3A_DSW_POK_BLK[7:0] +1)*128 us							

14.35 0x56 Register Table

Address	0x56							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSM_RST#_POK_BLK[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	1	1	1	0	0
Bit Name	**Bit Definition**							
RSM_RST#_POK_BLK[7:0]	default 1ms 0 : Disable , others RSM_RST#_POK BLANKING TIME = (RSM_RST#_POK_BLK[7:0]+1) *8 us							

14.36 0x57 Register Table

Address	0x57							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQ_POK_BLK[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	0	0	0	0
Bit Name	**Bit Definition**							
VDDQ_POK_BLK[7:0]	(default 1ms) VDDQ_POK BLANKING TIME = VDDQ_POK_BLK[7:0] *32 us							

14.37 0x58 Register Table

Address	0x58							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VR_PG_BLK[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	0	0	1	1
Bit Name	**Bit Definition**							
VR_PG_BLK[7:0]	(default 20us) VR_PG BLANKING TIME = VR_PG_BLK[7:0]*1 us							

14.38 0x59 Register Table

Address	0x59							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V5VA_DS3_PG_V105A_DLY [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	0	0	0	1	1
Bit Name	**Bit Definition**							
V5VA_DS3_PG_V105A_DLY [7:0]	(default 100ms) 0 : Disable , others V5VA_DS3_PG to V105A EN DELAY TIME = (V5VA_DS3_PG_V105A_DLY[7:0]+1)*1 ms							

14.39 0x5A Register Table

Address	0x5A							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQ_PG_FALLING_V9_EN_DLY[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	1	0	1
Bit Name	**Bit Definition**							
VDDQ_PG_FALLING_V9_EN_DLY[7:0]	(default 45ms) 0 : Disable , others VDDQ_PG FALLING to V9 EN DELAY TIME = (VDDQ_PG_FALLING_V9_EN_DLY[7:0])*1 ms							

14.40 0x5B Register Table

Address	0x5B							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V18U_25U_PG_TO_VDDQ_EN_DLY[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	1	1	1	1
Bit Name	**Bit Definition**							
V18U_25U_PG_TO_VDDQ_EN_DLY[7:0]	(default 2ms) 0 : Disable , others V18U_25U_PG to VDDQ_EN DELAY TIME = (V18U_25U_PG_TO_VDDQ_EN_DLY[7:0]* +1)32us							

14.41 0x5C Register Table

Address	0x5C							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQSEL_DEB[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	1	1	1	0	1	0	1	0
Bit Name	**Bit Definition**							
VDDQSEL_DEB[7:0]	VDDQSEL_DEB[7:0] : (default 30 ms) VDDQSEL TO LOW DEBOUNCE TIME = VDDQSEL_DEB[7:0] *128 us							

14.42 0x5D Register Table

Address	0x5D							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQ_POK_VTTPOK_EN	MEM_STRAP_SEL	VDDQSST[1:0]		MVTTPG	VDISO_DISCHG_EN	VLDO_DISCHG_EN	VCCSTU_DISCHG_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	1	1
Bit Name	**Bit Definition**							
VDDQ_POK_VTTPOK_EN	0 = VDDQ_POK without VTT_POK. 1 = VDDQ_POK with VTT POK.							
MEM_STRAP_SEL	1'b0 : MEM_STRAP AT V3V3_DSW_POK (11ms delay after V3P3DSW PG) 1'b1 : MEM_STRAP AT V3V3_DSW PG (internal)							
VDDQSST	VDDQ soft-start time select. 2'b00 = 1.25ms 2'b01 = 5 ms 2'b10 = 10 ms 2'b11 = 20 ms							
MVTTPG	VTT_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							
VDISO_DISCHG_EN	VDISO Discharge Resistance 0 = function disabled (R > 1k) 1 = 20 Ω							
VLDO_DISCHG_EN	VLDO Discharge Resistance 0 = function disabled (R > 1k) 1 = 20 Ω							
VCCSTU_DISCHG_EN	VCCSTU Discharge Resistance 0 = function disabled (R > 1k) 1 = 20 Ω							

14.43 0x5E Register Table

Address	0x5E							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	V18U_25U_TDLY[1:0]		VDDQ_TDLY[1:0]		V5VADS3_TDLY[1:0]		V3V3DSW_TDLY[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
V3V3DSW_TDLY[1:0]	V3V3_DSW delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1ms 2'b11 = 2ms							
V5VADS3_TDLY[1:0]	V5VA_DS3 delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1ms 2'b11 = 2ms							

14.43 0x5E Register Table (Cont.)

Address	0x5E
Bit Name	**Bit Definition**
VDDQ_TDLY[1:0]	VDDQ delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1ms 2'b11 = 2ms
V18U_25U_TDLY[1:0]	V18U_25U delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1ms 2'b11 = 2ms

14.44 0x5F Register Table

Address	0x5F							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MDISO_SW_PG	MVCCSTUPG	VLDO_TDLY[1:0]		V105A_TDLY[1:0]		V1V8A_TDLY[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
V1V8A_TDLY[1:0]	V1V8A delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1 ms 2'b11 = 2 ms							
V105A_TDLY[1:0]	V105A delay time select. 2'b00 = 0ms 2'b01 = 0.5ms 2'b10 = 1 ms 2'b11 = 2 ms							
VLDO_TDLY[1:0]	VLDO delay time select. 2'b00 = 0ms 2'b01 = 5μs 2'b10 = 10μs 2'b11 = 20μs							
MVCCSTUPG	VCCSTU_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							
MDISO_SW_PG	DISO_SW_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.							

14.45 0x60 Register Table

Address	0x60							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	BAT_TYP	VLDO_VSEL[2:0]			SDWN_FLAG_SEL	VLDO_CNTL[2:0]		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	0	0	1	0
Bit Name	**Bit Definition**							
VLDO_CNTL[2:0]	3'b000: LDO controlled by SLP_S3_L pin 3'b001: LDO controlled by SLP_S4_L pin 3'b010: LDO controlled by SLP_S0_L & SLP_S3_L pin 3'b011: LDO controlled by SLP_S0_L & SLP_S4_L pin 3'b100: LDO on 3'b101: LDO off 3'b110: LDO controlled by SLP_S3_L pin 3'b111: LDO controlled by AND of SLP_S0_L & SLP_S3_L pins							
SDWN_FLAG_SEL	0: SDWN_FLAG LATCH 1: SDWN_FLAG NO LATCH							
VLDO_VSEL[2:0]	000 = Vnom +3% 001 = Vnom +2% 010 = Vnom +1% 011 = Vnom +0% 100 = Vnom -1% 101 = Vnom -2% 110 = Vnom -3% 111 = Vnom -4%							
BAT_TYP	0: BATTERY 3S 1: BATTERY 1S (V5A_DS3 OFF)							

14.46 0x61 Register Table

Address	0x61							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MVLDOPG	VCC_STU_CNTL[2:0]			VDISO_SW_SEL	VDISO_CNTL[2:0]		
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	0	1	0
Bit Name	**Bit Definition**							
VDISO_CNTL[2:0]	3'b000: VDISO SW controlled by SLP_S3_L pin 3'b001: VDISO SW controlled by SLP_S4_L pin 3'b010: VDISO SW controlled by SLP_S0_L & SLP_S3_L pin 3'b011: VDISO SW controlled by SLP_S0_L & SLP_S4_L pin 3'b100: VDISO SW on 3'b101: VDISO SW off 3'b110: VDISO SW controlled by SLP_S3_L pin 3'b111: VDISO SW controlled by AND of SLP_S0_L & SLP_S3_L pins							
VDISO_SW_SEL	VDISO_SW_SEL 0: VOUT = VINA (1.8V) 1: VOUT = VINB (3.3V)							

14.46 0x61 Register Table (Cont.)

Address	0x61
Bit Name	**Bit Definition**
VCC_STU_CNTL[2:0]	3'b000: VCCSTU SW controlled by SLP_S3_L pin 3'b001: VCCSTU SW controlled by SLP_S4_L pin 3'b010: VCCSTU SW controlled by SLP_S0_L & SLP_S3_L pin 3'b011: VCCSTU SW controlled by SLP_S0_L & SLP_S4_L pin 3'b100: VCCSTU SW on 3'b101: VCCSTU SW off 3'b110: VCCSTU SW controlled by SLP_S3_L pin 3'b111: VCCSTU SW controlled by AND of SLP_S0_L & SLP_S3_L pins
MVLDOPG	VLDO_PG power good mask. Set and cleared by host. 0 = power good functions as part of the power good tree. 1= power good is masked (disconnected) from the power good tree.

14.47 0x62 Protection Register Table

Address	0x62							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDQ_OV_FAULT	VDDQ_UV_FAULT	V105A_OV_FAULT	V105A_UV_FAULT	V3V3DSW_OV_FAULT	V3V3DSW_UV_FAULT	V5VADS3_OV_FAULT	V5VADS3_UV_FAULT
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VRX_FAULT	0 = Normal 1 = VRX_FAULT							

14.48 0x63 Protection Register Table

Address	0x63							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VCCSTU_FAULT	VDISO_SW_FAULT	VLDO_UV_FAULT	CRITTEMP_FAULT	V1V8U_2P5U_OC_UV_FAULT	ILLEGAL_FAULT	V1V8A_OV_FAULT	V1V8A_UV_FAULT
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VRX_FAULT	0 = Normal 1 = FAULT							

14.49 0x64 Register Table

Address	0x64							
Field Name	-							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VTT_POK	VDDQ_ POK	V1V8U_2P5U_ POK	V105A_ POK	V5VADS3_ POK	V1V8A_ POK	V3V3DSW_ POK	SDWN_ EVEN
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VRX_FAULT	0 = Normal 1 = VRX_FAULT							
SDWN_EVEN	0 = Normal 1 = SDWN_EVEN							

15. Function Description

15.1 VR Function Description

Soft-Start

All VRs are equipped soft-start function, when enable signal of each VR is activated, an internal soft start ramps the output voltage at a certain rate. This allows the output voltage to ramp up gradually, eliminating overshoot and excessive inrush current.

Over Voltage Protection (OVP) Of V1V8A

The over voltage protection circuitry monitors the feedback voltage of V1V8A to prevent the output from accidently exceeding the desired set point. Once the feedback voltage exceeds typically 130% of the set point voltage, the high/low side MOSFETs turn off and internal latch circuitry is activated. This insures protection of the load damage and circuit reset is only achieved either by internal reset via the I2C(write “1” to VRFAULT bit) or by pulling low VDDQ_SEL.

Over Current Protection (OCP) and Under Voltage Protection (UVP)

The output of V5VA_DS3, V3V3_DSW, V1V8A, VDDQ and V105A is protected against gradual over current or sudden short on its output. When inductor current peak value exceeds the set threshold an internal over-current protection is activated which turns off the high side and low side MOSFETs. Once the output voltage drops below a typical threshold of 70% of the output set point value, both high side and low side MOSFETs turn off and an internal latch circuit is initiated.
When any of OCP or UVP is activated, the IC will be latch off and VRFAULT will be issued. To clear VRFAULT is to write “1” to VRFAULT bit (=Reg0x08[4]) via the I2C or to pull low VDDQ_SEL below 0.3V.

Over Voltage Protection (OVP) and Under Voltage Protection (UVP) Of V5VA_DS3, V3V3_DSW, VDDQ and V105A

Once the output voltage drops below a typical threshold of 70% of set point value or the output voltage exceeds typically 130% of the set point voltage, the PWM signal will be latched low to turn off the converter and discharge the output voltage.
When any of UVP or OVP is activated, the VRFAULT bit will be set to “1”. The VRFAULT(=Reg0x08[4]) residues in RTC well. Writing “1” into VRFAULT bit will clear its value to “0” after the fault event has disappeared. Only when the VRFAULT is reset or VDDQ_SEL is toggled low(<0.3V) the IC can resume to normal operation.

Soft Stop

When V1V8A is shut down by I2C, both Upper and Lower MOSFETs will be turned off and an internal MOSFET with about 15 ohms (Typ.) Rds-on discharges the output via its FBP pin. The VTT and VLDO_OUT also discharge the output via the output pin in shutdown mode.
When V5VA_DS3, V3V3_DSW, VDDQ or V105A is shut down by I2C, the PWM signal pin will be low level and both high side and low side MOSFETs turn off while an internal 15ohm (Typ.) Rds-on resided at FBP pin turns on to discharge the output voltage.
All internal discharge resistors can be individually programmed via I2C not to be activated during shutdown mode.

Memory Type Support

In order to support different type of memory, ex., DDR3L or DDR4, the VDDQ, V18U_25U and VTT output voltage level will be changed in response to VDDQ_SEL voltage level. An external pull low resistor, RVDDQ_SEL, on VDDQ_SEL pin can set the VDDQ_SEL voltage level due to a 10μA current source flowing out of VDDQ_SEL. During power on after VSYS rises above 3.6V APW8856 keeps sampling VDDQ_SEL’s voltage to decide which VDDQ_SEL state is selected. The VDDQ_SEL state is hold the moment that V3V3_DSW_POK asserts. There are totally 5 states of selectable voltage conditions as below as well as if this pin is pulled below 0.3V threshold using an external small signal MOSFET. If any fault event occurs, it is suggested to pull VDDQ_SEL pin below 0.3V to clear internal IRQ registers.

15.1 VR Function Description (Cont.)

Table 4. VDDQ_SEL State

VDDQ_SEL State	Suggested R_{VDDQ_SEL}, ±1% tol.	V_{VDDQ}	V_{V18U_25U}	V_{VTT}	Usage
1	using an external MOSFET to pull low < 0.3V	off	off	off	Reset fault event
2	60.4kΩ	1.15V	off	off	3DXPoint
3	110kΩ	1.1V	1.8V	off	LPDDR4
4	165kΩ	1.2V	1.8V	0.6V	LPDDR3/DDR4RS/DDR4E
5	267kΩ	1.2V	2.5V	0.6V	DDR4
6	316kΩ	1.35V	off	0.675V	DDR3L

POK Output

There are 3 POK pins to indicate power good conditions: VDDQ_POK, V3V3_DSW_POK and RSM_RST#_POK. The 3 POK pins are open drain outputs that will switch high via an external pull up resistor. It can be pulled up to a maximum voltage of up to 5.5V. The POK assertion and de-assertion are controlled in the following conditions, as shown as below table.

Table 5. POK Assertion and De-assertion Conditions

POK State	Conditions	Power State	Comment
V3V3_DSW_POK	POK Assertion: [V3V3_DSW_POK & VSYSPOR]=1	Ready to enter S5 mode	V3V3_DSW_POK is asserted with 10ms (min.) delay
	POK De-assertion: [V3V3_DSW_POK & VSYSPOR]=0		
RSM_RST#_POK	POK Assertion: [V1V8A_POK & V5VA_DS3_POK & V105A_POK & SLP_SUS_L(Note4) & V3V3_DSW_POK]=1	All S5 power rails is ready	RSM_RST#_POK is asserted with 1ms (typ.) delay
	POK De-assertion: [V1V8A_POK & V5VA_DS3_POK & V105A_POK & SLP_SUS_L(Note4) & V3V3_DSW_POK]=0		
VDDQ_POK	POK Assertion: [VDDQ_POK & V18U_25U_POK & RSM_RST#_POK & SLP_S4_L]=1	Ready to enter S0 mode	
	POK De-assertion: [VDDQ_POK & V18U_25U_POK & RSM_RST#_POK & SLP_S4_L]=0		

Note4: SLP_SUS_L is excluded when DS5, DS4 and DS3 are not supported

15.1 VR Function Description (Cont.)

Interrupts And Their Masks

The APW8856 keeps monitoring any occurrence of fault event during normal operation and reports this fault to the embedded controller (EC) via the assertion of PMIN_INT_L pin. The RESET, PMU and PWRSRC are level 1 interrupts. Level 1 interrupts consist of level 2 interrupts, which are VRFAULT, CRITTEMP, PMUVDC and PMICHOT. The VRFAULT consists of level 3 interrupts, which are made of each VR's fault event (namely, UV, OV or OC). The level 1 and level 2 interrupt registers have their relative mask registers as shown as below diagram. These mask registers are activated by default. When a specific mask bit is written a "1" the relative interrupt will not cause PMIC_INT_L to assert during fault event. However, a masked interrupt event still can be investigated by reading its interrupt bit.

When a lower level interrupt occurs the relative higher level interrupt bit in the meantime is set to "1" by APW8856. Writing a "1" to an individual interrupt bit which is set by a fault event will make this interrupt bit to be cleared to "0". If the fault event still persists the APW8856 will keep conveying a "1" to the relative interrupt bit and consequently makes a writing a "1" to clear it in vain. If a higher level interrupt bit is cleared, the lower level one will be cleared too, simultaneously and automatically. However, writing a "1" to clear the lower level interrupts will not clear the higher level one. Please be noted writing a "0" to an interrupt bit will result in no change.

As indicated in the below diagram, there are some registers reside at the RTC well. When any one of these RTC-well bits is set by a fault event, cycling VSYS power on off will not clear it to "0" unless coin battery voltage has dropped into "dead" level which make the RTC-well bit not be able to be maintained. When VRFAULT or CRITTEMP has been issued, the APW8856 will shutdown and will be failed to be powered-on by cycling VSYS unless VRFAULT or CRITTEMP has been cleared. To achieve a successful VSYS powering-on after the issue of VRFAULT or CRITTEMP, please write a "1" or pull VDDQ_SEL pin below 0.3V to clear any single "1" in VRFAULT or CRITTEMP.

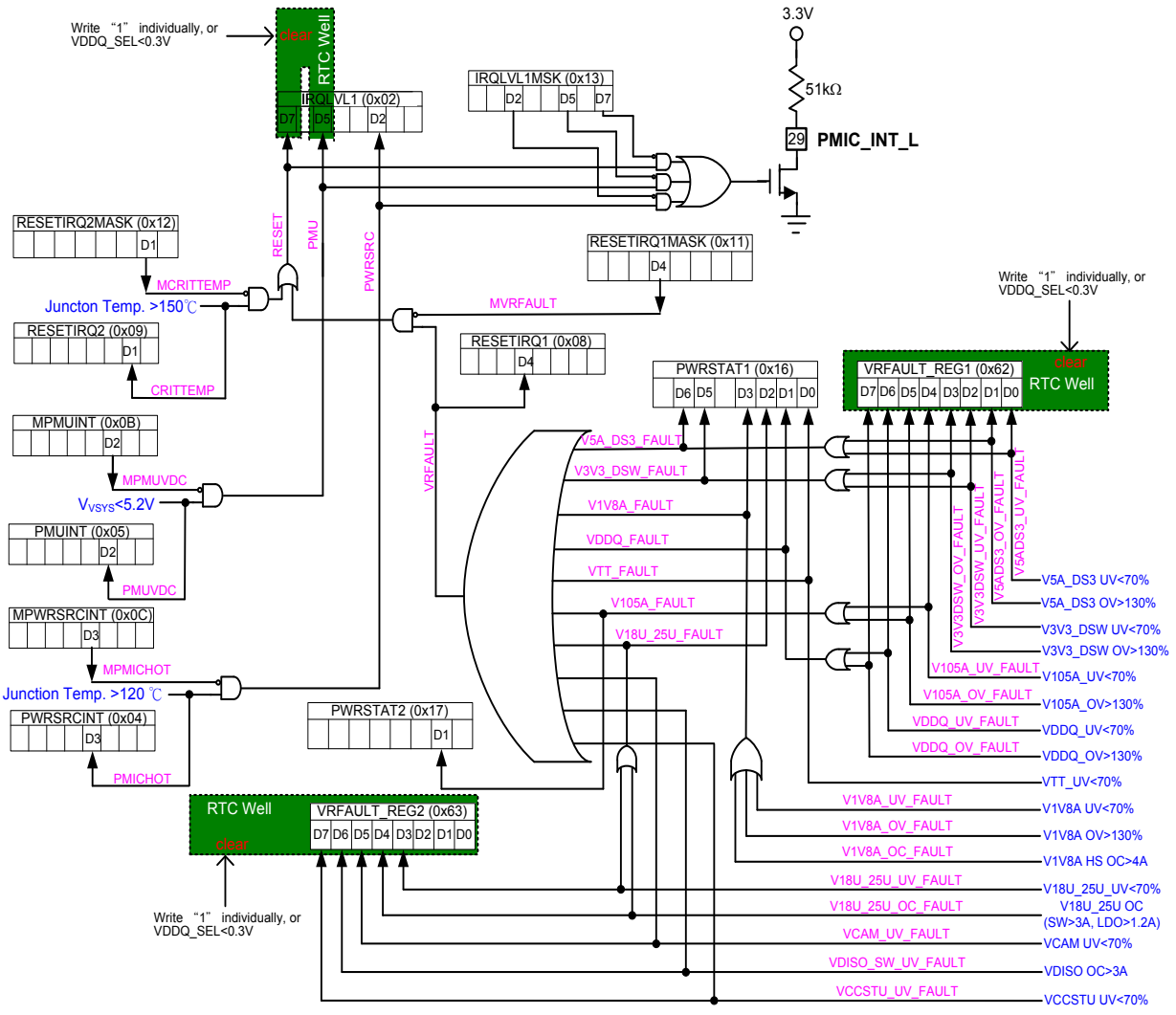


Figure 1. IRQ Architecture Block Diagram

15.1 VR Function Description (Cont.)

Truth Table of VDISO Voltage

The VDISO output voltage is either powered by switch A or switch B from two inputs, VDISO_IN3V3 or VDISO_IN1V8. The switches are made of N-MOSFETs whose gates are biased by an internal charge pump. Upon receiving control signals either switch A or switch B is turned on and transition between switch A and switch B is seamless. When the DISO output transits from off state to energized state by one of these two switches, the APL8856 controls the output voltage ramp up rate to reduce inrush current. The ramp up time is typically 300μs. Below table provides the truth table of switch A's and switch B's status versus control signals.

Table 6. VDISO Output Truth Table

EN	Reg0x61[3]	Switch A (input=VDISO_IN3V3)	Switch B (input=VDISO_IN1V8)	VDISO_OUT
Low	x	off	off	Discharge to ground
high	0	off	on	Conducted to VDISO_IN1V8
high	1	on	off	Conducted to VDISO_IN3V3

In the above table, the EN signal can be selected by register Reg0x61[2:0] as listed as below.

Table 7. VDISO EN Signal Selection

Reg0x61[2:0]	EN	Note
000	SLP_S3_L	
001	SLP_S4_L	
010	SLP_S0_L & SLP_S3_L	Default
011	SLP_S0_L & SLP_S4_L	
100	EN=high	
101	EN=low	
110	SLP_S3_L	
111	SLP_S0_L & SLP_S3_L	

15.2 I2C Function Description

I2C Overview

APW8856 is a slave-only device that is mastered by the SoC. It resides off the SoC's I2C. The slave device implemented on APW8856 side is an asynchronous implementation and will support the fast speed mode (1MHz). Some of the main features for the I2C slave are:

- APW8856 is accessed using a 7-bit addressing scheme.
- I2C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.
- The interface draws as minimum power when not actively reading/writing registers.
- Interface implementation is asynchronous.

Slave Address

APW8856 supports the standard I2C read and write functions. The configuration register space is divided to 59-byte partitions. APW8856 supports three 7-bit device addresses to access each of the 89 byte partitions. The 7-bit device address is "0110100" in default and changeable (in factory production line) to "0110000" or "0110010" as desired.

Table 8. I2C Slave Addresses

Reg0X54[1:0] value	7'bit Device Address
10	0110000
01	0110010
00	0110100 (default)

Protocol

Reads from PMIC registers follow the "combined protocol" as described in the I2C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different high-speed and fast-speed transaction format/protocol

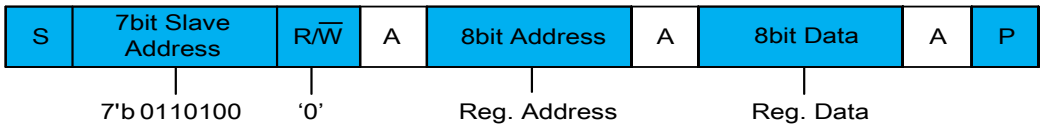


Figure2. I2C Fast Speed / Fast Speed Plus Single Byte Write

15.2 I2C Function Description (Cont.)

Protocol (Cont.)

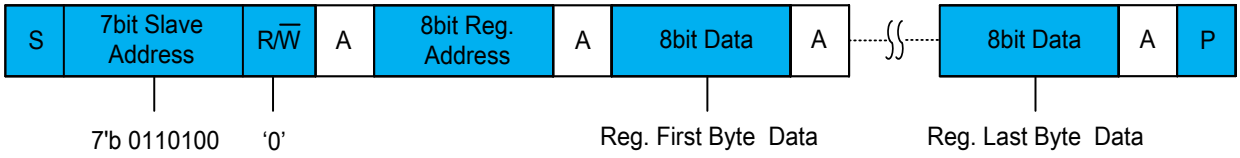


Figure3. I2C Fast Speed / Fast Speed Plus Multiple Byte Write

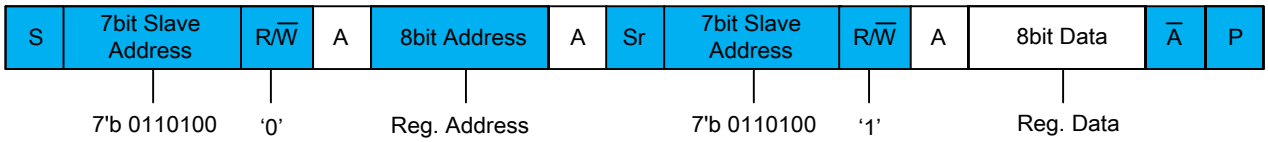


Figure4. I2C Fast Speed / Fast Speed Plus Single Byte Read

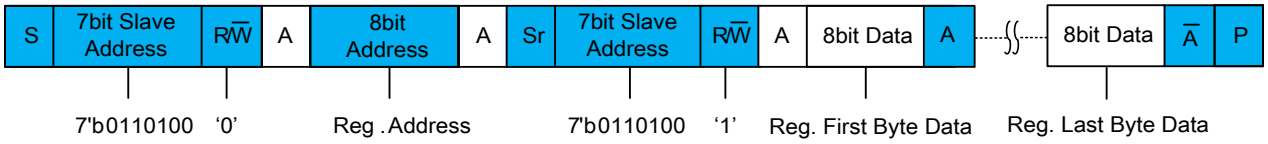


Figure5. I2C Fast Speed / Fast Speed Plus Multiple Byte Read

Master to Slave

Slave to Master

A = Acknowledge (SDA LOW)

$\overline{A}$ = Not Acknowledge (SDA HIGH)

S = START Condition

Sr = Repeated START Condition

P = STOP Condition

16. Application Information

Connected Standby Power Consumption

In order to help system designer to facilitate power design to meet Windows 8 and Windows 10 requirement in Connected Standby (CS) mode, the APW8856 is designed to minimize its quiescent current and optimizes the light load efficiency. Below table provides the actual data of the rails that are on in S3 and S5 mode and the total power loss associated with the system.

Rail Name	Voltage (V)	Output Current in CS mode (mA)	Power Loss (mW)
V5VA_DS3	5	1	0.814
V3V3_DSW	3.3	7	2.285
V1V8A	1.8	2	0.552
V18U_25U	1.8	4.5	0.005
VDDQ	1.2	8	2.708
V105A	1.05	16	4.2
VTT	0	0	0
VCC_RTC	3	0.006	0.0018
External VR Power Stage (4 set)	8.4	0.14	1.176
APW8856 IC	8.4	0.35	2.94
Total			**14.68**

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

For PWM converter, the inductor value (L) determines the sum of the inductor ripple currents, ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the switching frequency of the regulator, although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum

16. Application Information (Cont.)

Output Inductor Selection (cont.)

output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET. The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current.

Trace Layout Consideration for V3V3_FBP and V5V_FBP

Because one of the considerations of the APW8856 PMIC is to optimize package pin count and cost, these two feedback pins are designed not only to provide output voltage sensing for their respective regulators but also to provide input power for some internal circuitry. As a result the traces connecting the respective outputs to these pins must be designed such that it allows for at least 1A current for trace connecting the output of the 3.3V switching regulator to 3.3V FB pin and 100mA for 5V switching regulator back to the 5V FB pin.

V3V3_FBP PIN

Assuming that the total voltage drop will be less than 30mV with 1A current, this means that the trace resistance should be less than 30mΩ. Table x gives some guideline as to how to achieve this.

16. Application Information (Cont.)

5V_FBP

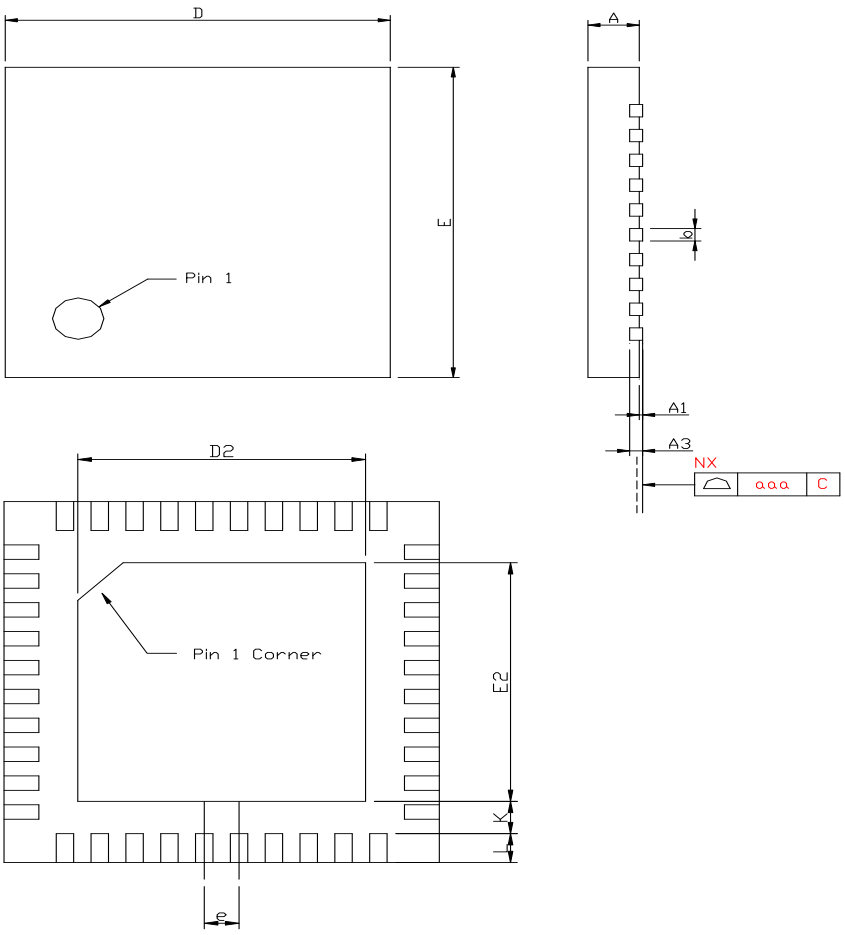
Assuming a 10mV drop at 100mA, this means that the trace resistance should be less than 10mΩ. Table x gives some guideline as to how to achieve this.

Layout Consideration

Signal Name	Description	Layout Guidelines
DGND	IC's analog ground.	Connect the GND pin to GND plane through several vias directly.
Each of VR's Input Pins (VSYS, V1V8A_IN...)	All VR's input voltage pins.	Place the input capacitors on each of the VR's input pins with low impedance to GND and low impedance to the each of VR's input pins.
Each of PWM VR's LX pins (V1V8A_LX…)	These are the connections to the mid point of the power stage consisting of the high- and low-side switch. The output inductor is connected here.	Connect to the output inductor with a short wire. For higher efficiency requirement, the inductor and LX pins should be as close as possible, and the trace resistance from LX pin to inductor should be less than 10mOhm is recommended. Ideally, route the high current path like LX pins to inductors and inductors to output capacitors on the top layer is recommended.
Each of PWM VR's output voltage feedback pins (V5VA_FBP, V3V3_FBP, V1V8A_FBP, V105A_FBP, VDDQ_FBP…)	Voltage feedback pin for each of VR.	The pins are high impedance and sensible to noise from the switch node. The positive feedback signal should be tied to the V+ pad of the output capacitor directly. The feedback pin could be routed to the input capacitor on the load side for remote sense. Coupling from fast switching signals must be avoided.
VSYS	APW8856 input supply voltage.	Connect the input capacitors from VSYS to GND for noise decoupling. The capacitors and VSYS pins should be as close as possible.
V5VA_PWM, V3V3_PWM, V105A_PWM, VDDQ_PWM	The gate driver outputs of V5VA_DS3, V3V3_DSW, V105A and VDDQ.	The traces of PWM signal from the gate driver output pins to the APW8703 should be short to eliminate the parasitical capacitance; the parasitical capacitance less than 80pF is recommended.
V3V3_FBP	Feedback pin of V3V3_DSW rail	This pin provides the feedback for the 3.3V PWM controller as well as supplying input power to the 3.3V LDO , the VCCSTG LDO as well as the V9 internal 2.5VLDO regulator. Connect this pin to the output of the 3.3V switching regulator via a trace capable of carrying at least 1A with less than 30mV drop.
V5VA_FBP	Feedback pin of V5VA_DS3 rail	This pin provides the feedback for the V5VA_DS3 PWM controller as well as supplying input power to the V5VA_LDO. Connect this pin to the power plane of V5VA_DS3 switching regulator via a trace capable of carrying at least 100mA with less than 10mV drop.
V1V8U_2V5U_OUT, VCCSTU_OUT, VLDO_OUT	LDO output without feedback pin	Since these outputs don't have their own dedicated feedback pin, the load regulation would be not good seen at load point if the PCB is not well laid-out. If the load regulation is concerned, place a wide PCB trace from these outputs to their load points to gain better load regulation..

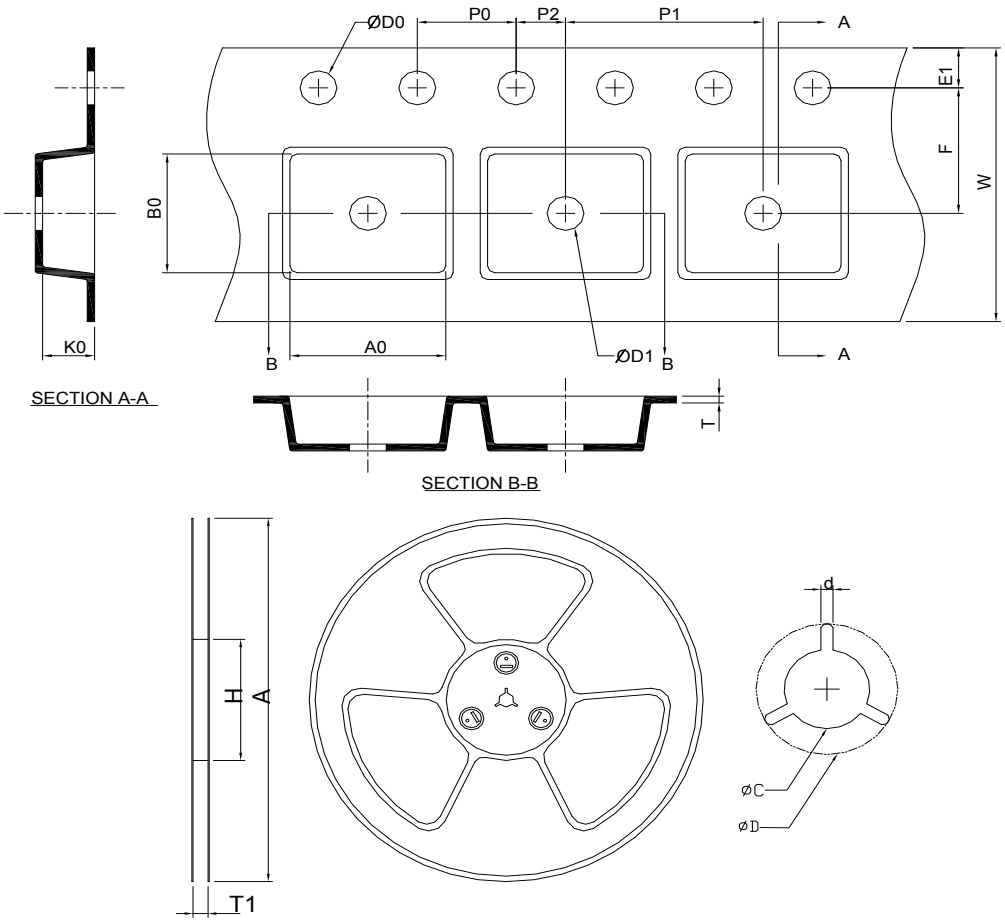
17. Package Information

TQFN5x5-40



SYMBOL	TQFN5*5-40			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.20	3.50	0.126	0.138
E	4.90	5.10	0.193	0.201
E2	3.20	3.50	0.126	0.138
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

18. Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

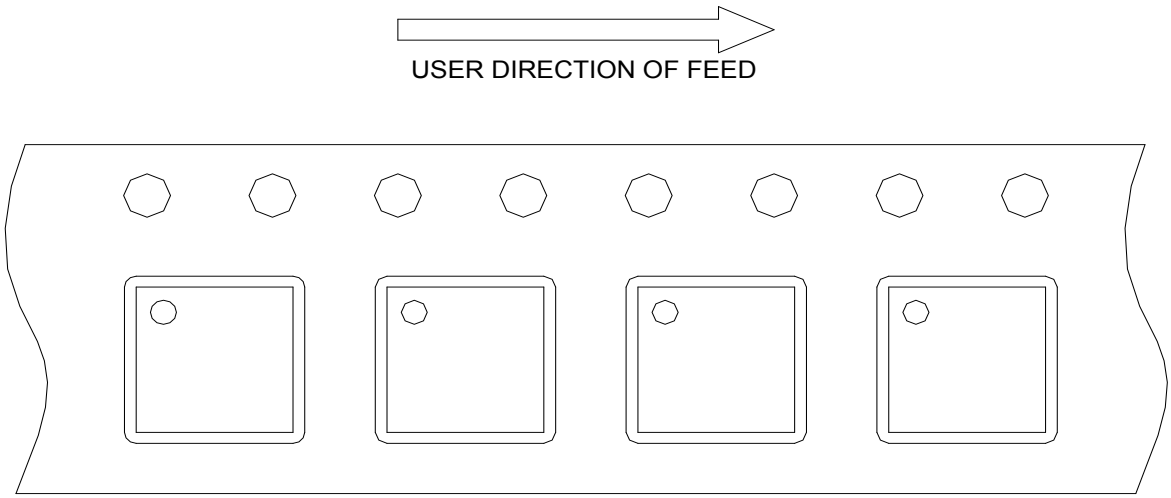
(mm)

19. Devices Per Unit

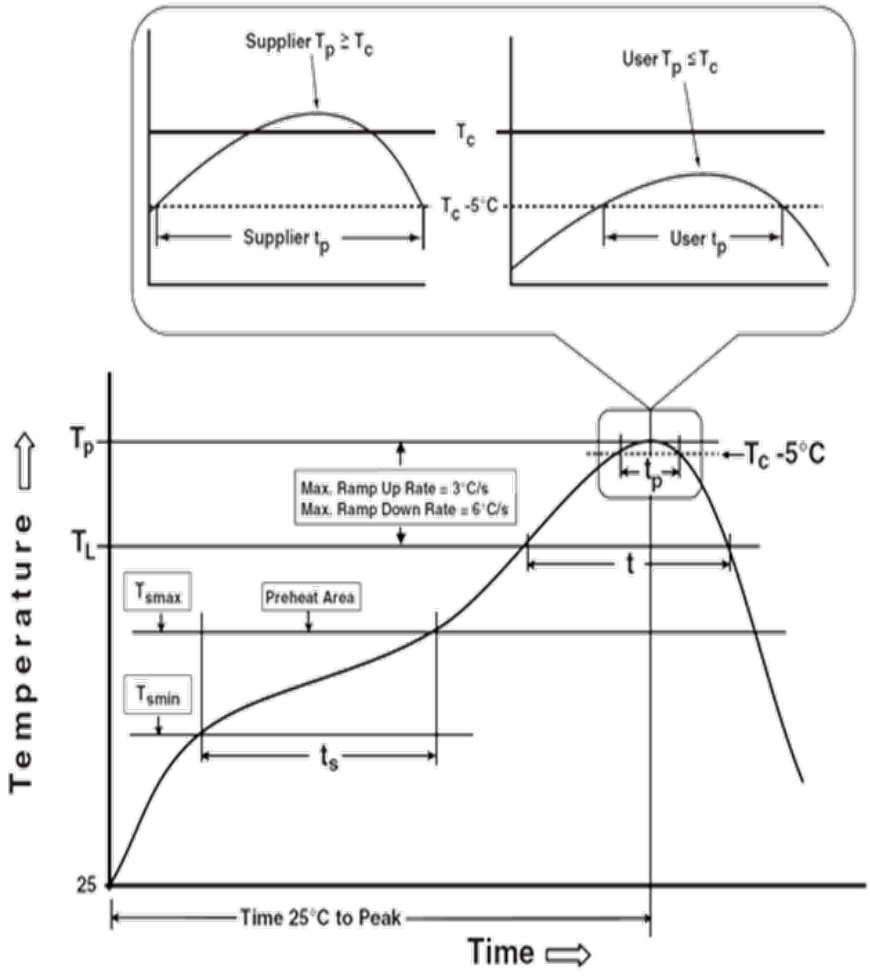
Package Type	Unit	Quantity
TQFN5x5	Tape & Reel	2500

20. Taping Direction Information

TQFN5x5-40



21. Classification Profile



22. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

23. Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≧ 2KV
MM	JESD-22, A115	VMM ≧ 200V
Latch-Up	JESD 78	10ms, 1_{tr} ≧ 100mA

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