High Current, High Frequency 8 Outputs Voltage Regulator and 1 Power Switch Power Management IC for High Performance Tablet and Ultra Notebook Applications

1.General Description

The APW8857 is a Power Management IC (PMIC) designed to provide 8 Voltage regulators and 1 Power Switch for AMD's Raven Ridge APU with ability to communicate via an I2C interface. The IC operates from a wide input voltage of 6V to 20V. There are 5 Switching Buck regulators 3 low power LDOs and 1 Power Switch that are all controlled and sequenced via the serial interface. The Buck PWM regulators consists of 3 switching controller driving external power stage such as APW8707/ APW8703/APW8706 which is capable of supplying up to 13A, 8A and 6A supply, 2 single phase switching regulators supplying up to 3A and 1A supply. The IC is equipped with all the standard protection features such as over current, over voltage and internal under voltage lock out protection. The serial interface is an I2C communication interface which allows supply sequencing as well as controlled supply ramp up and ramp down of all supplies except for the always on 1.5V LDO supplying to RTC load. The IC is offered in TQFN5x5-40 package.

2.Applications

- **High Performance Tablet PCs**
- **Ultra Notebook PCs**
- **Netbook PCs**
- **High Performance Digital Signage**
- **Medical Devices**
- **Smart phones**

3.Features

■ Voltage Rail

- **Provide 3 Buck PWM Controllers with High Accuracy over Temperature**
  - -VR1 provides 3.3V, 8A peak output current.
  - -VR2 provides 5V, 8A peak output current.
  - -VR3 provides 0.8V, 4A peak output current.
- **Provide 2 Buck PWM Converters with High Accuracy over Temperature**
  - -VR4 provides 1.8V, 3A peak output current.
  - -VR6 provides 0.8V, 1A peak output current
- **Provide 3 LDO and 1 Power Switch Outputs with High Accuracy over Temperature**
  - -VR5 combines a 1.2/1.5/1.8V, 0.25A LDO output with a power switch.
  - -VR7 provides a 3.3V LDO output.
  - -VR8 provides a low quiescent LDO output for RTC.
  - -One Power Switch with 2.5A output current.
  - -One 5V LDO output.
- **Built in Current limit, Over Voltage protection and Over temperature protection**

■ Serial Interface

- **I²C communication Interface for SoC Access**
- **Support Bit Rate 0.4MBit/s, 1MBit/s and 3.4MBit/s**
- **Power Sequence Control by GPIO_G3, EN_S0 and EN_S5 Pins.**
- **Built-in Thermal Diode and I²C Reading Function for Temperature Sensing.**
- **POK Signal for VR power state.**

■ Implement One Time Programmable (OTP) Function

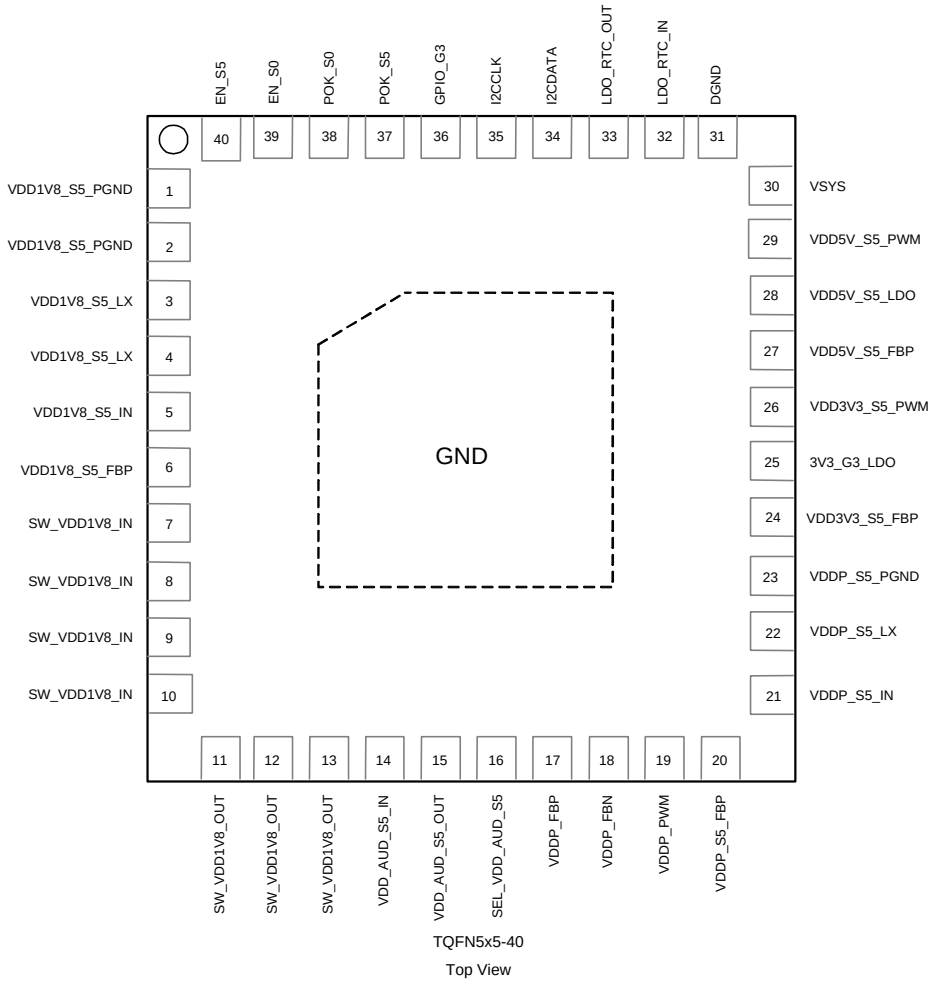
■ 5x5 TQFN-40 Package

4.Ordering and Marking Information

APW8857 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN5x5-40 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8857 QB: 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

5.Pin Configuration



TQFN5x5-40

Top View

6.Absolute Maximum Ratings (Note 1)

Pin or Symbol	Parameter	Rating	Unit
VSYS	VSYS to GND	-0.3~28	V
VDD1V8_S5_LX, VDDP_S5_LX VDD1V8_S5_IN, VDDP_S5_IN	VDD1V8_S5_LX to VDD1V8_S5_PGND VDDP_S5_LX to VDDP_S5_PGND VDD1V8_S5_IN to VDD1V8_S5_PGND VDDP_S5_IN to VDDP_S5_PGND	-0.3 to 6.5	V
VDD1V8_S5_PGND, VDDP_S5_PGND VDD_AUD_S5_PGND	PGND to GND	-0.3 to 0.3	V
All Other Pins	All Other Pins to GND	-0.3 to 6.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	30	°C/W

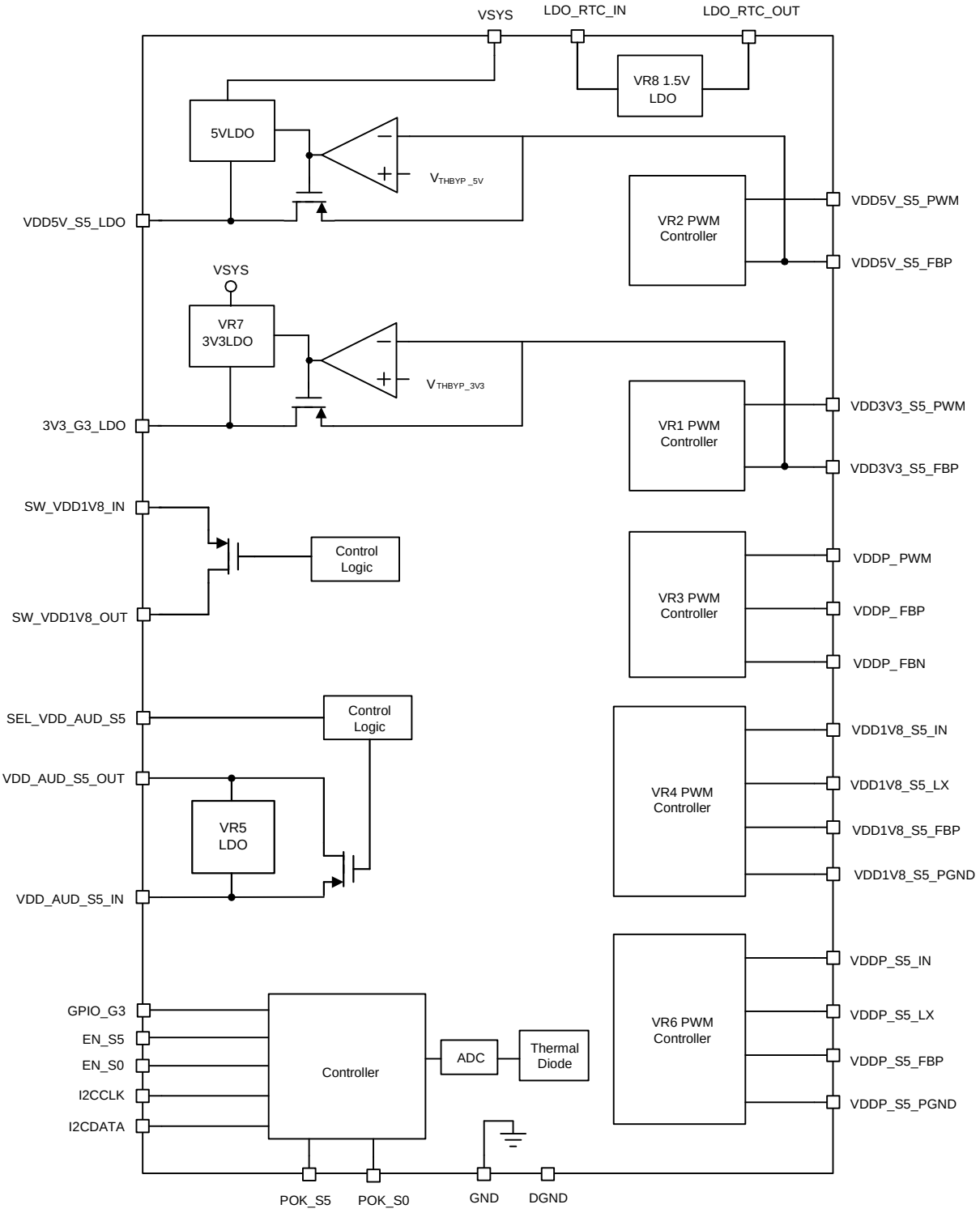
Note2: θ_{JA} is measured with the component mounted on a JESD-51-7 high effective thermal conductivity test board in free air.

8.Recommended Operating Conditions(Note3)

Symbol	Parameter	Range	Unit
V_{VSYS}	System Rail From Battery Management Unit	6 ~ 20	V
$V_{VDD1V8\_S5\_IN}$	VDD1V8_S5 Regulator Input Voltage	3 ~ 5.5	V
$V_{VDDP\_S5\_IN}$	VDDP_S5 Regulator Input Voltage	3 ~ 5.5	V
$V_{VDD\_AUD\_S5\_IN}$	VDD_AUD_S5 Regulator Input Voltage	1.8 ~ 5.5	V
$V_{SW\_VDD1V8\_IN}$	VDD1V8 Switch Input Voltage	1.8 ~ 5.5	V
$V_{LDO\_RTC\_IN}$	RTC Input Voltage	1.65 ~ 3.6	V
	EN_Sx, GPIO_G3 Input Low Voltage	0 ~ 0.6	V
	EN_Sx, GPIO_G3 Input High Voltage	1.2 ~ 5.5	V
$V_{POK\_Sx\_H}$	POK_Sx Pull High Voltage	~ 5.5	V
	I2CCLK, I2CDATA Pull High Voltage	1.8 ~ 3.3	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

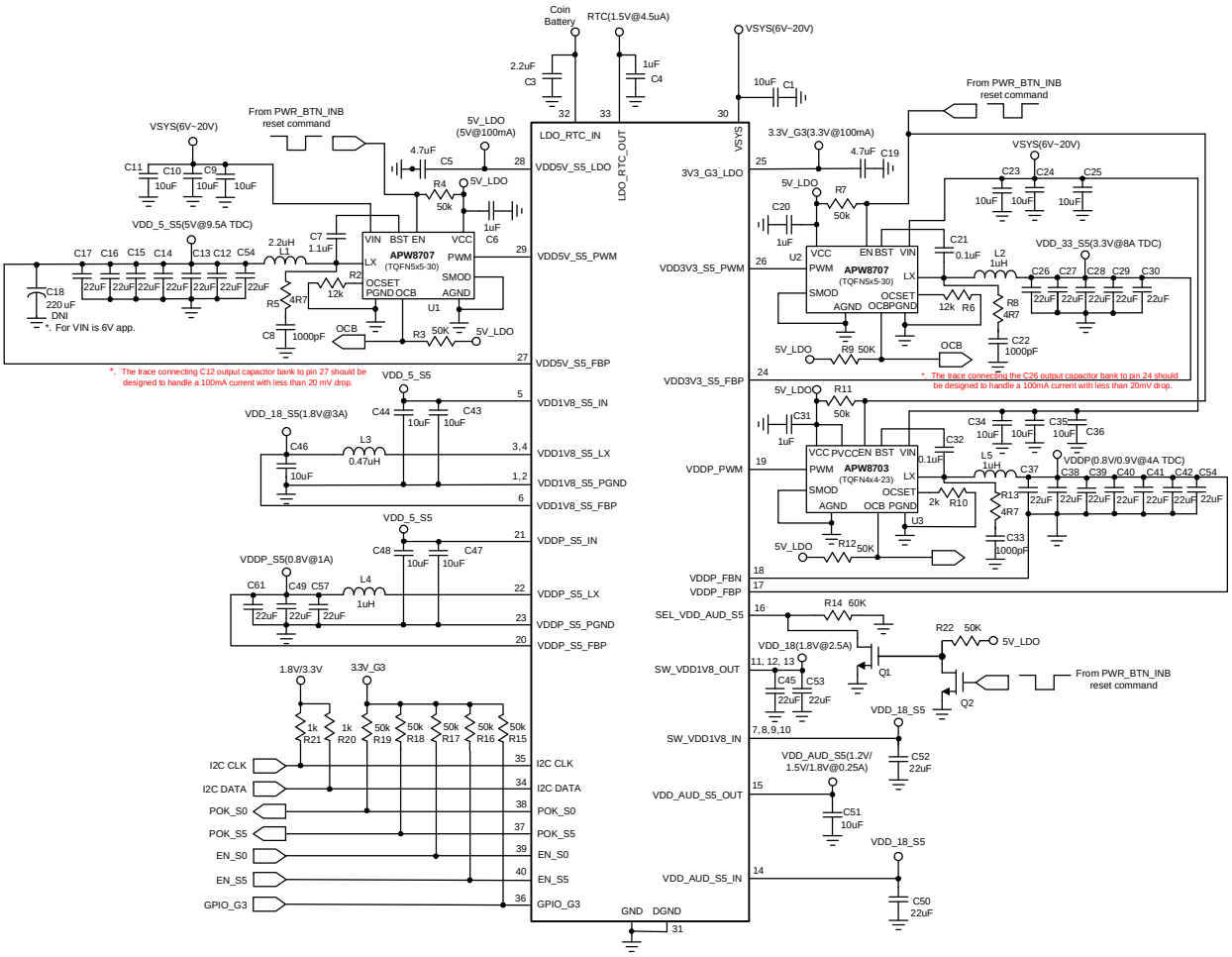
Note 3: Refer to the typical application circuit.

9.Block Diagram



10.Typical Application Circuit

10.1 Typical Application Circuit



10.2 Bill of Materials

Designator	Quantity	Value	Description	Size	Part Number	MFR
C12, C13, C14, C15, C16, C17, C54	7	22µF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM31CR61A226KE19#	Murata
C26, C27, C28, C29, C30, C37, C38, C39, C40, C41, C42, C50, C52, C53 C45, C49, C57,C61	22	22µF	Cap, Ceramic, 6.3V, X7R, 10%	1206	GRM31CR70J226KE19#	Murata
C1, C9, C10, C11, C23, C24, C25, C34, C35, C36	9	10µF	Cap, Ceramic, 35V, X5R, 10% ,	1206	GRM31CR6YA106KA12#	Murata
C43, C44, C47, C48	4	10µF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM319R61A106KE19#	Murata
C46, C51	4	10µF	Cap, Ceramic, 6.3V, X5R, 10%	1206	GRM319R60J106KE19#	Murata
C6, C20, C31	3	1µF	Cap, Ceramic, 10V, X5R, 10%	0805	GRM219R61A105KA01#	Murata
C7, C21, C32	3	0.1µF	Cap, Ceramic, 50V, X7R, 20%	0603	LLL185R71A104MA01#	Murata
C4	1	1µF	Cap, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J105KA01#	Murata
C5, C19	2	4.7µF	Cap, Ceramic, 10V, X5R, 10%	1206	GRM319R61A475KA01#	Murata
C3	1	2.2µF	Cap, Ceramic, 6.3V, X5R, 10%	0603	GRM185R60J225KE26#	Murata
C8, C22, C33	3	1000pF	Cap, Ceramic, 25V, X7R, 10%	0603	GRM188R71E102KA01#	Murata
C18	1	220µF	Cap, POSCAP, 10V, 20%	1812	10TPE220MIL	Panasonic
L1	1	2.2µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 12.7mΩ	6.36mm x 6.56mm x 3.1mm	XAL6030-222MEB	Coilcraft
L1	1	2.2µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 12mΩ	7.3mm x 6.6mm x 2.8mm	TMPC0603H-2R2MG-13M8-D	TAI-TECH
L2,	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 5.62mΩ	6.36mm x 6.56mm x 3.1mm	XAL6030-102MEB	Coilcraft
L2,	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 6.9mΩ	7.3mm x 6.6mm x 2.8mm	TMPC0603H-1R0MG-6M9-D	TAI-TECH
L3	1	0.47µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 14.07mΩ	4mm x 4mm x 1.2mm	XFL4012-471MEB	Coilcraft
L3	1	0.47µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 18mΩ	4.45mm x 4.06mm x 1.8mm	TMPC0412HP-R47MG-Z02	TAI-TECH

10.2 Bill of Materials

Designator	Quantity	Value	Description	Size	Part Number	MFR
L4	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 10.8mΩ	4mm x 4mm x 2.1mm	XFL4020-102MEB	Coilcraft
L4	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 22mΩ	4.45mm x 4.06mm x 1.8mm	TMPC0402HP-1R0MG-Z02	TAI-TECH
L5	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 13.25mΩ	4mm x 4mm x 2.1mm	XAL4020-102ME	Coilcraft
L5	1	1.0µH	Inductor, SMD Flat Wire Coils-SDB, shielding, 22mOhm	5.7mm x 5.2mm x 1.3mm	TMPC0515HP-1R0MG-D	TAI-TECH
R3, R4, R7, R9, R11, R12, R15, R16, R17, R18, R19	11	50kΩ	RES, 5%	0402		
R14	1	60kΩ	RES, 1%	0402		
R20, R21	2	1kΩ	RES, 5%	0402		
R5, R8, R13	3	4.7Ω	RES, 5%	0402		
R2, R6	1	12kΩ	RES, 5%	0402		
R10	1	2kΩ	RES, 5%	0402		
U1, U2	1	-	Power Stage	TQFN5x5-30	APW8707	ANPEC
U3	1	-	Power Stage	TQFN4x4-23	APW8703	ANPEC
U4	1	-	PMIC	TDFN5x5-40	APW8857	ANPEC
Q1,2	2	-	N-MOSFET	SOT-23	2N7002	

11.Pin Description

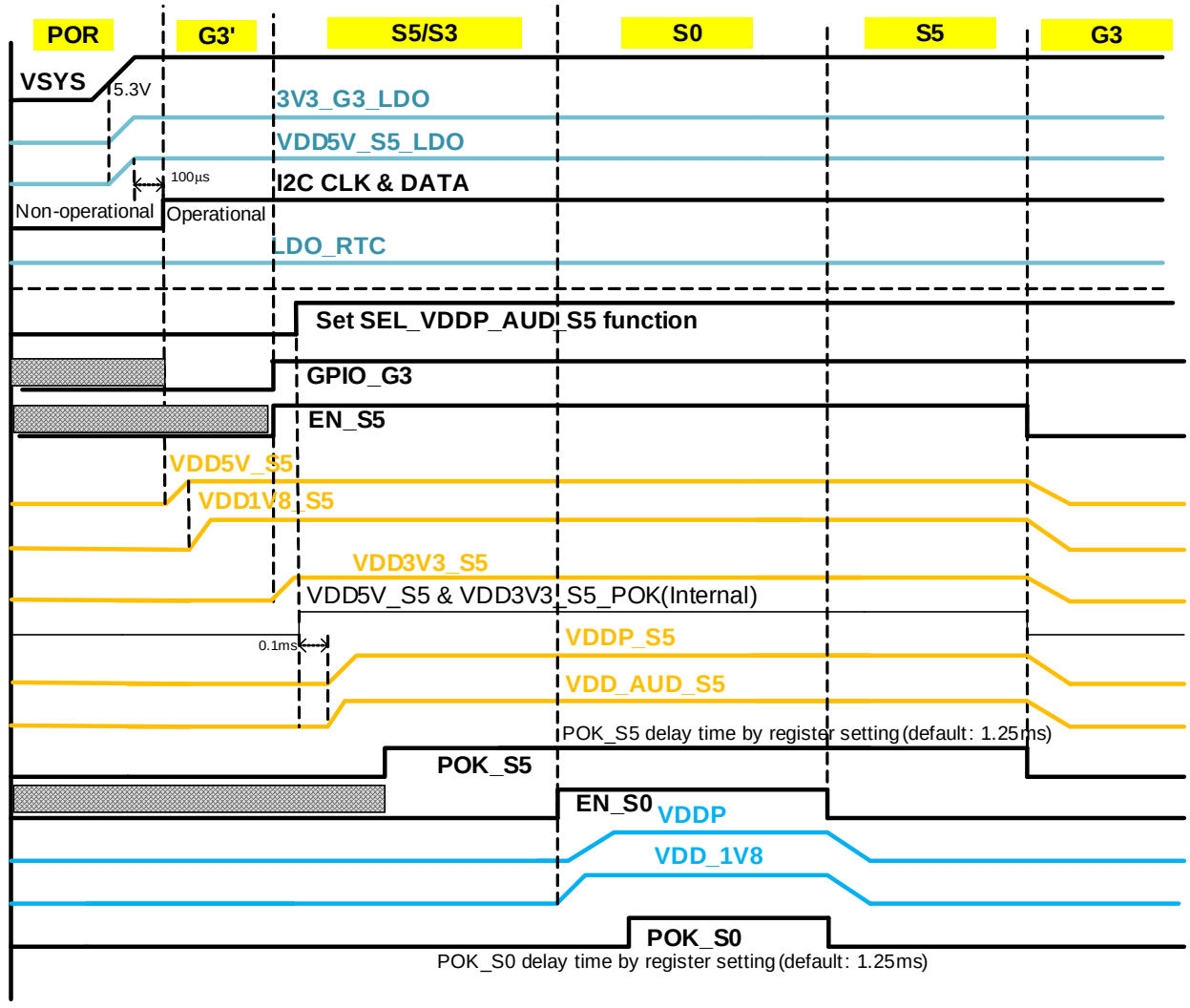
PIN		FUNCTION
NO.	NAME	
1	VDD1V8_S5_PGND	VDD1V8_S5 Power Ground Pin.
2	VDD1V8_S5_PGND	VDD1V8_S5 Power Ground Pin.
3	VDD1V8_S5_LX	VDD1V8_S5 PWM LX Output Pin. Connect to external inductor for output LC filter.
4	VDD1V8_S5_LX	VDD1V8_S5 PWM LX Output Pin. Connect to external inductor for output LC filter.
5	VDD1V8_S5_IN	VDD1V8_S5 Input Pin.
6	VDD1V8_S5_FBP	VDD1V8_S5 Output Voltage Feedback Pin. Connect to VDD1V8_S5 Output Voltage
7	SW_VDD1V8_IN	SW_VDD1V8 Switch Input Pin. Connect to VDD1V8_S5 Output Voltage.
8	SW_VDD1V8_IN	SW_VDD1V8 Switch Input Pin. Connect to VDD1V8_S5 Output Voltage.
9	SW_VDD1V8_IN	SW_VDD1V8 Switch Input Pin. Connect to VDD1V8_S5 Output Voltage.
10	SW_VDD1V8_IN	SW_VDD1V8 Switch Input Pin. Connect to VDD1V8_S5 Output Voltage.
11	SW_VDD1V8_OUT	SW_VDD1V8 Switch Output Pin.
12	SW_VDD1V8_OUT	SW_VDD1V8 Switch Output Pin.
13	SW_VDD1V8_OUT	SW_VDD1V8 Switch Output Pin.
14	VDD_AUD_S5_IN	VDD_AUD_S5 Input Pin. Connect to VDD1V8_S5 Output Voltage.
15	VDD_AUD_S5_OUT	VDD_AUD_S5 Output Pin.
16	SEL_VDD_AUD_S5	VDD_AUD_S5 Output Voltage Select Pin. Connect a resistor to ground to set the output voltage, and pull this pin to GND will reset the IC from fault state.
17	VDDP_FBP	VDDP Output Voltage Feedback Pin. Connect to VDDP Output Voltage
18	VDDP_FBN	VDDP Negative Output Feedback Pin. Connect to ground.
19	VDDP_PWM	VDDP PWM Signal Pin. Connect to External power stage's PWM input pin.
20	VDDP_S5_FBP	VDDP_S5 Output Voltage Feedback Pin. Connect to VDDP_S5 Output Voltage.
21	VDDP_S5_IN	VDDP_S5 Input Pin.
22	VDDP_S5_LX	VDDP_S5 LX Output Pin. Connect to external inductor for output LC filter.
23	VDDP_S5_PGND	VDDP_S5 Power Ground Pin.
24	VDD3V3_S5_FBP	VDD3V3_S5 Output Voltage Feedback Pin. Connect to VDD3V3_S5 Output Voltage.
25	3V3_G3_LDO	3.3V LDO Output Pin.
26	VDD3V3_S5_PWM	VDD3V3_S5 PWM Signal Pin. Connect to External power stage's PWM input pin.
27	VDD5V_S5_FBP	VDD5V_S5 Output Voltage Feedback Pin. Connect to VDD5V_S5 Output Voltage.
28	VDD5V_S5_LDO	5V LDO Output Pin.
29	VDD5V_S5_PWM	VDD5V_S5 PWM Signal Pin. Connect to External power stage's PWM input pin.
30	VSYS	IC Power Input Pin.
31	DGND	IC Digital Ground Pin.
32	LDO_RTC_IN	LDO_RTC Input Voltage Pin.
33	LDO_RTC_OUT	LDO_RTC Output Voltage Pin.
34	I2CDATA	I2C Data Connection Pin.
35	I2CCLK	I2C Clock Signal Pin.
36	GPIO_G3	System Power State Control Pin
37	POK_S5	Power Good Indicator. Connect a resistor from POK_S5 to a pull high voltage.
38	POK_S0	Power Good Indicator. Connect a resistor from POK_S0 to a pull high voltage.

11.Pin Description

PIN		FUNCTION
NO.	NAME	
39	EN_S0	System Power State Control Pin.
40	EN_S5	System Power State Control Pin.
Exposed Pad	GND	IC Analog Ground.

12.Power Sequence

12.1 G3' transfer to S5, and then S0

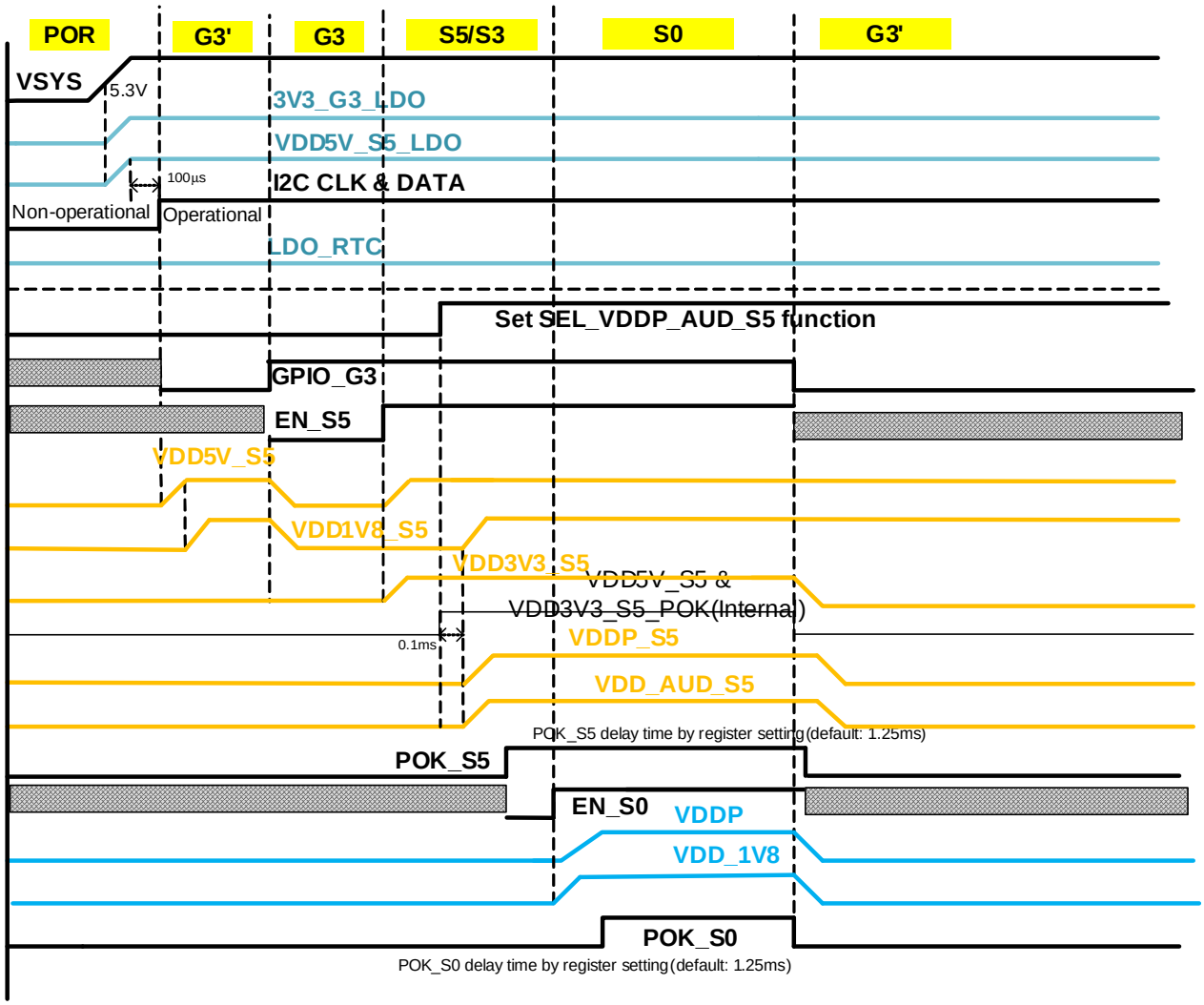


Ignore signal

Note 4: APW8857 enters SOC_G3 & SOC_G3' state will re-load OTP state

Note 5: VSYS rise faster than 4.5V/ms

12.2 G3' transfer to G3, and then S5, S0

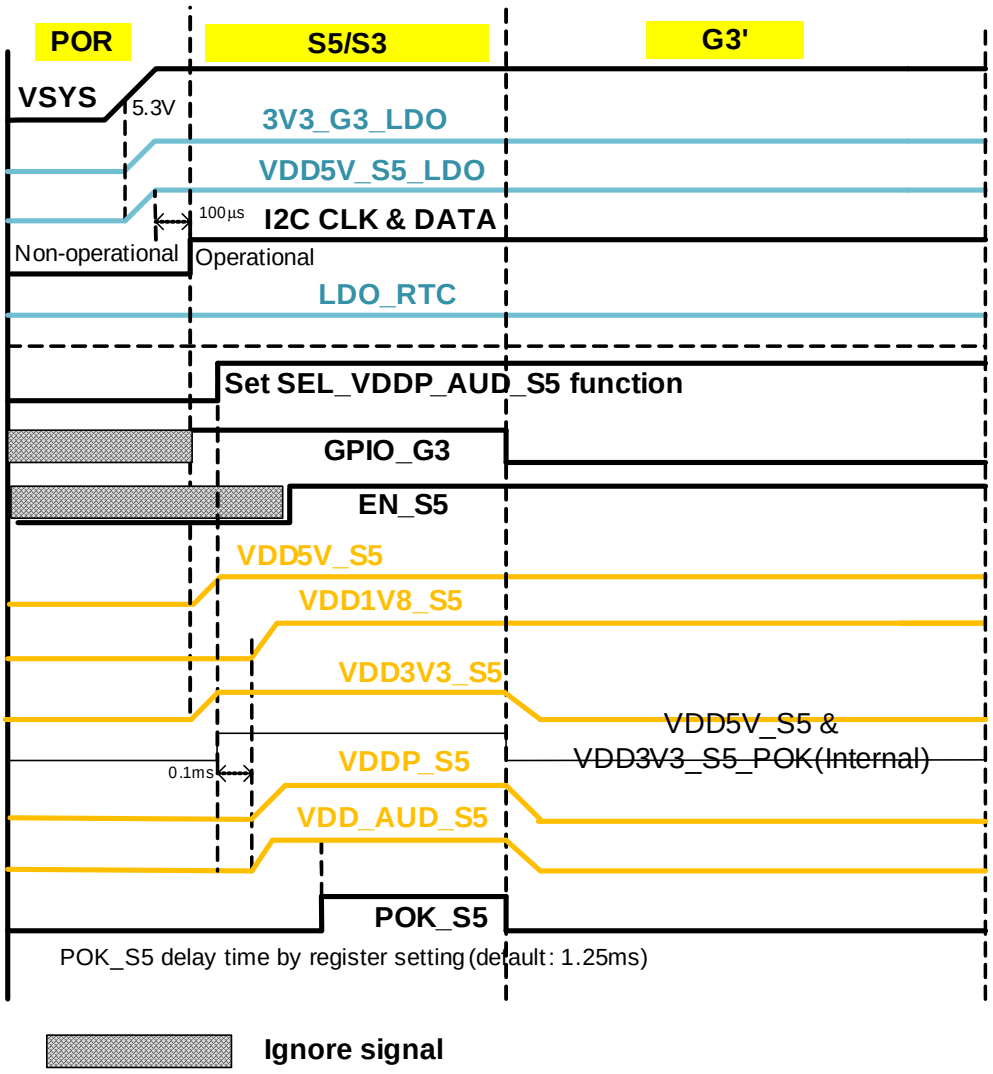


Ignore signal

Note 4: APW8857 enters SOC_G3 & SOC_G3' state will re-load OTP state

Note 5: VSYS rise faster than 4.5V/ms

12.3 System boot to S5



Note 4: APW8857 enters SOC_G3 & SOC_G3' state will re-load OTP state

Note 5: VSYS rise faster than 4.5V/ms

13.Electrical Characteristics

13.1 Regulator Table

Table 1. PWM Controllers VR1, VR2,VR3

Symbol	Parameter	VR1(VDD3V3_S5)	VR2(VDD5V_S5)	VR3(VDDP)	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	3.3	5.06	0.8	V
	Output Voltage Range	2.9~4	4.5~5.5	0.5~1.5	
I_{OUT}	Continuous Output Current	4	4	-	A
I_{PEAK}	Peak Output Current	8	8	4	A
F_{SW}	Switching Frequency (Default)	600	600	600	kHz
C_{IN}	Input Capacitor	3 x 10	3 x 10	3x 10	µF
C_{OUT}	Output Capacitor	5 x 22	7 x 22	7 x 22	µF
ESR	Output Capacitor ESR	6	6	6	mΩ
L	Output Inductor	1	2.2	1	µH
DCR	Output Inductor DCR	<10	<10	<10	mΩ

Table 2. PWM Converters VR4, VR6

Symbol	Parameter	VR4(VDD1V8_S5)	VR6(VDDP_S5)	Unit
V_{IN}	Input Voltage	V_{VDD5V_S5}	V_{VDD5V_S5}	V
V_{OUT}	Default Output Voltage	1.8	0.8	V
	Output Voltage Range	1.45~2.25	0.5~1.5	
I_{OUT}	Continuous Output Current	2.5	-	A
I_{PEAK}	Peak Output Current	3	1	A
F_{SW}	Switching Frequency (Default)	2000	1000	kHz
C_{IN}	Input Capacitor	2 x 10	2 x 10	µF
C_{OUT}	Output Capacitor	1 x 10	3 x 22	µF
ESR	Output Capacitor ESR	6	6	mΩ
L	Output Inductor	0.47	1	µH
DCR	Output Inductor DCR	<15	<15	mΩ

Table 3. LDO Regulators VR5, VR8 and SW_VDD1V8

Symbol	Parameter	VR8(LDO_RTC)	VR5(VDD_AUD_S5)	SW_VDD1V8	Unit
V_{IN}	Input Voltage	$V_{LDO\_RTC\_IN}$ (3.3V Battery or V_{VSYS})	V_{VDD1V8_S5}	V_{VDD1V8_S5}	V
V_{OUT}	Default Output Voltage	1.5	1.2	-	V
	Output Voltage Range	-	0.5 ~1.8	-	V
I_{OUT}	Continuous Output Current	4.5µ	0.25(LDO)/1A(Switch)	2.5	A
C_{IN}	Input Capacitor	2.2	22	2 x 22	µF
C_{OUT}	Output Capacitor	1	22	47	µF

13.1 Regulator Table

Table 4. LDO Regulators VDD5V_S5_LDO, VR7(3V3_G3_LDO)

Symbol	Parameter	VDD5V_S5_LDO	VR7(3V3_G3_LDO)	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	5.0	3.3	V
	Output Voltage Range	4.5~5.5	2.9~4	
I_{OUT}	Continuous Output Current	100	100	mA
C_{IN}	Input Capacitor	10	10	µF
C_{OUT}	Output Capacitor	4.7	4.7	µF

13.2 VR1 / VR7 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR1)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.6	%
	Output Voltage Line/Load Regulation	V_{IN}=7.5V to 20V, I_{OUT}=1mA to8A	-	-	±0.4	%
	Load Transient Drop Voltage	T_r=1µs, IOUT=2.4A to 8A, Refer to the typical circuit	-	-	-4	%
	Load Transient Overshoot Voltage	T_f=1µs, IOUT=8A to 2.4A, Refer to the typical circuit	-	-	+4	%
	Output Step Ramp Rate Accuracy	Default setting is 10mV/µs	-10	-	+10	%
	Output Voltage Soft-start Time	output from 10% to 90%, 1.25ms (Default setting)	1.125	1.25	1.375	ms
		output from 10% to 90%, 2.5ms	2.25	2.5	2.75	ms
		output from 10% to 90%, 5ms	4.5	5	5.5	ms
		output from 10% to 90%, 10ms	9	10	11	ms
	Output Discharge Resistance		-	10	-	Ω
	Feedback Input Current	$V_{VDD3V3\_S5\_FBP}$ = 2.9V	-	-	40	µA
PWM GATE DRIVER						
Fsw	Switching Frequency	Fsw=0.6MHz (Default setting)	540	600	660	kHz
	Minimum Off Time		-	200	-	ns
	Minimum Controllable On Time		-	100	130	ns
	PWM Sink Resistance		-	15	20	Ω
	PWM Source Resistance		-	15	20	Ω
	PWM Leakage Current	$V_{VDD3V3\_S5\_PWM}$=5.5V	-	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce TIme		-	2	-	µs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	V_{OUT}=3.3V, I_{OUT}=5mA/50mA (PFM Mode)	-	93	-	%
		V_{OUT}=3.3V, I_{OUT}=50mA/500mA	-	93	-	%
		V_{OUT}=3.3V, I_{OUT}=2A	-	93	-	%
		V_{OUT}=3.3V, I_{OUT}=8A	-	88	-	%

13.2 VR1 / VR7 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR1)			Unit
			Min	Typ	Max	
VR7 (3V3_G3_LDO)						
$V_{3V3\_G3\_LDO}$	LDO Regulator Output Voltage Accuracy	V_{VSYS}=6~20V, I_{OUT}=100mA	3.267	3.33	3.346	V
	LDO Dropout Voltage	I_{OUT}=100mA	-	-	0.4	V
	LDO Current Limit		150	200	300	mA
	LDO Discharge Resistance		-	10	-	Ω
	LDO Soft-start Time		-	100	-	µs
V_{THBYP_3V3}	Bypass Threshold	VR1 Rising	3.03	3.13	3.23	V
		Hysteresis	-	0.1	-	V
	Bypass Switch On Resistance		-	1.5	3	Ω

13.3 VR2 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 5.06V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR2)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.7	%
	Output Voltage Line/Load Regulation	V_{VSYS}=7.5V to 20V, I_{OUT}=1mA to 8A	-	-	±0.3	%
	Load Transient Drop Voltage	T_r=1µs, I_{OUT}=2.4A to 8A, Refer to the typical circuit	-	-	-4	%
	Load Transient Overshoot Voltage	T_f=1µs, I_{OUT}=8A to 2.4A, Refer to the typical circuit	-	-	+4	%
	Output Step Ramp Rate Accuracy	Default setting is 10mV/µs	-10	-	+10	%
	Output Voltage Soft-start Time	output from 10% to 90%, 1.25ms (Default setting)	1.125	1.25	1.375	ms
		output from 10% to 90%, 2.5ms	2.25	2.5	2.75	ms
		output from 10% to 90%, 5ms	4.5	5	5.5	ms
		output from 10% to 90%, 10ms	9	10	11	ms
	Output Discharge Resistance		-	10	-	Ω
	Feedback Input Current	$V_{VDD5V\_S5\_FBP}$ = 4V	-	-	50	µA
PWM GATE DRIVER						
	Switching Frequency	Fsw=0.6MHz (Default setting)	540	600	660	kHz
	Switching Frequency	V_{VSYS} =6V, V_{OUT}= 5.06V	-	-	300	kHz
	Minimum Off Time		-	200	-	ns
	Minimum Controllable On Time		-	100	130	ns
	PWM Sink Resistance		-	15	20	Ω
	PWM Source Resistance		-	15	20	Ω
	PWM Leakage Current	$V_{VDD5V\_S5\_PWM}$=5.5V	-	-	100	nA

13.3 VR2 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 5.06V, TA = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR2)			Unit
			Min	Typ	Max	
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce TIme		-	2	-	µs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	V_{OUT}=5.06V, IOUT=5mA/50mA(PFM Mode)	-	93	-	%
		V_{OUT}=5.06V, IOUT=50mA/500mA	-	93	-	%
		V_{OUT}=5.06V, IOUT=2A	-	92	-	%
		V_{OUT}=5.06V, IOUT=8A	-	90	-	%
LDO REGULATOR						
$V_{5V\_LDO\_POR}$	LDO Regulator Under-voltage Lockout (UVLO)	$V_{VDD5V\_S5\_LDO}$ Rising, enable other VRs	4.2	4.3	4.4	V
		Hysteresis	-	0.2	-	V
$V_{VDD5V\_S5\_LDO}$	LDO Regulator Output Voltage Accuracy	V_{VSYS} =6~20V, V_{V5VA_FBP}=0V, I_{OUT}=100mA	4.96	5.06	5.16	V
	LDO Dropout Voltage	I_{OUT}=100mA, V_{VDD5V_S5} =5.06V	-	-	0.4	V
	LDO Current Limit		150	200	300	mA
	LDO Discharge Resistance			10		Ω
V_{THBYP_5V}	Bypass Threshold	PWM Voltage Rising	4.55	4.7	4.85	V
		Hysteresis	-	0.15	-	V
	Bypass Switch On Resistance		-	1.5	3	Ω
	LDO Soft-start Time	C_{OUT}=4.7µF	-	100	-	µs

13.4 VR3 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 0.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR3)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.8	%
	Output Voltage Line/Load Regulation		-	-	±0.2	%
	Load Transient Drop Voltage	T_r=1µs, I_{OUT}=1.2A to 4A, Refer to the typical circuit	-	-	-4	%
	Load Transient Overshoot Voltage	T_f=1µs, I_{OUT}=4A to 1.2A, Refer to the typical circuit	-	-	+4	%
	Output Step Ramp Rate Accuracy	Default setting is 10mV/µs	-10	-	+10	%
	Output Voltage Soft-start Time	output from 10% to 90%, 1.25ms (Default setting)	1.125	1.25	1.375	ms
		output from 10% to 90%, 2.5ms	2.25	2.5	2.75	ms
		output from 10% to 90%, 5ms	4.5	5	5.5	ms
		output from 10% to 90%, 10ms	9	10	11	ms
	Output Discharge Resistance		-	10	-	Ω
	Feedback Input Current	V_{VDDP_FBP} =110%*V_{OUT}	-	-	20	µA
PWM GATE DRIVER						
	Switching Frequency	Fsw=0.6MHz (Default setting)	540	600	660	kHz
	Minimum Off Time		-	200	-	ns
	Minimum Controllable On Time		-	100	130	ns
	PWM Sink Resistance		-	15	20	Ω
	PWM Source Resistance		-	15	20	Ω
	PWM Leakage Current	V_{VDDP_PWM}=5.5V	-	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce TIme		-	2	-	µs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	V_{OUT}=0.8V, IOUT=50mA/100mA (PFM Mode)	-	80	-	%
		V_{OUT}=0.8V, IOUT=3A	-	81	-	%
		V_{OUT}=0.8V, IOUT=4A	-	80	-	%
		V_{OUT}=0.9V, IOUT=4A	-	80	-	%

13.5 VR4 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR4)			Unit
			Min	Typ	Max	
PWM CONVERTER						
	Switching Frequency Accuracy	V_{IN} =5V, Fsw=2MHz (Default setting)	1.8	2	2.2	MHz
	Maximum Duty Cycle		100	-	-	%
	Minimum Controllable On Time		-	60	80	ns
	High-side MOSFET On Resistance	$V_{VDD1V8\_S5\_IN}$=5V	-	55	-	mΩ
	Low-side MOSFET On Resistance	$V_{VDD1V8\_S5\_IN}$=5V	-	40	-	mΩ
	LX Leakage Current	$V_{VDD1V8\_S5\_LX}$ =5.5V, $V_{VDD1V8\_S5\_IN}$=5.5V	-	-	1	µA
	Zero Current Offset		-5	-	5	mV
PWM OUTPUT VOLTEGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.5	%
	Output Voltage Load Regulation		-	-	±0.5	%
	Load Transient Drop Voltage	T_f=1µs, I_{OUT}=0.9A to 3A, Refer to the typical circuit	-	-	-4	%
	Load Transient Overshoot Voltage	T_f=1µs, I_{OUT}=3A to 0.9A, Refer to the typical circuit	-	-	+4	%
	Output Step Ramp Rate Accuracy	Default setting is 10mV/µs	-10	-	+10	%
	Output Voltage Soft-start Time	output from 10% to 90%, 1.25ms (Default setting)	1.125	1.25	1.375	ms
		output from 10% to 90%, 2.5ms	2.25	2.5	2.75	ms
		output from 10% to 90%, 5ms	4.5	5	5.5	ms
		output from 10% to 90%, 10ms	9	10	11	ms
	Output Discharge Resistance		-	40	-	Ω
	Feedback Input Current	$V_{VDD1V8\_S5\_FBP}$ =110%*V_{OUT}	-	-	30	µA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce TIme		-	2	-	µs
	High-side MOSFET Over-current-Protection(OCP)		4	4.5	5	A
	OCP Debounce TIme		-	2	-	µs
	Thermal Shutdown Protection	T_J Rising	-	150	-	°C
		Hysteresis	-	20	-	

13.5 VR4 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 1.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR4)			Unit
			Min	Typ	Max	
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	V_{OUT}=1.8V, IOUT=50mA/100mA(PFM Mode)	-	87	-	%
		V_{OUT}=1.8V, IOUT=1.5A/3A	-	85	-	%

13.6 VR5 Electrical Characteristics

These specifications apply over V_{VDD5V_S5} = 5.06V, $V_{VDD\_AUD\_S5}$ = 1.2V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR5)			Unit
			Min	Typ	Max	
REGULATOR OUTPUT						
	Output Voltage Accuracy	T_A = 25°C	-	-	±1	%
	Output Voltage Load Regulation	IOUT=0.06A to 0.25A	-	-	±0.5	%
	Output Load Transient Drop Voltage	T_r=1µs, IOUT=0.06A to 0.25A, Refer to the typical circuit	-	-	-3.5	%
	Output Load Transient Overshoot Voltage	T_f=1µs, IOUT=0.25A to 0.06A, Refer to the typical circuit	-	-	+3.5	%
	Dropout Voltage	I_{OUT}=250mA	-	210	230	mV
	Output Discharge Resistance		-	40	-	Ω
	Output Noise	f=100 to 100kHz	-	100	-	μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	40	-	-	dB
	Current Limit		300	400	500	mA
	Under Voltage Protection (UVP)		65	70	75	%
	Output Voltage Soft-start Rate		1	1.25	1.5	ms
SWITCH OUTPUT						
	Switch On Resistance		-	50	60	mΩ
	Over Current-Protection		1	1.5	-	A
	Input Leakage Current	V_{EN_S0}=V_{EN_S5}=0V, $V_{VDD\_AUD\_S5\_IN}$=5V	-	-	1	µA
OUTPUT VOLTAGE CONTROL						
	SEL_VDDAUD_S5 Source Current		-	10	-	µA

13.7 VR6 Electrical Characteristics

These specifications apply over V_{VSYS} = 11.1V, V_{OUT} = 0.8V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR6)			Unit
			Min	Typ	Max	
PWM CONVERTER						
	Switching Frequency Accuracy	V_{IN} =5V, Fsw=1MHz (Default setting)	0.9	1	1.1	MHz
	Maximum Duty Cycle		70	80	90	%
	Minimum Controllable On Time		-	70	-	ns
	High-side MOSFET On Resistance	$V_{VDDP\_S5\_IN}$=5V	-	55	-	mΩ
	Low-side MOSFET On Resistance	$V_{VDDP\_S5\_IN}$=5V	-	40	-	mΩ
	LX Leakage Current	$V_{VDDP\_S5\_LX}$ =5.5V, $V_{VDDP\_S5\_IN}$=5.5V	-	-	1	µA
	Zero Current Offset		-5	-	5	mV
PWM OUTPUT VOLTEGE						
	Output Voltage Accuracy	T_A = 25°C	-	-	±0.8	%
	Output Voltage Load Regulation		-	-	±0.2	%
	Load Transient Drop Voltage	T_r=1µs, I_{OUT}=0.2A to 1A, Refer to the typical circuit	-	-	15	mV
	Load Transient Overshoot Voltage	Tf=1µs, IOUT=1A to 0.2A, Refer to the typical circuit	-	-	15	mV
	Output Step Ramp Rate Accuracy		-10	-	+10	%
	Output Voltage Soft-start Time	output from 10% to 90%, 1.25ms (Default setting)	1.125	1.25	1.375	ms
		output from 10% to 90%, 2.5ms	2.25	2.5	2.75	ms
		output from 10% to 90%, 5ms	4.5	5	5.5	ms
		output from 10% to 90%, 10ms	9	10	11	ms
	Output Discharge Resistance		-	40	-	Ω
	Feedback Input Current	VVDDP_S5_FBP =110%*VOUT	-	-	30	µA
PROTECTION						
	Under-voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	Over-voltage Protection (OVP)		125	130	135	%
	OVP Debounce TIme		-	2	-	µs
	High-side MOSFET Over-current- Protection(OCP)		1.7	2	2.3	A
	OCP Debounce TIme		-	2	-	µs
	Thermal Shutdown Protection	T_J Rising	-	150	-	°C
		Hysteresis	-	20	-	
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	V_{OUT}=0.8V, IOUT=50mA/100mA	-	75	-	%
		V_{OUT}=0.8V, IOUT=0.5A/1A	-	80	-	%

13.8 VR8 Electrical Characteristics

These specifications apply over $V_{LDO\_RTC\_IN}$ = 3.3V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(VR8)			Unit
			Min	Typ	Max	
SUPPLY VOLTAGE						
	Input Bias Current		-	1	2	μA
REGULATOR OUTPUT						
	Output Voltage	I_{OUT}=4.5μA	1.425	1.500	1.575	V
	Output Current Capability		4.5	-	-	μA
	Output Noise	f=100 to 100kHz	-	100	-	μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	-	50	-	dB
	Output Voltage Soft-start Time		-	1	-	ms

13.9 SW_VDD1V8 Switch

These specifications apply over V_{VDD5V_S5} = 5.06V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857(SW_VDD1V8)			Unit
			Min	Typ	Max	
	Power Switch On Resistance	$V_{SW\_VDD1V8\_IN}$=1.8V	-	16	20	mΩ
		$V_{SW\_VDD1V8\_IN}$=3.3V	-	-	20	mΩ
	Output Discharge Resistance		-	40	-	Ω
	Output Voltage Soft-start Time		160	200	240	us
	Current Limit	T_A = 25 °C	5	-	-	A
	Thermal Shutdown Protection	T_J Rising	-	150	-	℃
		Hysteresis	-	20	-	

13.10 VSYS & POK_Sx & EN_Sx Electrical Characteristics

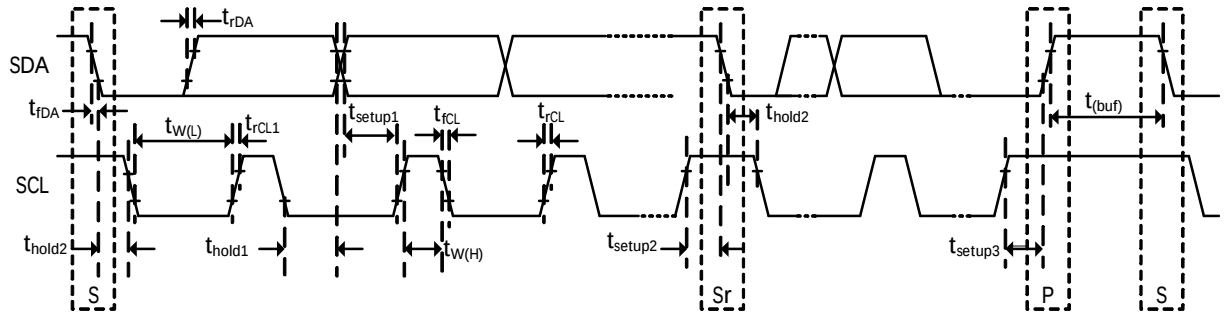
These specifications apply over V_{VDD5V_S5} = 5.06V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8857			Unit
			Min	Typ	Max	
VSYS INPUT						
	VSYS Supply Current	V_{SYS}=20V, EN_Sx=Low, only VDD5V_S5_LDO, 3V3_G3_LDO, LDO_RTC are on	-	120	-	µA
		EN_Sx=High, all VR are on, VR1/2/3/4/6 are no switching	-	90	-	µA
V_{SYS_UVLO}	VSYS Under-voltage Lockout (UVLO)	V_{VSYS} Rising, enable 5V_LDO and 3V3_G3_LDO	-	5.2	-	V
		Hysteresis	-	0.3	-	V
	VSYS Power-on Delay	V_{SYS}>V_{SYS_UVLO} to 5V_LDO soft-start starting	-	20	-	µs
POK_Sx, EN_Sx AND GPIO_G3						
	POK_Sx Threshold	POK in from Lower (POK goes high)	87	90	93	%
		POK out to normal (POK goes low)	125	130	135	%
		POK Hysteresis	-	3	-	%
	POK_Sx Leakage Current	V_{POK_Sx} = 5V	-	0.1	1	µA
	POK_Sx Low Voltage	I_{POK_sink} =4mA	-	0.5	1	V
	POK_Sx Enable Blanking Time	From VRs rising to POK goes High	-	1250	-	µs
	POK_Sx Disable Blanking Time	From VRs falling to POK goes Low	-	20	-	µs
	EN_Sx/GPIO_G3 Input Logic Threshold	V_{EN_Sx} rising	1.5	-	-	V
		V_{EN_Sx} falling	-	-	0.6	V
	EN_Sx/GPIO_G3 Leakage Current	EN_Sx =5V	-	-	1	µA
RESET FUNCTION						
	SEL_VDDAUD_S5 Reset Threshold		0	-	0.3	V
	SEL_VDDAUD_S5 Reset Debounce		-	30	-	ms

13.11 I²C Electrical Characteristics

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted).

Symbol	Parameter	High Speed		Fast Speed Plus		Fast Speed		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	Frequency, SCL	-	3.4	-	1	-	0.4	MHz
$t_{W(H)}$	Pulse Duration, SCL High	60	-	260	-	600	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low	160	-	500	-	1300	-	ns
t_{rCL}	Rise Time of SCL	10	40	-	120	20+0.1CL(pF)	300	ns
t_{rCL1}	rise time of SCL signal after a repeated START condition and after an acknowledge bit	10	80	-	-	-	-	ns
t_{fCL}	Fall Time of SCL	10	40	-	120	20+0.1CL(pF)	300	ns
t_{rDA}	Rise Time of SDA	10	80	-	120	20+0.1CL(pF)	300	ns
t_{fDA}	Fall Time of SDA	10	80	-	120	20+0.1CL(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	10	-	-	-	100	-	ns
t_{hold1}	Hold Time, SCL to SDA	10	70	100	-	100	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition	-	-	500	-	1300	-	ns
t_{setup2}	Setup Time, SCL to Start Condition	160	-	-	-	600	-	ns
t_{hold2}	Hold Time, Start condition to SCL	160	-	-	-	600	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition	160	-	-	-	600	--	ns
C_L	Load Capacitance for Each Bus Line	-	100	-	-	-	400	pF



I²C timing diagram

14.Register Description

14.1 Register Map

Channel	Register Name	Register Address	Read/Write/Read Only State	Default Value
VR1	VDD3V3_S5 DAC	0x02	R/W	14h
	VDD3V3_S5 Control	0x03	R/W	04h
VR2	VDD5V_S5 DAC	0x04	R/W	6Ch
	VDD5V_S5 Control	0x05	R/W	04h
VR3	VDDP DAC	0x06	R/W	1Eh
	VDDP Control	0x07	R/W	00h
VR4	VDD1V8_S5 DAC	0x08	R/W	23h
	VDD1V8_S5 Control	0x09	R/W	04h
VR5	VDD_AUD_S5 Control	0x0A	R/W	03h
VR6	VDDP_S5 DAC	0x0B	R/W	1Eh
	VDDP_S5 Control	0x0C	R/W	08h
SW_VDD1V8	SW_VDD1V8 Control	0x0D	R/W	00h
POK	POK Blanking Time	0x0E	R/W	44h
Thermal	Thermal Report	0x10	R	-
ID	Version ID	0x01	R	-

14.2 VR1 Register Table

Address	0x02							
Field Name	VDD3V3_S5 DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD3V3_S5_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	0	1	0	0
Bit Name	**Bit Definition**							
VDD3V3_S5_VSEL	00h : shutdown 01h : VR1 Voltage = 2920mV. 02h : VR1 Voltage = 2940mV. 03h : VR1 Voltage = 2960mV. … 14h : VR1 Voltage = 3300mV (Default) …. 37h : VR1 Voltage = 4000mV. 38h ~ ffh: Reserved.							

Address	0x03							
Field Name	VDD3V3_S5 CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD3V3_S5_RAMP		VDD3V3_S5_SLEW		VDD3V3_S5_FSW_SEL		VDD3V3_S5__SEL	VDD3V3_S5__EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	0
Bit Name	**Bit Definition**							
VDD3V3_S5_EN	0: VR1 off (Default) 1: VR1 on							
VDD3V3_S5_SEL	0: VR1 on/off is controlled by EN_S5 (Default) 1: VR1 on/off is controlled by VDD3V3_S5_EN State							
VDD3V3_S5_FSW_SEL	00 : FSW = 1.0MHz at PWM mode 01 : FSW = 0.6MHz at PWM mode (Default) 10 : FSW = 0.8MHz at PWM mode 11 : FSW = 1.2MHz at PWM mode							
VDD3V3_S5_SLEW	00 : Transition slew rate = 10mV/µs. (Default) 01 : Transition slew rate = 15mV/µs 10 : Transition slew rate = 20mV/µs 11 : Transition slew rate = 25mV/µs							
VDD3V3_S5_RAMP	00 : Ramp up Time = 1.25ms (Default) 01 : Ramp up Time = 2.5ms 10 : Ramp up Time = 5ms 11 : Ramp up Time = 10ms							

14.3 VR2 Register Table

Address	0x04							
Field Name	VDD5V_S5 DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD5V_S5_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	1	0	1	1	0	0
Bit Name	**Bit Definition**							
VDD5V_S5_VSEL	00h : shutdown 50h : VR2 Voltage = 4500mV. 51h : VR2 Voltage = 4520mV. 52h : VR2 Voltage = 4040mV. … 6ch : VR2 Voltage = 5060mV (Default) …. 82h : VR2 Voltage = 5500mV. 83h ~ ffh: Reserved.							

Address	0x05							
Field Name	VDD5V_S5 CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD5V_S5_RAMP		VDD5V_S5_SLEW		VDD5V_S5_FSW _SEL		VDD5V_S5 _SEL	VDD5V_S5 _EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	0
Bit Name	**Bit Definition**							
VDD5V_S5_EN	0: VR2 off (Default) 1: VR2 on							
VDD5V_S5_SEL	0: VR2 on/off is controlled by EN_S5 (Default) 1: VR2 on/off is controlled by VDD5V_S5_EN State							
VDD5V_S5_FSW_SEL	00 : FSW = 1.0MHz at PWM mode. 01 : FSW = 0.6MHz at PWM mode. (Default) 10 : FSW = 0.8MHz at PWM mode. 11 : FSW = 1.2MHz at PWM mode.							
VDD5V_S5_SLEW	00 : Transition slew rate = 10mV/µs. (Default) 01 : Transition slew rate = 15mV/µs. 10 : Transition slew rate = 20mV/µs. 11 : Transition slew rate = 25mV/µs							
VDD5V_S5_RAMP	00 : Ramp up Time = 1.25ms (Default) 01 : Ramp up Time = 2.5ms 10 : Ramp up Time = 5ms 11 : Ramp up Time = 10ms							

14.4 VR3 Register Table

Address	0x06							
Field Name	VDDP DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDP _VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	1	1	0
Bit Name	**Bit Definition**							
VDDP _VSEL	00h : shutdown 01h : VR3 Voltage = 510mV 02h : VR3 Voltage = 520mV … 1eh : VR3 Voltage = 800mV (Default) …. 28h : VR3 Voltage = 900mV … 64h : VR3 Voltage = 1500mV 65h~ffh : Reserved							

Address	0x07							
Field Name	VDDP CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDP _RAMP		VDDP _SLEW		VDDP _FSW _SEL		VDDP _SEL	VDDP_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
VDDP_EN	0: VR3 off (Default) 1: VR3 on							
VDDP_SEL	0: VR3 on/off is controlled by EN_S0 (Default) 1: VR3 on/off is controlled by VDDP_EN State							
VDDP_FSW_SEL	00 : FSW = 0.6MHz at PWM mode. (Default) 01 : FSW = 0.3MHz at PWM mode. 10 : FSW = 0.5MHz at PWM mode. 11 : FSW = 0.8MHz at PWM mode.							
VDDP_SLEW	00 : Transition slew rate = 10mV/μs. (Default) 01 : Transition slew rate = 15mV/μs. 10 : Transition slew rate = 20mV/μs. 11 : Transition slew rate = 25mV/μs							
VDDP _RAMP	00 : Ramp up Time = 1.25ms (Default) 01 : Ramp up Time = 2.5ms 10 : Ramp up Time = 5ms 11 : Ramp up Time = 10ms							

14.5 VR4 Register Table

Address	0x08							
Field Name	VDD1V8_S5 DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD1V8_S5_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	0	0	1	1
Bit Name	**Bit Definition**							
VDD1V8_S5_VSEL	00h : shutdown 01h : VR4 Voltage = 1460mV. 02h : VR4 Voltage = 1470mV. 03h : VR4 Voltage = 1480mV. … 23h : VR4 Voltage = 1800mV (Default) …. 50h : VR4 Voltage = 2250mV. 51h~ffh : Reserved							

Address	0x09							
Field Name	VDD1V8_S5 CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDD1V8_S5_RAMP		VDD1V8_S5_SLEW		VDD1V8_S5_FSW_SEL		VDD1V8_S5_SEL	VDD1V8_S5_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	0
Bit Name	**Bit Definition**							
VDD1V8_S5_EN	0: VR4 off (Default) 1: VR4 on							
VDD1V8_S5_SEL	0: VR4 on/off is controlled by EN_S5 (Default) 1: VR4 on/off is controlled by VDD1V8_S5_EN State							
VDD1V8_S5_FSW_SEL	00 : FSW = 3.0MHz at PWM mode. 01 : FSW = 2.0MHz at PWM mode. (Default) 10 : FSW = 1.0MHz at PWM mode. 11 : FSW = 4.0MHz at PWM mode.							
VDD1V8_S5_SLEW	00 : Transition slew rate = 10mV/µs. (Default) 01 : Transition slew rate = 15mV/µs. 10 : Transition slew rate = 20mV/µs. 11 : Transition slew rate = 25mV/µs							
VDD1V8_S5_RAMP	00 : Ramp up Time = 1.25ms (Default) 01 : Ramp up Time = 2.5ms 10 : Ramp up Time = 5ms 11 : Ramp up Time = 10ms							

14.6 VR5 Register Table

Address	0x0A							
Field Name	VDD_AUD_S5 CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved		VDD_AUD_S5_SEL	VDD_AUD_S5_EN	VDD_AUD_S5_VSEL			
Read/Write			R/W	R/W	R/W	R/W	R/W	R/W
Power On Default			0	0	0	0	1	1

Bit Name	Bit Definition
VDD_AUD_S5_VSEL	00 : shutdown. 01h : VDD_AUD_S5 Voltage = Vnominal -2%. 02h : VDD_AUD_S5 Voltage = Vnominal -1%. 03h : VDD_AUD_S5 Voltage = Vnominal 0%. (Default) 04h : VDD_AUD_S5 Voltage = Vnominal +1%. 05h : VDD_AUD_S5 Voltage = Vnominal +2%. 06h : VDD_AUD_S5 Voltage = Vnominal +3%. 07h : VDD_AUD_S5 Voltage = Vnominal +4%. 08h : VDD_AUD_S5 Voltage = Vnominal +5%. 09h : VDD_AUD_S5 Voltage = Vnominal +6%.
VDD_AUD_S5_EN	0: VR5 off (Default) 1: VR5 on
VDD_AUD_S5_SEL	0: VR5 on/off is controlled by EN_S5. (Default) 1: VR5 on/off is controlled by VDD_AUD_S5_EN State.

14.7 VR6 Register Table

Address	0x0B							
Field Name	VDDP_S5 DAC [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDP_S5_VSEL							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	1	1	1	1	0
Bit Name	**Bit Definition**							
VDDP_S5_VSEL	00h : shutdown 01h : VR6 Voltage = 510mV. 02h : VR6 Voltage = 520mV. 03h : VR6 Voltage = 530mV. … 1eh : VR6 Voltage = 800mV (Default) …. 64h : VR6 Voltage = 1500mV. 65h~ffh : Reserved							

Address	0x0C							
Field Name	VDDP_S5_CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VDDP_S5_RAMP		VDDP_S5_SLEW		VDDP_S5_FSW _SEL		VDDP_S5_ _SEL	VDDP_S5_ _EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	0	0	0
Bit Name	**Bit Definition**							
VDDP_S5_EN	0: VR6 off (Default) 1: VR6 on							
VDDP_S5_SEL	0: VR6 on/off is controlled by EN_S5 (Default) 1: VR6 on/off is controlled by VDDP_S5_EN State							
VDDP_S5_FSW_SEL	00 : FSW = 3.0MHz at PWM mode. 01 : FSW = 2.0MHz at PWM mode. 10 : FSW = 1.0MHz at PWM mode. (Default) 11 : FSW = 4.0MHz at PWM mode.							
VDDP_S5_SLEW	00 : Transition slew rate = 10mV/µs. (Default) 01 : Transition slew rate = 15mV/µs. 10 : Transition slew rate = 20mV/µs. 11 : Transition slew rate = 25mV/µs							
VDDP_S5_RAMP	00 : Ramp up Time = 1.25ms (Default) 01 : Ramp up Time = 2.5ms 10 : Ramp up Time = 5ms 11 : Ramp up Time = 10ms							

14.8 SW_VDD1V8 Register Table

Address	0x0D							
Field Name	SW_VDD1V8_CONTROL [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved						SW_VDD1V8_SEL	SW_VDD1V8_EN
Read/Write							R/W	R/W
Power On Default							0	0
Bit Name	**Bit Definition**							
SW_VDD1V8_EN	0: SW_VDD1V8 off (Default) 1: SW_VDD1V8 on							
SW_VDD1V8_SEL	0: SW_VDD1V8 on/off is controlled by EN_S0 & EV_S5(Default) 1: SW_VDD1V8 on/off is controlled by VDDP_S5_EN State							

14.9 Thermal Report Register Table

Address	0x10							
Field Name	THERMAL REPORT[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved			THERMAL REPORT				
Read/Write				R	R	R	R	R
Power On Default				-	-	-	-	-
Bit Name	**Bit Definition**							
Thermal Report	00000 : -10℃ 00001 : -5℃ 00010 : 0℃ … 01000 : 30℃ … 11110 : 140℃ 11111 : 145℃							

14.10 POK BLANKING Time Register Table

Address	0x0E							
Field Name	POK BLANKING TIME [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	POK_S5 BLANKING TIME				POK_S5 BLANKING TIME			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	0	0	1	0	0
Bit Name	**Bit Definition**							
POK_S5 Blanking Time	00h : 250µs 01h : 500µs 02h : 750µs … 04h : 1250µs (Default) …. 0fh : 4000µs							
POK_S0 Blanking Time	00h : 250µs 01h : 500µs 02h : 750µs … 04h : 1250µs (Default) …. 0fh : 4000µs							

14.11 Version ID Register

Address	0x01							
Field Name	VERSION ID [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MAJOR VERSION ID [7:4]				Reserved	MINOR VERSION ID [2:0]		
Read/Write	R	R	R	R	R	R	R	R
Power On Default	-	-	-	-	-	-	-	-
Bit Name	**Bit Definition**							
MAJOR VERSION ID	0Ah:Verson A 0Bh:Verson B 0Ch:Verson C 0Dh:Verson D 0Eh:Verson E 0Fh:Verson F							
MINOR VERSION ID	00h:Verson 0 01h:Verson 1 02h:Verson 2 03h:Verson 3 04h:Verson 4 05h:Verson 5 06h:Verson 6 07h:Verson 7							

15.Function Description

15.1 VR Function Description

Soft-Start

All VRs are equipped soft-start function, when enable signal of each VR is activated, an internal soft start ramps the output voltage at a time which can be set via I²C. This allows the output voltage to ramp up gradually, eliminating overshoot and excessive in rush current.

Over Voltage Protection (OVP) for VR4 and VR6

The over voltage protection circuitry monitors the feedback voltage to prevent the output from accidently exceeding the desired set point. Once the feedback voltage exceeds typically 130% of the set point voltage, the high side MOSFET turn off, low side MOSFET turns off and internal latch circuitry is activated. This insures protection of the load damage and circuit reset is only achieved either by pulling SEL_VDDAUD_S5 to ground or by cycling the power.

Over Current Protection (OCP) and Under Voltage Protection (UVP) for VR4 and VR6

The switching converter is protected against gradual over current and sudden short on its output. When inductor current peak value exceeds the set threshold, an internal over-current protection is activated which turns off the high side and low side MOSFETs. Once the output voltage drops below a typical threshold of 70% of set point value, both high side and low side MOSFETs turn off and an internal latch circuit is initiated. When any of OCP or UVP is activated, the IC will be latched off, circuit reset is only achieved either by pulling SEL_VDDAUD_S5 to ground or by cycling the power.

Over Voltage Protection (OVP) and Under Voltage Protection (UVP) for VR1, VR2 and VR3

Once the output voltage drops below a typical threshold of 70% of set point value or the output voltage exceeds typically 130% of the set point voltage, the PWM signal will be latched low to turn off the converter and discharge the output voltage. When any of UVP or OVP is activated, the IC will be latched off, circuit reset is only achieved either by pulling SEL_VDDAUD_S5 to ground or by cycling the power.

Soft-Stop

When VR4, VR6 is shut down by EN_Sx or I2C, both upper and lower MOSFETs will be turned off and an internal MOSFET with about 40 ohm (Typ.) Rds-on discharges the output via the FBP pin. The VR5 also discharges the output via the output pin.

When VR1, VR2, VR3 is shut down by EN_Sx or I²C, the PWM signal pin will be low level to discharge the output voltage via the low-side MOSFET of power stage.

VDD_AUD_S5 Output Voltage

The VDD_AUD_S5 output voltage level can be set by connected a resistor from SET_VDDAUD_S5 pin to ground, below table shows the resistor value for different voltage setting. Because the input voltage of VDD_AUD_S5 comes from output voltage of VDD1V8_S5, when 1.2V or 1.5V output voltage is selected, the VDD_AUD_S5 is a LDO regulator; and when 1.8V is selected, the VDD_AUD_S5 will be changed to a power switch.

Resistor Value	Output Voltage	VDD_AUD_S5 Output State
60k, 1%	1.2V	LDO Regulator
110k, 1%	1.5V	LDO Regulator
165k, 1%	1.8V	Power Switch

15.1 VR Function Description(Cont.)

POK Output

The POK_Sx circuitry monitor the VR1~VR6 and SW_VDD1V8 via the FB pins of each regulator to make sure that the output of each regulator has reached its desired set point during the start up. When all these voltages have reached about 90% of their set point, then POK_Sx will switch from a low state to high after a 1.25 ms delay time. The POK_Sx pin are an open drain output that will switch high via an external pull up resistor. It can be pulled up to a maximum voltage of up to 5.5V.

The POK_Sx also monitor the FB voltage for any over voltage that may happen during the operation. This threshold is typically set at 130% of the desired set point. If any of the voltages exceeds this threshold and satisfied the blanking time the POK_Sx switch low and after a short delay time about 20u sec or so, the outputs latch off and system returns to G3 state.

During the power down or at any point either of these VRs, output voltages drop below about 87% of the set point and continue over blanking time, the POK pin switches to low state.

SW _VDD1V8 Power Switch

The SW_VDD1V8 is an N-channel MOSFET power switch with current limit protection. The RDS(ON) is about 16 mOhm to load at least 2.5A current.

The switch is controlled by EN_S0, when EN_S0 is high, the switch is on, and a soft-start will control the slew rate of output voltage and limit the current surge during start-up; when EN_S0 is low, the switch is off and a output discharge device is turned on to discharge the output voltage.

15.2 I2C Function Description

I2C Overview

APW8857 is a slave-only device that is mastered by the SoC. It resides off the SoC's I^2C. The slave device implemented on APW8857 side is an asynchronous implementation and will support the high speed mode (3.4MHz). Some of the main features for the I^2C slave are:

- APW8857 is accessed using a 7-bit addressing scheme.
- I^2C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.
- The interface draws as minimum power when not actively reading/writing registers.
- The slave adapts to the incoming frequency without any communication as the protocol for fast mode and high speed mode is the same.
- Interface implementation is asynchronous.

Slave Address

APW8857 supports the standard I^2C read and write functions. The configuration register space is divided to 59-byte partitions. APW8857 supports a 7-bit device addresses to access each of the 59 byte partitions.

Slave Address
1101110

Table 5. I^2C Slave Addresses

The slave addresses need to be locked in order to avoid that software can overwrite them and disable the communication.

15.2 I²C Function Description(Cont.)

Protocol

Reads from PMIC registers follow the “combined protocol” as described in the I²C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different high-speed and fast-speed transaction format/protocol.

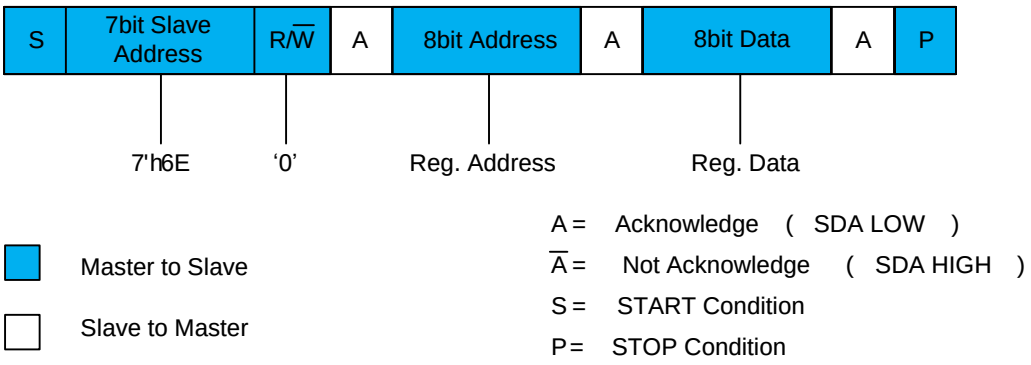


Figure 1. I²C Fast Speed / Fast Speed Plus Single Byte Write

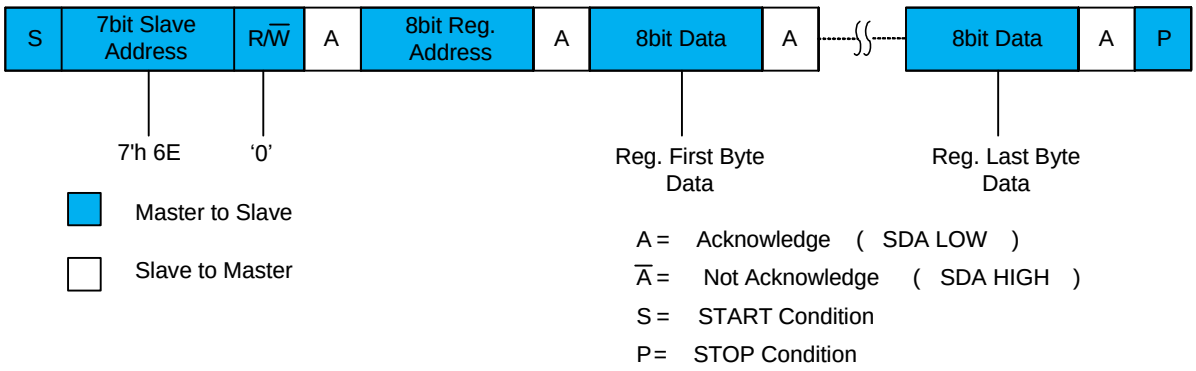


Figure 2. I²C Fast Speed / Fast Speed Plus Multiple Byte Write

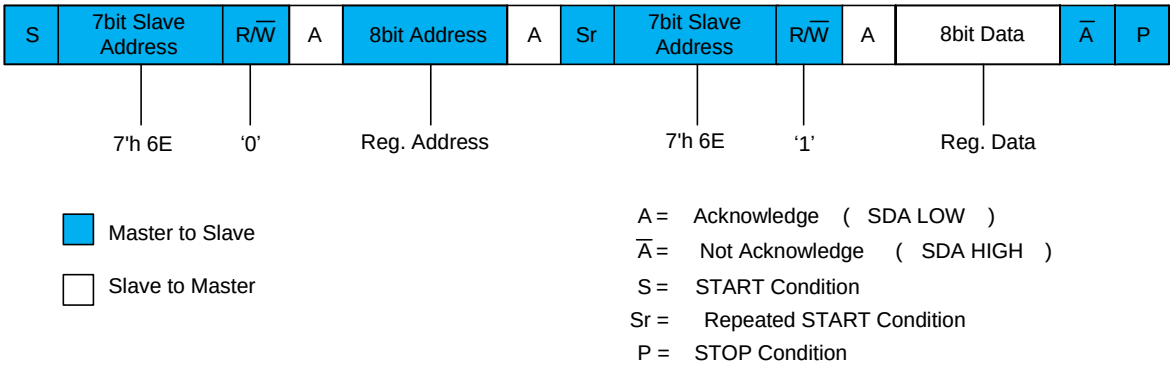


Figure 3. I²C Fast Speed / Fast Speed Plus Single Byte Read

15.2 I²C Function Description(Cont.)

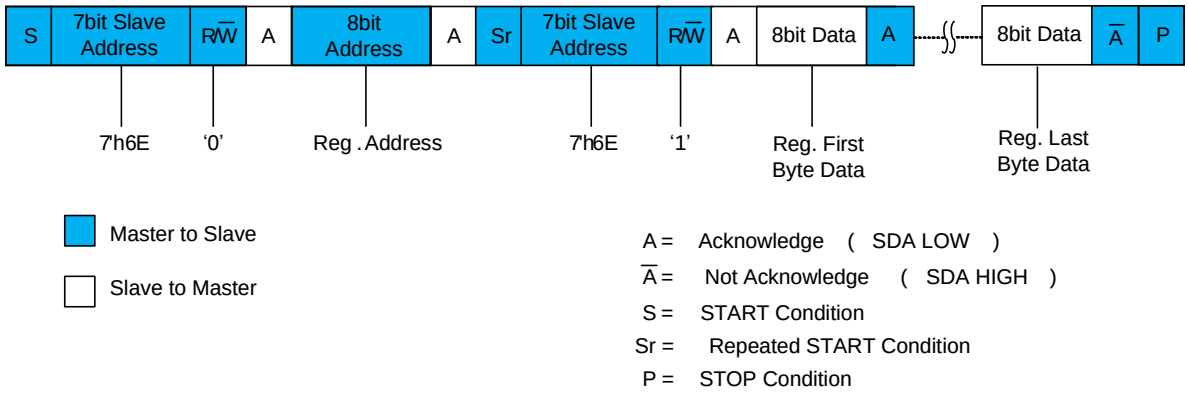


Figure 4. I²C Fast Speed / Fast Speed Plus Multiple Byte Read

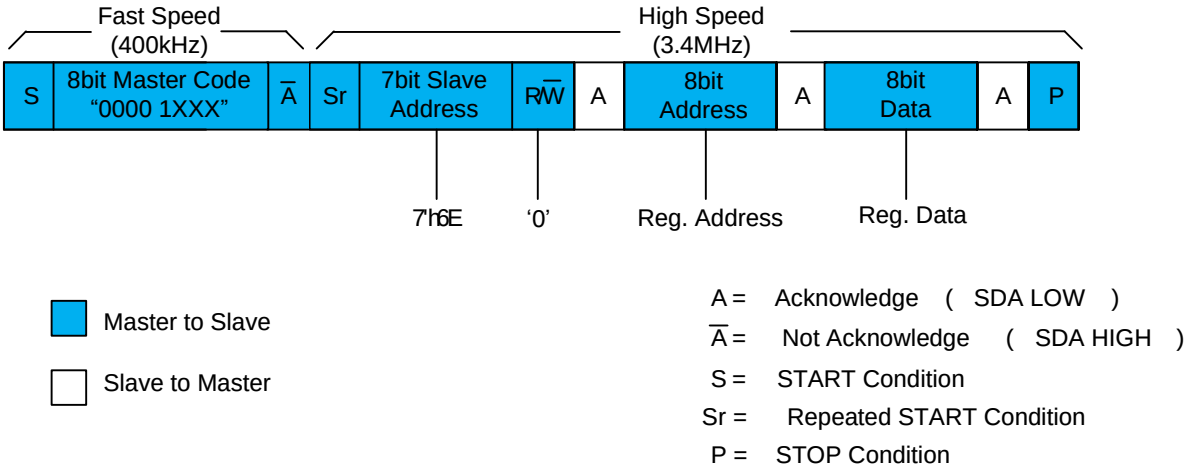


Figure 5. I²C High Speed Single Byte Write

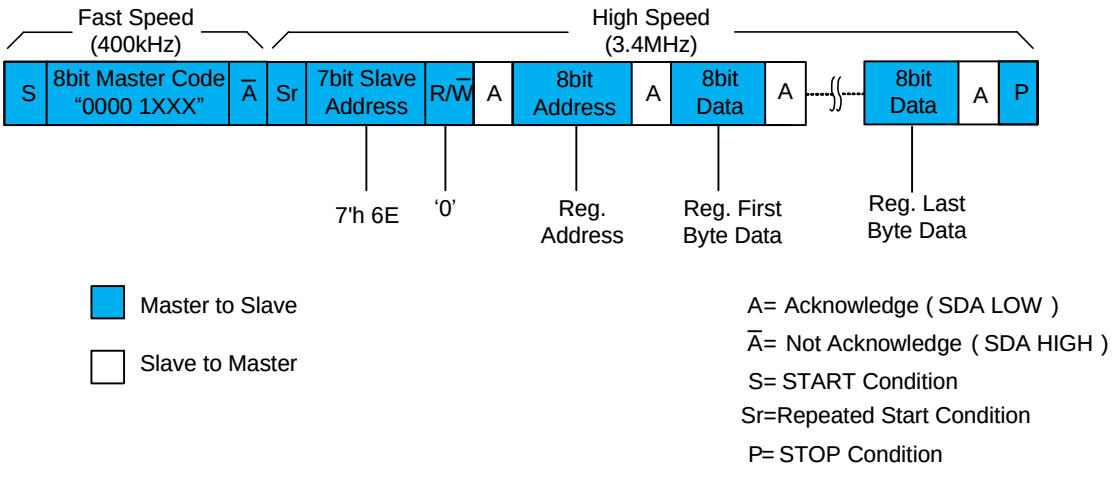


Figure 6. I²C High Speed Multiple Byte Write

15.2 I²C Function Description(Cont.)

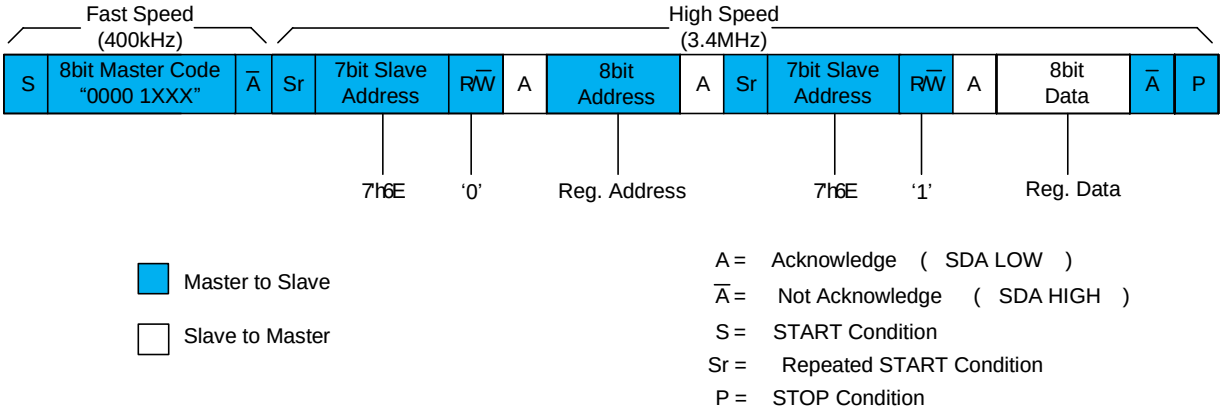


Figure 7. I²C High Speed Single Byte Read

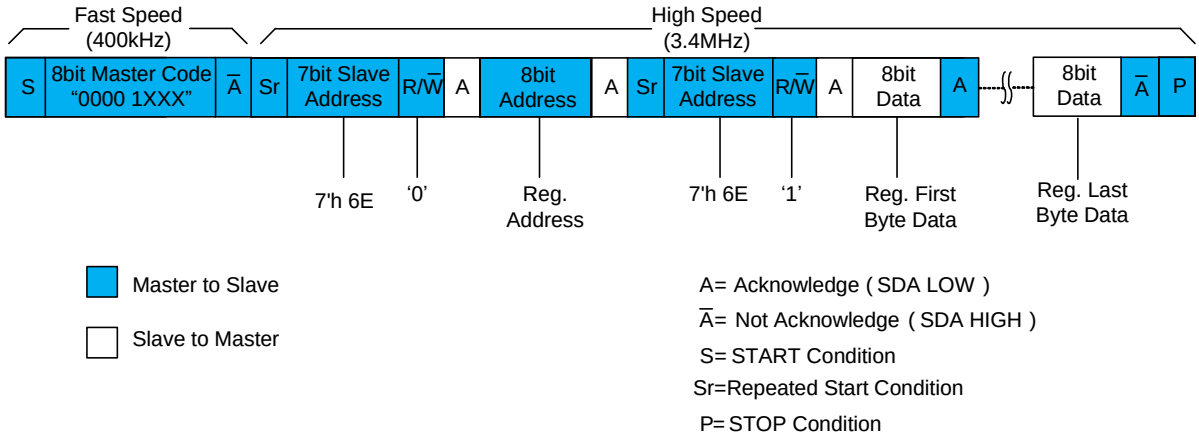


Figure 8. I²C High Speed Multiple Byte Read

16.Application Information

PWM Converter Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

For PWM converter, the inductor value (L) determines the sum of the inductor ripple currents ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator, although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

PWM Converter Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

16.Application Information(Cont.)

PWM Converter Input Capacitor Selection (Cont.)

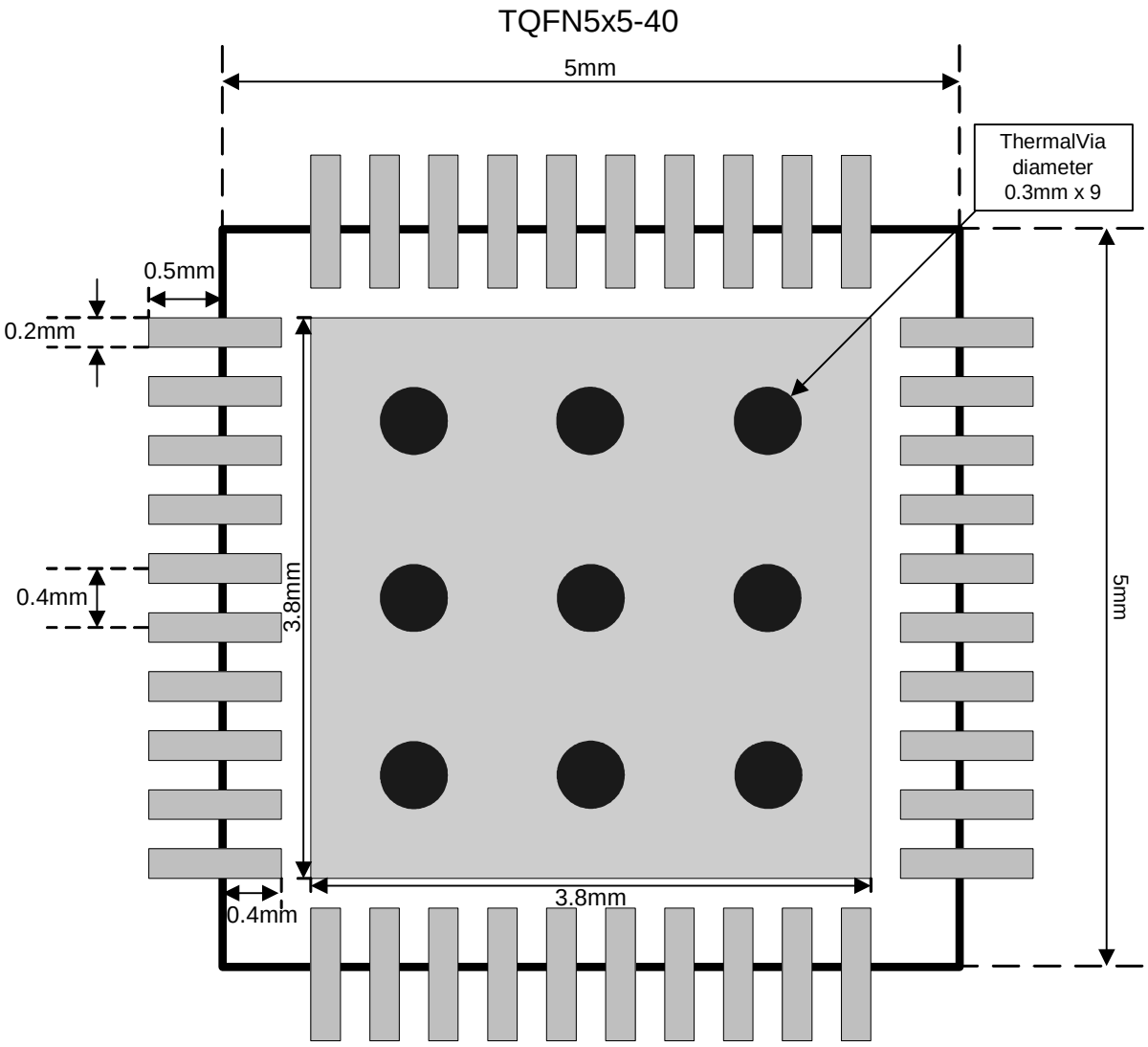
Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET. The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The maximum RMS current rating requirement is approximately $I_{OUT/2}$, where I_{OUT} is the load current.

Layout Consideration

Signal Name	Description	Layout Guidelines
GND	IC's analog ground.	Connect the GND pin to GND plane through several vias directly.
VDDP_S5_PGND,and VDD1V8_S5_PGND	IC's power ground pins of VR4 and VR6.	Use a ground plane or a short and wide trace to connect the ground terminals of input capacitors and output capacitors, and PGND pins.
Each of VR's Input Pins (VSYS, VDD1V8_S5_IN...)	All VR's input voltage pins.	Place the input capacitors on each of the VR's input pins with low impedance to GND and low impedance to the each of VR's input pins.
Each of PWM VR's LX pins (VDD5V_S5_LX, VDD1V8_S5_LX…)	These are the connections to the mid point of the power stage consisting of the high- and low-side switch. The output inductor is connected here.	Connect to the output inductor with a short wire. For higher efficiency requirement, the inductor and LX pins should be as close as possible, and the trace resistance from LX pin to inductor should be less than 10mOhm is recommended. Ideally, route the high current path like LX pins to inductors and inductors to output capacitors on the top layer is recommended.
Each of PWM VR's output voltage feedback pins (VDD5V_S5_FBP, VDD1V8_S5_FBP…)	Voltage feedback pin for each of VR.	The pins are high impedance and sensible to noise from the switch node. The positive feedback signal should be tied to the V+ pad of the output capacitor directly. Coupling from fast switching signals must be avoided. Due to LDO bypass function requirement, the width and length of PCB trace from output to these pins should be as wide (short) as possible, <0.2 Ohm is recommended.
VSYS	APW8857 input supply voltage	Connect the input capacitors from VSYS to GND for noise decoupling. The capacitors and VSYS pin should be as close as possible.
VDD5V_S5_PWM, VDD3V3_S5_PWM, VDDP_PWM	The gate driver outputs of VDD5V_S5, VDD3V3_S5 and VDDP	The traces of PWM signal from the gate driver output pins to the DrMOS should be short to eliminate the parasitical capacitance; the parasitical capacitance less than 80pF is recommended.

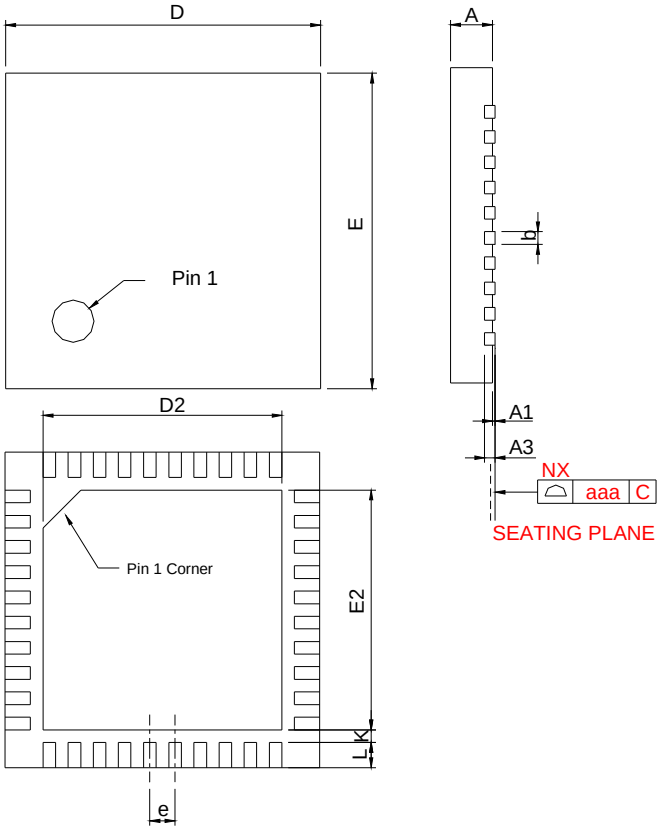
16.Application Information(Cont.)

TQFN 5x5 40pin min. footprint



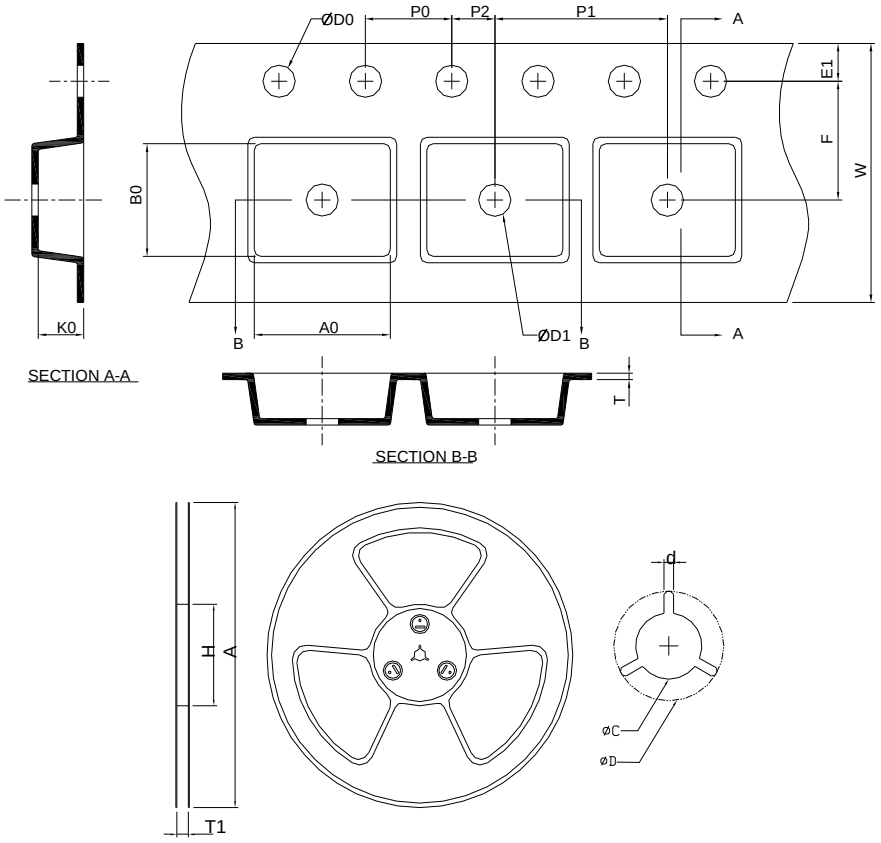
17.Package Information

TQFN5x5-40



SYMBOL	TQFN5*5-40			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.20	3.50	0.126	0.138
E	4.90	5.10	0.193	0.201
E2	3.20	3.50	0.126	0.138
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

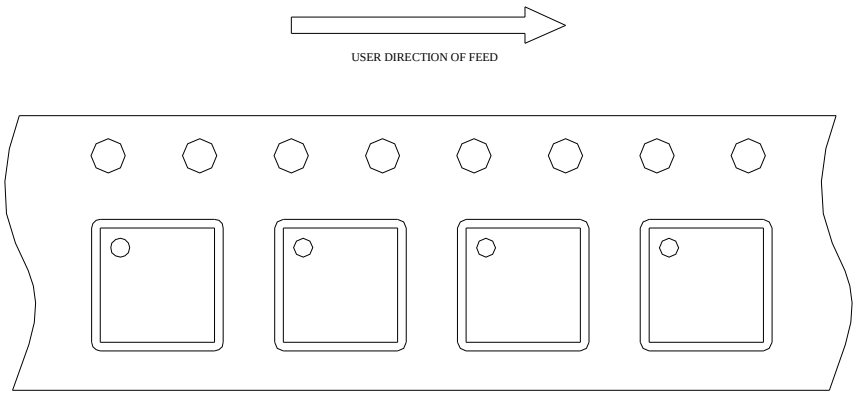
(mm)

Devices Per Unit

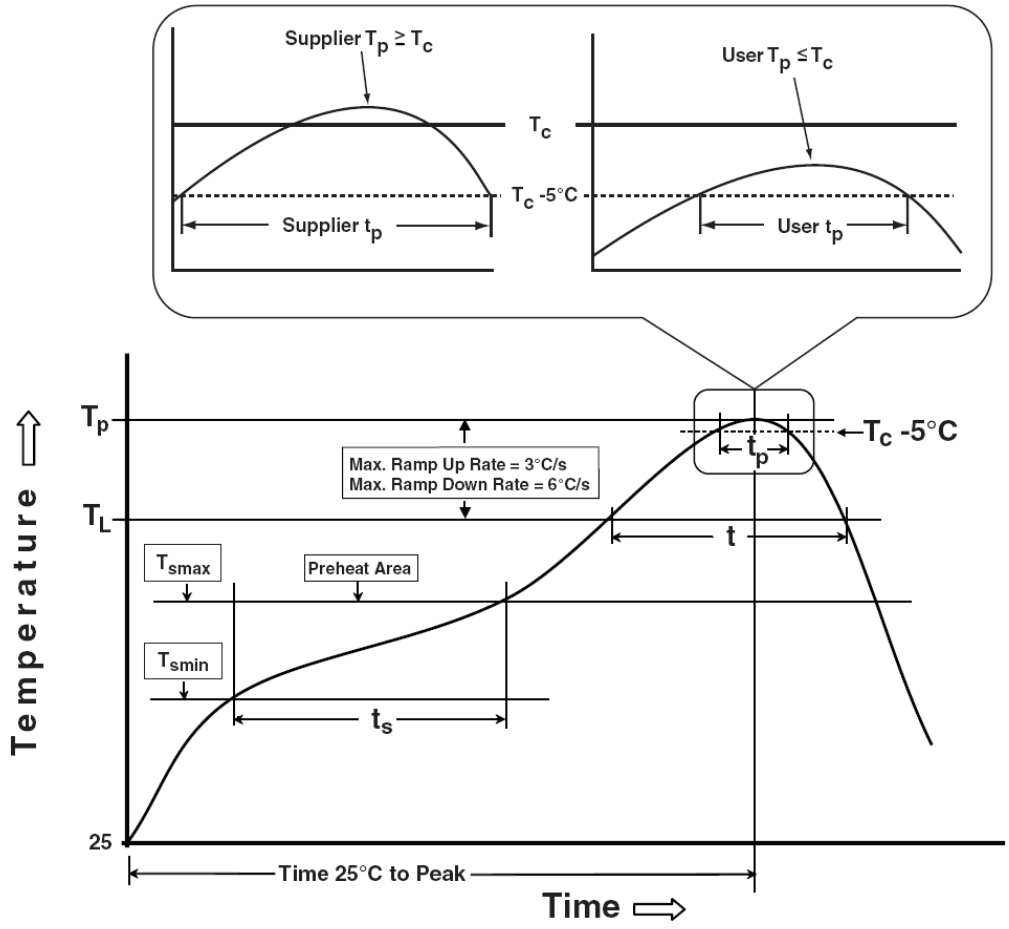
Package Type	Unit	Quantity
TQFN5x5	Tape & Reel	2500

Taping Direction Information

TQFN5x5-40



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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