Wide Input 5.4V to 21V Power Management IC(PMIC) for High Performance Computing Applications

1.General Description

The APW8858 is a Power Management IC (PMIC) designed to provide complete Power Management solution for Intel GLK(*) plateform applications. The IC operates from a single supply voltage of 5.4V to 21V allowing it to be used in 2 Cell to 4 Cell battery applications. The APW8858 is designed to provide maximum number of regulators in the smallest available cost effective package. Included in the IC are; Four Switching Buck controllers for 5V and 3.3V system voltages as well as VDDQ and VCCRAM, Two LDOs for variety of applications such as memory VTT and VPP(V25U), Tow internal high frequency 3A Buck regulators typically used for 1.8V and 1.2V supply and One load switch(V18U). The PWM controllers use the ANPEC cost effective external Power Blocks APW870x family for minimum pin interface with the PMIC, while providing output currents of up to 25A capability.

The IC is equipped with all the standard protection features such as over current, over voltage and internal under voltage lock out protection as well as thermal SD.

The serial interface is an I²C communication interface which allows supply sequencing as well as controlled margining of ramp up and ramp down of all supplies to optimize battery power consumption. The I²C interface also allows for adjustability of Soft Start, Forced PWM/Auto PFM/PWM, power sequencing as well output discharge and IRQ.

The IC is offered in a small TQFN, 5x5-40L package for best thermal performance while optimizing the cost.

(*)Intel Trade mark

2.Applications

- **High Performance Notebook and Ultra Notebook**
- **2 Cell Tablet Applications**
- **High Performance Digital Signage**

3.Features

■ Voltage Rail

- **Provide 4 Buck Single Phase PWM Controllers**
  - VR1(VNN) 0.5V ~ 1.45V, 5A peak
  - VR2(VCCGI) 0.5V ~ 1.45V, 25A peak
  - VR3(VCCRAM) 1.05V ~ 1.1V, 4.5A peak
  - VR6(VDDQ) 1.1V/1.15V1.2V/1.35V, 7A peak
- **Provide 2 Buck Single Phase PWM Converters**
  - VR4(V1P8A) 1.8V ~ 1.88V, 3A peak
  - VR5(V1P2A) 1.1V ~ 1.24V, 2.5A peak
- **Provide 2 LDO Outputs**
  - VR7(VTT) 0.5*VDDQ, 0.6A continuous
  - VR8(VPP) 2.5V, 1A continuous
- **Provide 1 Load Switche**
  - VR8(V18U) 1.8V, 1A continuous

■ Power Management Controller

- **Support G3, S5/S4, S3, S0, DS5, DS4, DS3, and S0ix states**
- **POK and IRQ Signal for VR power state: PCH_PWROK, RSM_RST# and IRQ#**
- **Support Several Memory Types: DDR3L, DDR4, LPDDR3, LPDDR4, DDR4RS, DDR4E, 3DXPoint**

■ Communication Interface

- **I2C Interface for SoC Access**
- **Support Bit Rate 0.4MBit/s and 1MBit/s**

■ Built in Current limit, Over Voltage protection and Over temperature protection

■ TQFN5x5-40 Package.

4.Ordering and Marking Information

<table>
<tr>
<td>APW8858 □□□□□□-□□□
Assembly Material
Handling Code
Temperature Range
Package Code
Product Code</td>
<td>Product Code
Omited or -01, -02, -03 or -04, see below table for details
Package Code
QB : TQFN 5x5-40
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device</td>
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XXXXX
X - Date Code</td>
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<td>APW8858-04QBI : 04
APW 8858
XXXXX
X - Date Code</td>
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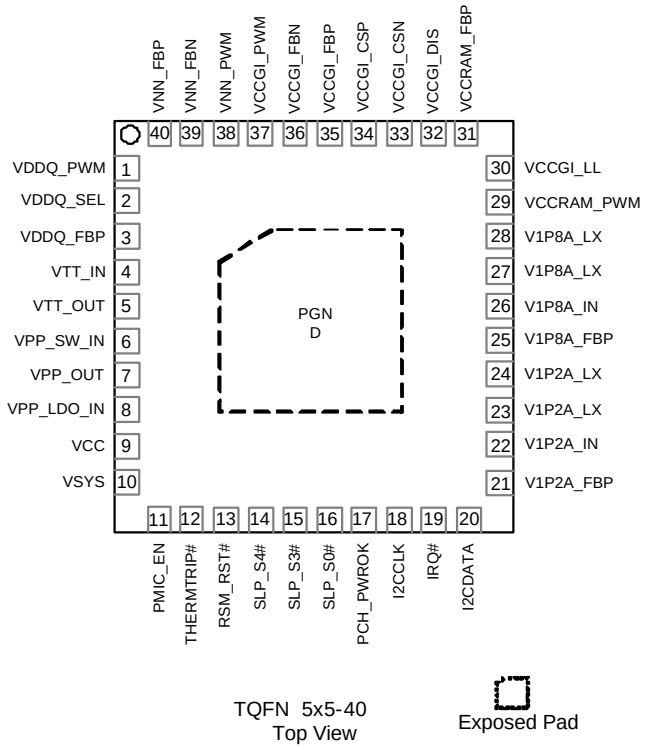
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Part Number	Description
APW8858QBI	All VRs are enabled
APW8858-01QBI	VNN and VCCGI are disabled
APW8858-02QBI	V1P2A is disabled. V1P2A power rail is supplied by VDDQ via external circuitry. VDDQ’s timing is different from APW8858QBI
APW8858-03QBI	VCCRAM is disabled. VCCRAM power rail is merged into VNN power rail. VNN’s voltage is fixed at 1.05V and not adjustable.
APW8858-04QBI	1. V1P2A is disabled. V1P2A power rail is supplied by VDDQ via external circuitry. VDDQ’s timing is different from APW8858QBI 2. VCCRAM is disabled. VCCRAM power rail is merged into VNN power rail. VNN’s voltage is fixed at 1.05V and not adjustable.

5.Pin Configuration



6.Absolute Maximum Ratings (Note 1)

Pin or Symbol	Parameter	Rating	Unit
VSYS	VSYS to PGND	-0.3~28	V
VCC, V1P8A_IN, V1P2A_IN, VTT_IN, VPP_LDO_IN, VPP_SW_IN	VCC, V1P8A_IN, V1P2A_IN, VTT_IN, VPP_LDO_IN, VPP_SW_IN to PGND	-0.3 to 6.5	V
V1P8A_LX, V1P2A_LX	V1P8A_LX, V1P2A_LX to PGND	-0.3 to 6.5	V
VNN_FBP, VNN_FBN, V3V3_FBP, VCCGI_ FBP, VCCGI_ FBN, VCCGI_ CSP, VCCGI_ CSN, VCCRAM_FBP, V1P8A_ FBP, V1P2A_ FBP, VDDQ_FBP	VNN_FBP, VNN_FBN, V3V3_FBP, VCCGI_ FBP, VCCGI_ FBN, VCCGI_ CSP, VCCGI_ CSN, VCCRAM_FBP, V1P8A_ FBP, V1P2A_ FBP, VDDQ_FBP to PGND	-0.3 to 6.5	V
VNN_PWM, VCCGI_PWM, VCCRAM_PWM, VDDQ_PWM	VNN_PWM, VCCGI_PWM, VCCRAM_PWM, VDDQ_PWM to PGND	-0.3 to 6.5	V
All Other Pins	All Other Pins to PGND	-0.3 to 6.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	43	°C/W
θ_{JC}	Junction-to-Case Resistance in free air	5	°C/W

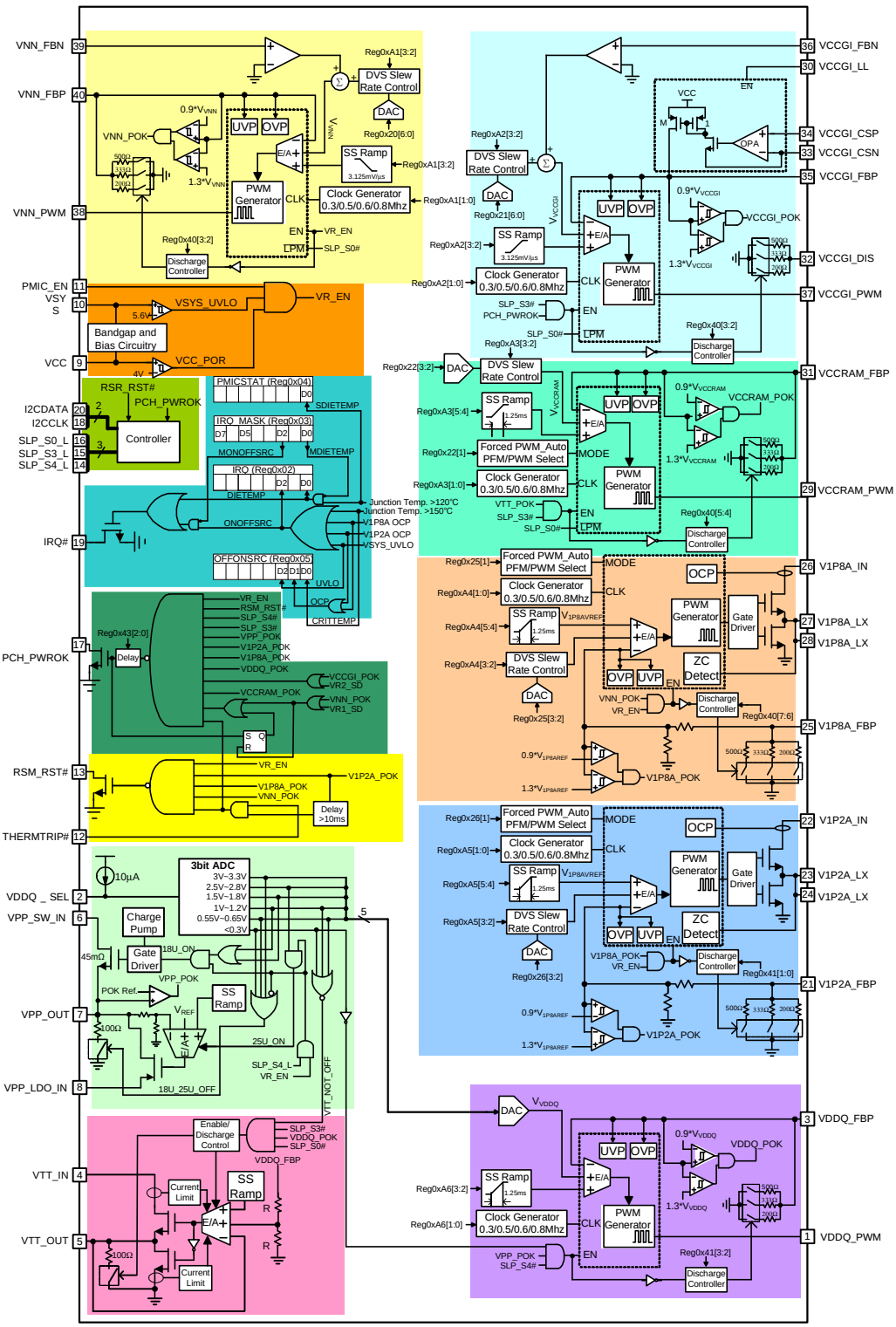
Note2: θ_{JA} is measured with the component mounted on a JESD-51-7 high effective thermal conductivity test board in free air.

8.Recommended Operating Conditions(Note3)

Symbol	Parameter	Range	Unit
V_{VSYS}	System Rail From Battery Management Unit	5.4 ~ 21	V
V_{VCC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{V1P8A_IN}	V1P8A Regulator Input Voltage	3 ~ 5.5	V
V_{V1P2A_IN}	V1P2A Regulator Input Voltage	3 ~ 5.5	V
$V_{PP\_LDO\_IN}$	GATE1 LDO Input Voltage	V_{V3P3A}	V
$V_{PP\_SW\_IN}$	GATE1 Load Switch Input Voltage	V_{V1P8A}	V
$V_{SLP\_S0\#}$	SLP_S0_L Input Low Voltage	0 ~ 0.4	V
	SLP_S0_L Input High Voltage	1.2 ~ 3.3	V
$V_{SLP\_S3\#}$	SLP_S3_L Input Low Voltage	0 ~ 0.4	V
	SLP_S3_L Input High Voltage	1.2 ~ 3.3	V
$V_{SLP\_S4\#}$	SLP_S4_L Input Low Voltage	0 ~ 0.4	V
	SLP_S4_L Input High Voltage	1.2 ~ 3.3	V
V_{PMIC_EN}	PMIC_EN Input Low Voltage	0 ~ 0.4	V
	PMIC_EN Input High Voltage	1.2 ~ 3.3	V
$V_{THERMTRIP\#}$	THERMTRIP# Input Low Voltage	0 ~ 0.4	V
	THERMTRIP# Input High Voltage	1.2 ~ 3.3	V
$V_{RSM\_RST\#}$	RSM_RST# Pull High Voltage	1.8 ~ 3.3	V
V_{PCH_PWROK}	PCH_PWROK Pull High Voltage	1.8 ~ 3.3	V
$V_{IRQ\#}$	IRQ Pull High Voltage	1.8 ~ 3.3	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

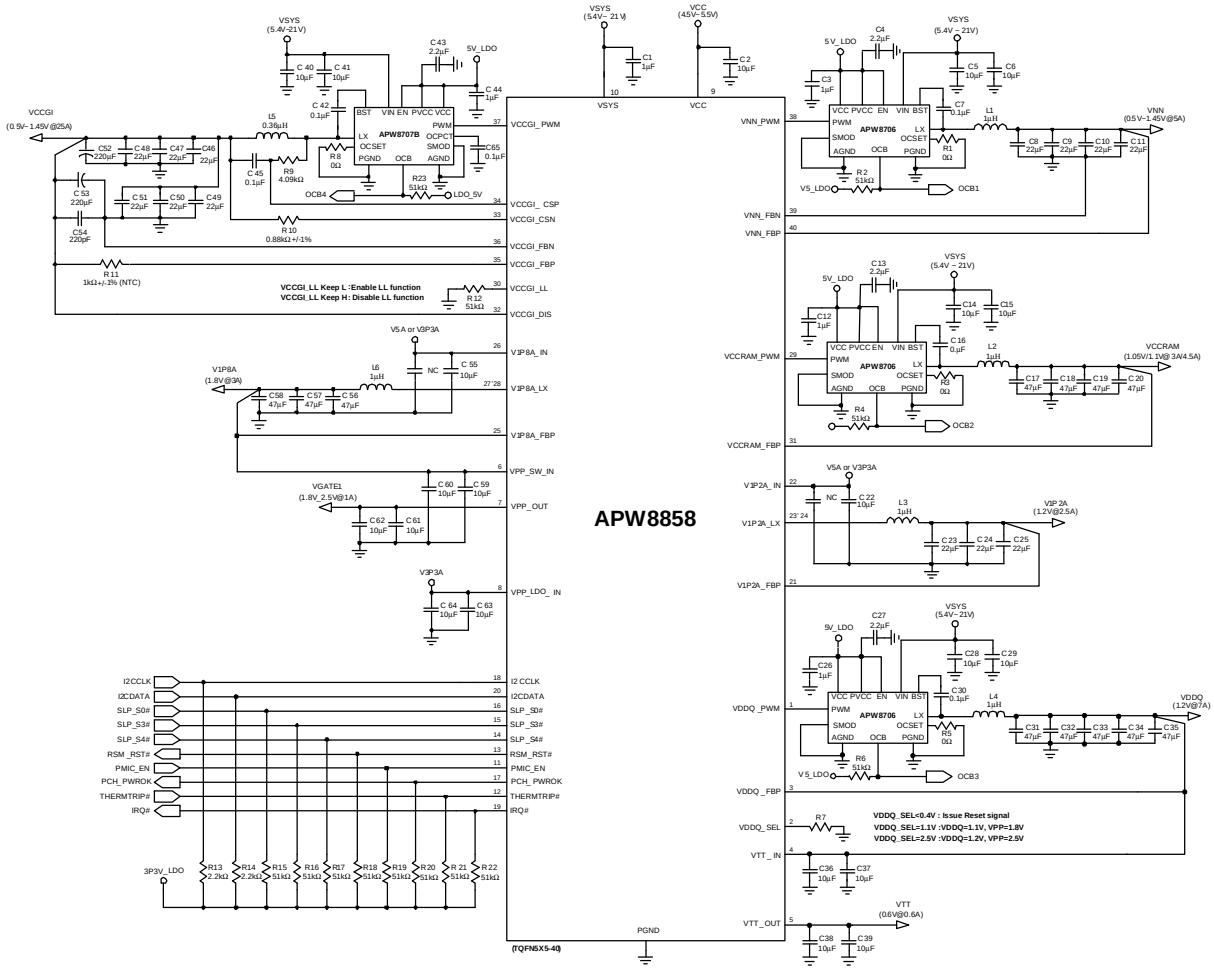
Note 3: Refer to the typical application circuit.

9.Block Diagram

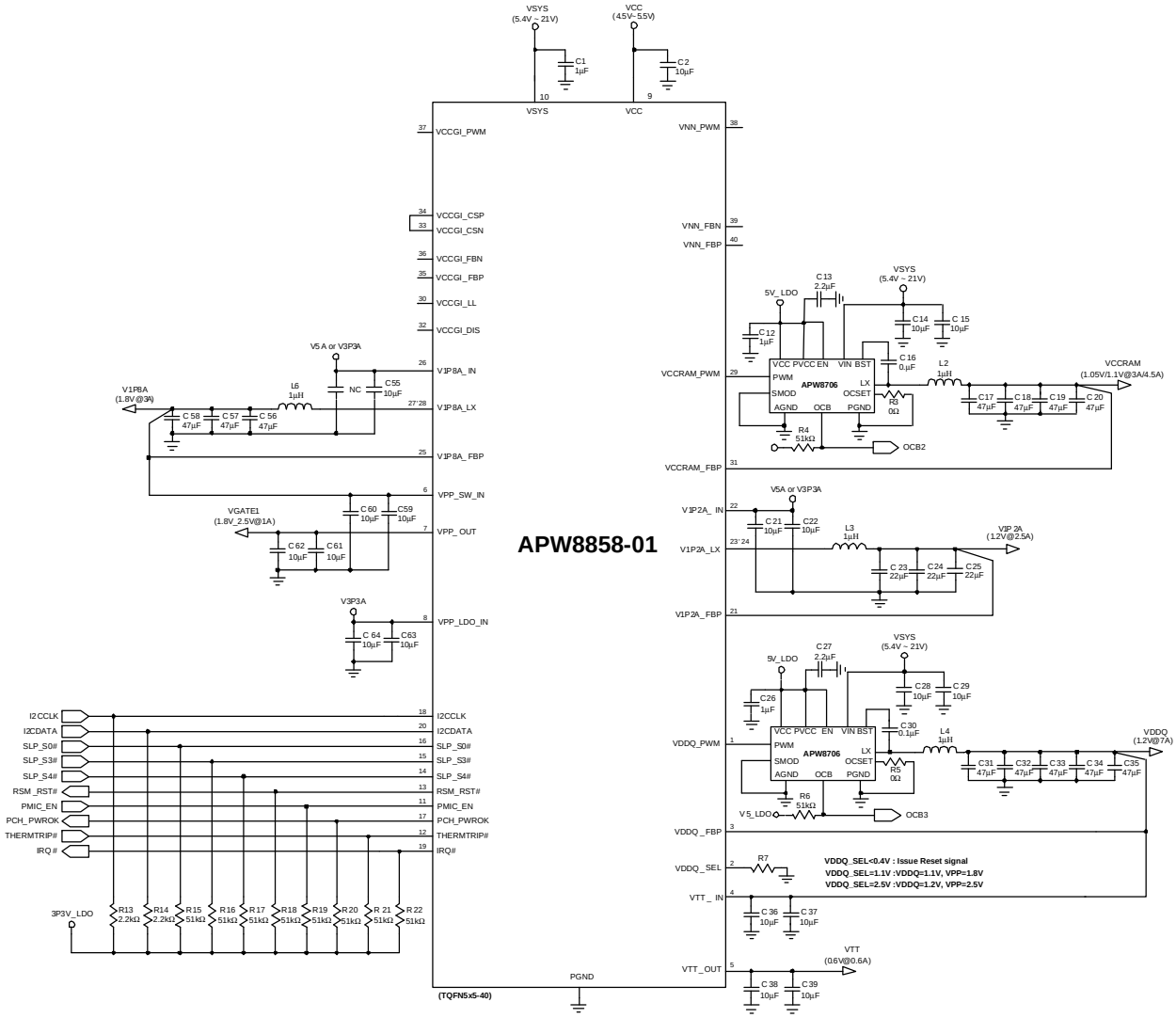


10.Typical Application Circuit

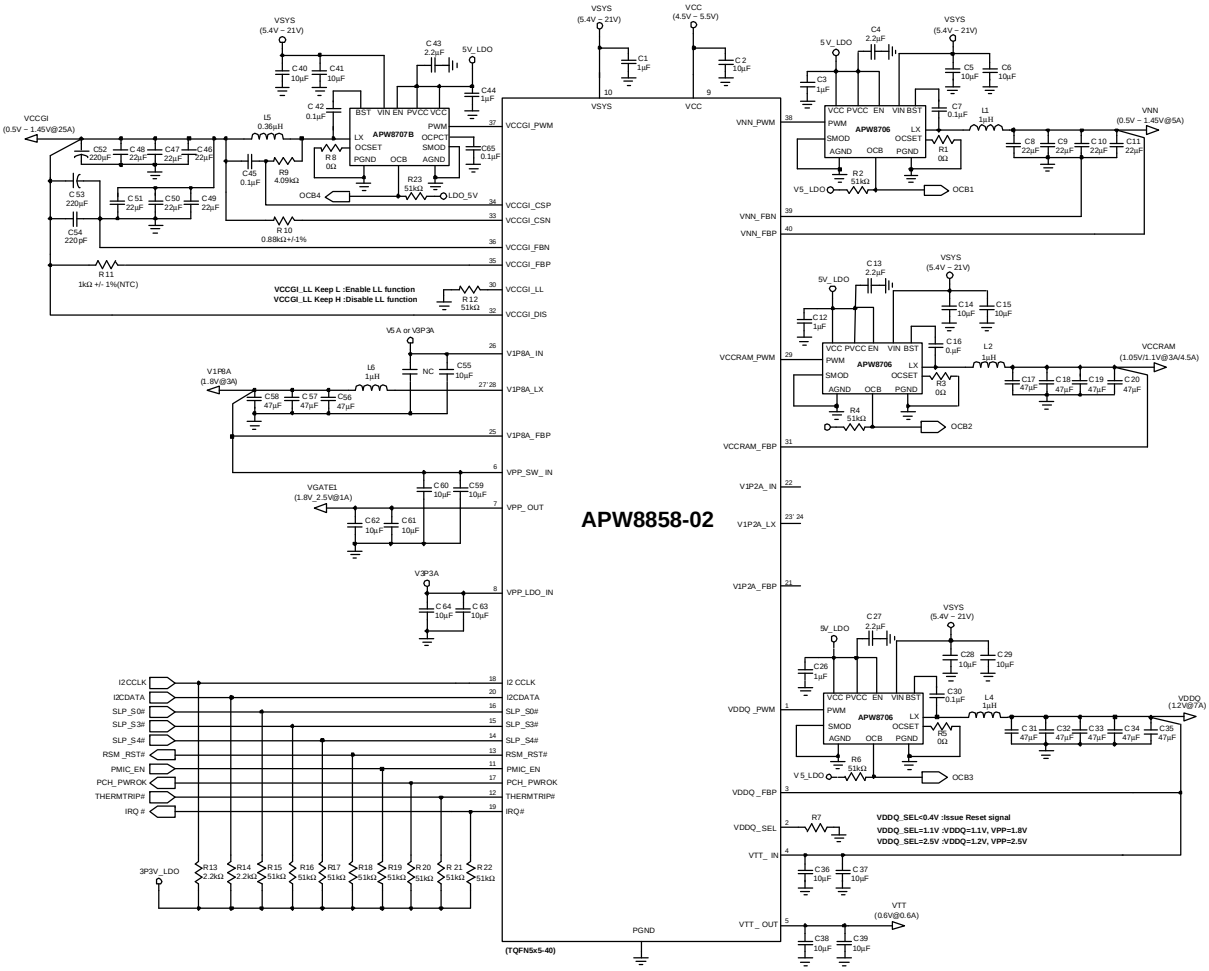
10.1 Typical Application Circuit



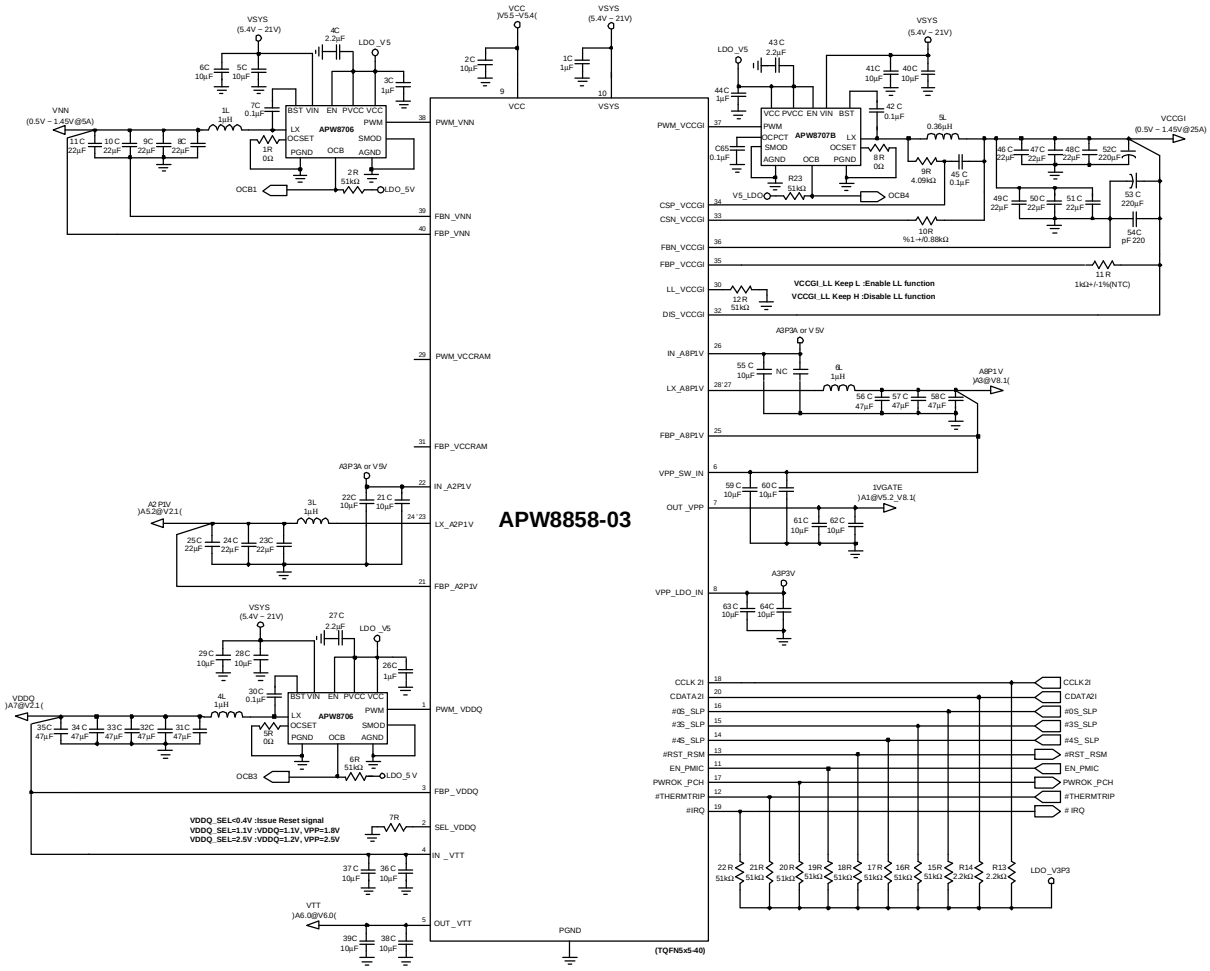
10.2 Typical Application Circuit (APW8858-01)



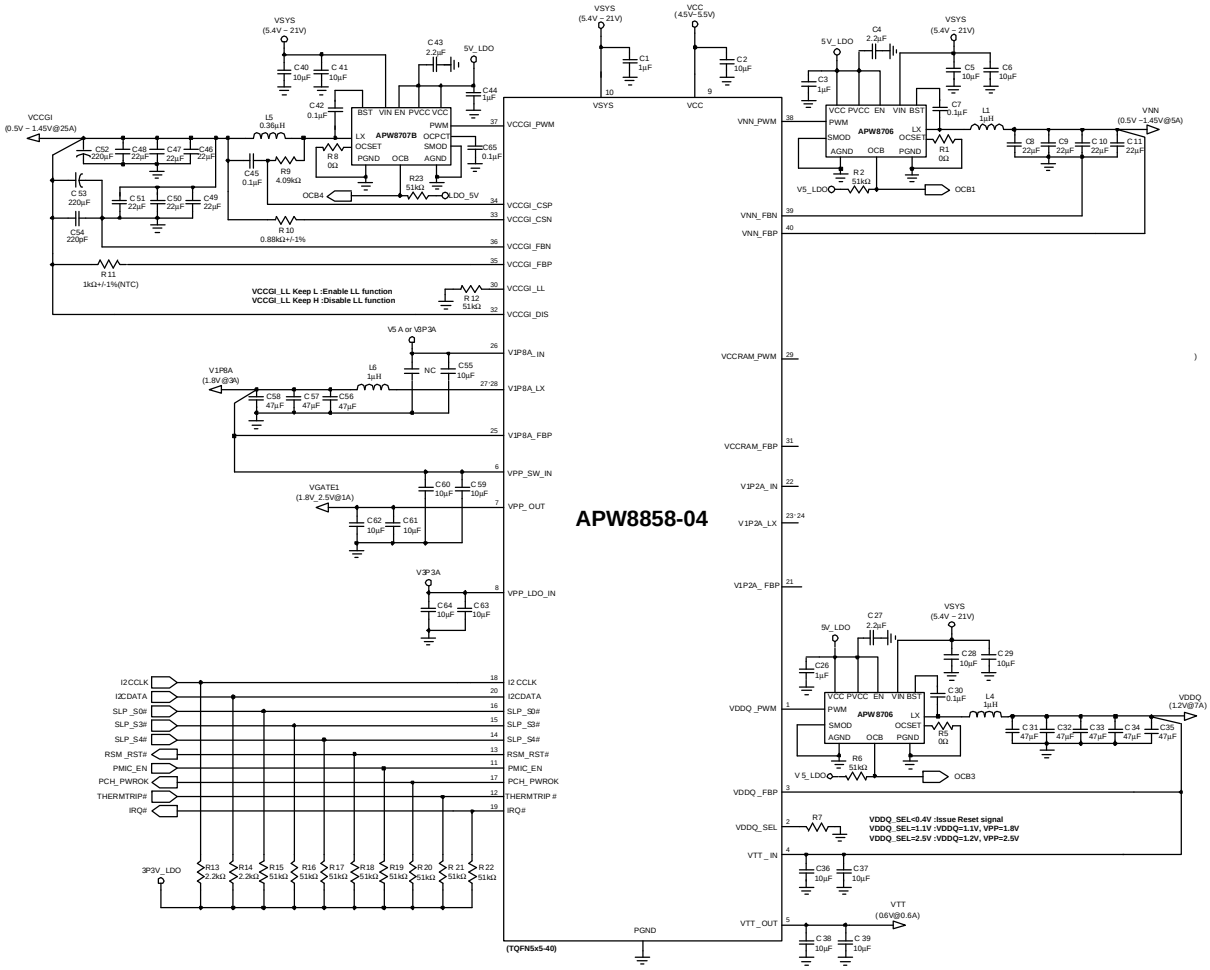
10.3 Typical Application Circuit (APW8858-02)



10.4 Typical Application Circuit (APW8858-03)



10.5 Typical Application Circuit (APW8858-04)



11. Pin Description

PIN		FUNCTION
NO.	NAME	
1	VDDQ_PWM	VDDQ PWM Signal Output Pin. Connect to External power stage's PWM input pin.
2	VDDQ_SEL	VDDQ output select pin. Connect a 1% resistor from this pin to PGND per Table 5 to select appropriate output voltage.
3	VDDQ_FBP	VDDQ Positive Output Feedback Pin. Connect to VDDQ output voltage.
4	VTT_IN	VTT Sink/Source LDO Input Pin.
5	VTT_OUT	VTT Sink/Source LDO Output Pin.
6	VPP_SW_IN	Power Input Pin for 1.8V Load Switch.
7	VPP_OUT	Output pin of 2.5V-LDO or 1.8V Load Switch.
8	VPP_LDO_IN	Power Input Pin for 2.5V LDO.
9	VCC	IC Power Input Pin.
10	VSYS	IC Power Input Pin.
11	PMIC_EN	PMIC Enable.
12	THERMTRIP#	Thermal Shutdown Input Pin.
13	RSM_RST#	Power Good Indicator. Connect a resistor from RSM_RST# to a pull-high voltage.
14	SLP_S4#	Active low signal from SOC to PMIC that indicates S4 state entry upon assertion (SLP_S4# =Low) and exit upon de-assertion (SLP_S3# =High).
15	SLP_S3#	Active low signal from SOC to PMIC that indicates S3 state entry upon assertion (SLP_S3# =Low) and exit upon de-assertion (SLP_S3# =High).
16	SLP_S0#	Active low signal from SOC to PMIC that indicates S0iX state entry upon assertion (SLP_S0# =Low) and exit upon de-assertion (SLP_S0# =High).
17	PCH_PWROK	Power Good Indicator. Connect a resistor from PCH_PWROK to a pull-high voltage.
18	I2CCLK	I2C Clock Signal Pin.
19	IRQ#	PMIC active low interrupt pin.
20	I2CDATA	I2C Data Connection Pin.
21	V1P2A_FBP	V1P2A Output Voltage Feedback Pin. Connect to V1P2A output voltage.
22	V1P2A_IN	V1P2A PWM Regulator Input Pin.
23, 24	V1P2A_LX	V1P2A PWM Regulator LX Pin. Connect to external inductor for output LC filter.
25	V1P8A_FBP	V1P8A Output Voltage Feedback Pin. Connect to V1P8A output voltage.
26	V1P8A_IN	V1P8A PWM Regulator Input Pin.
27, 28	V1P8A_LX	V1P8A PWM Regulator LX Pin. Connect to external inductor for output LC filter.
29	VCCRAM_PWM	VCCRAM PWM Signal Output Pin. Connect to external power stage's PWM input pin.
30	VCCGI_LL	Load Line Disable Mode. L: Enable Load Line Function. H: Disable Load Line Function.
31	VCCRAM_FBP	VCCRAM Output Voltage Feedback Pin. Connect to VCCRAM output voltage.
32	VCCGI_DIS	Connect to VCCGI output voltage. Internal connected a resistance to PGND for soft stop behavior requirement.
33	VCCGI_CSN	Negative Input of current sensing Amplifier. This pin combined with VCCGI_CSP senses the inductor current through an RC network.
34	VCCGI_CSP	Positive Input of current sensing Amplifier. This pin combined with VCCGI_CSN senses the inductor current through an RC network.

11. Pin Description (Cont.)

PIN		FUNCTION
NO.	NAME	
35	VCCGI_FBP	VCCGI Output Voltage Feedback Pin and Load Line (Droop) Setting. Connect a resistor between this pin and VCCGI to set the droop.
36	VCCGI_FBN	VCCGI Negative Output Feedback Pin. Connect to ground.
37	VCCGI_PWM	VCCGI PWM Signal Output Pin. Connect to External power stage's PWM input pin.
38	VNN_PWM	VNN PWM Signal Output Pin. Connect to External power stage's PWM input pin.
39	VNN_FBN	VNN Negative Output Feedback Pin. Connect to ground.
40	VNN_FBP	VNN Output Voltage Feedback Pin. Connect to VNN output voltage.
Exposed Pad	PGND	IC Power Ground.

12. Electrical Characteristics

12.1 Regulator Table

Table 1. PWM Controllers VR1, VR2, VR3, VR6

Symbol	Parameter	VR1(VNN)	VR2(VCCGI)	V3(VCCRAM)	VR6(VDDQ\)	Unit
V_{IN}	Input Voltage	V_{VSYS}	V_{VSYS}	V_{VSYS}	V_{VSYS}	V
V_{OUT}	Default Output Voltage	1.05	0	1.05	1.1/1.15/1.2/1.35 selected by VDDQ_SEL	V
	Output Voltage Range	0.5 ~ 1.45	0.5 ~ 1.45	1.05 ~ 1.1		
I_{OUT}	Continuous Output Current	–	13	3	–	A
I_{PEAK}	Peak Output Current	5	25	4.5	7	A
C_{IN}	Input Capacitor (Note 4)	14	14	14	14	µF
C_{OUT}	Output Capacitor(Note 4)	62	282	62	103	µF
ESR	Output Capacitor ESR	6	6	6	6	mΩ
L	Output Inductor	1	0.36	1	1	µH
DCR	Output Inductor DCR	<10	<10	<10	<10	mΩ

Table 2. PWM Converter VR4, VR5

Symbol	Parameter	VR4(V1P8A)	VR5(V1P2A)	Unit
V_{IN}	Input Voltage	V_{V5A} or V_{V3P3A}	V_{V5A} or V_{V3P3A}	V
V_{OUT}	Default Output Voltage	1.8	1.2	V
	Output Voltage Range	1.8 ~ 1.88	1.1 ~ 1.2	
I_{OUT}	Continuous Output Current	–	–	A
I_{PEAK}	Peak Output Current	3	2.5	A
C_{IN}	Input Capacitor (Note 4)	7	7	µF
C_{OUT}	Output Capacitor (Note 4)	42	31	µF
ESR	Output Capacitor ESR	6	6	mΩ
L	Output Inductor	1	1	µH
DCR	Output Inductor DCR	<15	<15	mΩ

Table 3. LDO Regulators VR7(VTT), VR8 (V25U) and Load Switch VR8(V18U)

Symbol	Parameter	VR7 (VTT)	VR8 (VPP)	Unit
V_{IN}	Input Voltage	V_{VDDQ}	V_{V1P8A} / V_{V3P3A}	V
V_{OUT}	Default Output Voltage	1/2*VDDQ	1.8 or 2.5 selected by VDDQ_SEL	V
	Output Voltage Range	0.6		
I_{OUT}	Continuous Output Current	0.6	1	A
C_{IN}	Input Capacitor	2 x 10	2 x 10	µF
C_{OUT}	Output Capacitor	2 x 10	2 x 10	µF

Note 4: Users should take non-ideal factors of capacitor into consideration when deploying capacitors. Examples of non-ideal factors are: variations over voltage and temperature, degrade over time, tolerance in manufacturing. After taking these non-ideal factors into account, the remained values should be greater than the values indicated in the tables above. Typical values please refer to Typical Application Circuit.

12.2 [V1] VNN Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VNN} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V1)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Tolerance In PFM mode	I_{OUT}<10mA, V_{OUT}=0.6V, L, COUT conditions refer to Typicial Application Circuit,	-20	5	40	mV
	Output Voltage Tolerance In PWM mode	I_{OUT}=6A, V_{OUT}=0.6V L, COUT conditions refer to Typicial Application Circuit	-15	-	15	mV
	Transient Drop Voltage	V_{VNN}=1.05V, I_{OUT}=1.5A~5A, tr=1000ns, L, COUT conditions refer to Typicial Application Circuit	-	-	35	mV
	Transient Overshoot Voltage	V_{VNN}=1.05V, I_{OUT}=5A~1.5A, tf=1000ns, L, COUT conditions refer to Typicial Application Circuit	-	-	35	mV
V_DC(1%)	Output Voltage Accuracy	T_A= 25°C, V_{VNN} = 1.05V	-1	-	1	%
	Output Voltage Load Regulation	V_{VCC} = 5V, V_{VSYS} = 5V, I_{OUT}=1.5A to 5A (-1mV/A)	-	3.5	-	mV
	Output Voltage Line Regulation	V_{VCC} = 5V, V_{VSYS} = 5.6V to 21V,, I_{OUT}=1A (0.4mV/V)	-	6.2	-	mV
	Output Voltage Temperature Regulation	V_{VCC} = 5V, V_{VISYS} = 12.6V, I_{OUT}=0.5A, T_A= -40~85°C (| 0.2 | mV/10°C)	-	2.5	-	mV
	Output Voltage Dynamic Voltage Scaling And Soft-start Ramp Up Slew Rate	VNN_SLEW[1:0]=00h (default)	-	3.125	-	mV/µs
		VNN_SLEW[1:0]=01h	–	6.25	–	mV/µs
		VNN_SLEW[1:0]=10h	–	12.5	–	mV/µs
		VNN_SLEW[1:0]=10h	–	25	–	mV/µs
	Output Voltage Dynamic Voltage Scaling Slew Rate Accuracy	V_{VCC} = 4.5V ~ 5.5V, T_A= -40 ~ 85°C	–20	-	20	%
	Output Voltage Soft-start Delay Time	Delay time, from enable command to start ramping up	–	0	–	ms
	Output Discharge Resistance	BUCK1_DIS[1:0]=01h (default)	–	100	150	Ω
		BUCK1_DIS[1:0]=10h	–	200	–	Ω
		BUCK1_DIS[1:0]=11h	–	500	–	Ω
		BUCK1_DIS[1:0]=00h	1	–	–	kΩ
	Feedback Leakage Current	V_{VNN_FBP} = 5.5V, or V_{VNN_FBN} = 0V	-100	–	100	nA

12.2 [V1] VNN Electrical Characteristics (Cont.)

These specifications apply over V_{VCC} = 5V, V_{VNN} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V1)			Unit
			Min	Typ	Max	
PWM GATE DRIVER						
	Switching Frequency	VNN_FSW_SEL[1:0]=00h (default)	-	600	-	kHz
		VNN_FSW_SEL[1:0]=01h	-	300	-	kHz
		VNN_FSW_SEL[1:0]=10h	-	500	-	kHz
		VNN_FSW_SEL[1:0]=11h	-	800	-	kHz
	Switching Frequency Accuracy	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V	-10	–	10	%
	Minimum Off Time	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V	–	200	230	ns
	Minimum Controllable On Time	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V	–	100	130	ns
	PWM Sink Resistance	V_{VCC} =5V	–	15	20	Ω
	PWM Source Resistance	V_{VCC} =5V	–	15	20	Ω
	VNN_PWM Leakage Current	V_{VNN_PWM}=5.5V	–		100	nA
PROTECTION						
	Under-voltage Protection (UVP)	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} = 5.4~21V	65	70	75	%
	UVP Debounce TIme		-	25	-	µs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} = 5.4~21V	120	130	135	%
	OVP Debounce Time			2	-	µs
	OTP Protection	The second phase, junction temperature	-	150	-	℃
EFFICIENCY						
	Quiescent Current of VNN	IOUT=0A, PFM	-	25	50	µA
		V_{VNN} =1.05V, I_{OUT} = 5A	-	80	-	%
	Efficiency of VNN	V_{SYS} =12.6V, V_{OUT} =0.8V, I_{OUT} = 100mA ~ 300mA	80	-	-	%

12.3 [V2] VCCGI Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VCCGI} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V2)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Tolerance In PFM mode	I_{OUT}<10mA, V_{VCCGI}=0.75V, L, COUT conditions refer to Typicial Application Circuit,	-20	5	40	mV
	Output Voltage Tolerance In PWM mode	I_{OUT}=25A L, COUT conditions refer to Typicial Application Circuit	-15	-	15	mV
	Transient Drop Voltage	V_{VCCGI}=1V, I_{OUT}=1A~25A, tr=1000ns, L, COUT conditions refer to Typicial Application Circuit	-	-	50	mV
	Transient Overshoot Voltage	V_{VCCGI}=1V, I_{OUT}=25A~1A, tf=1000ns, overshoot duration≦50s,L, COUT conditions refer to Typicial Application Circuit	-	-	100	mV
V_DC(1%)	Output Voltage Accuracy	T_A = 25°C, V_{VCCGI} = 15V	-1	-	1	%
	Output Voltage Load Regulation	V_{VCC} = 5V, V_{VSYS} = 5V, I_{OUT}=1A to 25A (-1mV/A)	-	24	-	mV
	Output Voltage Line Regulation	V_{VCC} = 5V, V_{VSYS} = 5.6V to 21V, I_{OUT}=1A (0.4mV/V)	-	6.2	-	mV
	Output Voltage Temperature Regulation	V_{VCC} = 5V, V_{VIN} = 5V, I_{OUT}=0.5A, T_A = -40~85°C (｜0.2｜mV/10°C)	-	2.5	-	mV
	Output Voltage Tolerance	V_{VSYS} = 12.6V, V_{VCCGI}=1V, I_{OUT}= 25A, load line=0mΩ	-5	-	5	mV
	Non-zero Load Line Tolerance	V_{VSYS} = 12.6V, V_{VCCGI}=1V, I_{OUT} = 25A, load line=0~15mΩ	-20	-	20	mV
	Output Voltage Line Regulation	V_{VSYS} = 5.4V to 21V, I_{OUT}=1.3A (0.4mV/V)	-	5	-	mV
	Output Voltage Temperature Regulation	V_{VSYS} = 12.6V, I_{OUT}=1A, T_A = -40~85°C (｜0.2｜mV/10°C)	-	3	-	mV
	Output Voltage Dynamic Voltage Scaling And Soft-start Ramp Up Slew Rate	VCCGI_SLEW[1:0]=00h (default)	-	3.125	-	mV/µs
		VCCGI_SLEW[1:0]=01h	–	6.25	–	mV/µs
		VCCGI_SLEW[1:0]=10h	–	12.5	–	mV/µs
		VCCGI_SLEW[1:0]=10h	–	25	–	mV/µs
	Output Voltage Dynamic Voltage Scaling Slew Rate Accuracy	V_{VCC} = 4.5V ~ 5.5V, T_A = -40 ~ 85°C	–20	-	20	%
	Output Voltage Soft-start Delay Time	Delay time, from enable command to start ramping up	–	0	-	ms
	Output Discharge Resistance	BUCK2_DIS[1:0]=01h (default)	–	100	150	Ω
		BUCK2_DIS[1:0]=10h	–	200	–	Ω
		BUCK2_DIS[1:0]=11h	–	500	–	Ω

12.3 [V2] VCCGI Electrical Characteristics (Cont.)

These specifications apply over V_{VCC} = 5V, V_{VCCGI} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V2)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE(CONT.)						
	Output Discharge Resistance	BUCK2_DIS[1:0]=00h	1	–	–	kΩ
	Feedback Leakage Current	V_{VCCGI_FBP} = 5.5V, or V_{VCCGI_FBN} = 0V	-100	-	100	nA
PWM GATE DRIVER						
	Switching Frequency	VCCGI_FSW_SEL[1:0]=00h (default)	-	600	-	kHz
		VCCGI_FSW_SEL[1:0]=01h	-	300	-	kHz
		VCCGI_FSW_SEL[1:0]=10h	-	500	-	kHz
		VCCGI_FSW_SEL[1:0]=11h	-	800	-	kHz
	Switching Frequency Accuracy	V_{VCC} = 4.5 ~ 5.5V, V_{VSYS} =5.4~21V	-10	-	10	%
	Minimum Off Time	V_{VCC} = 4.5 ~ 5.5V, V_{VSYS} =5.4~21V	-	200	230	ns
	Minimum Controllable On Time	V_{VCC} = 4.5 ~ 5.5V, V_{VSYS} =5.4~21V	-	100	130	ns
	PWM Sink Resistance	V_{VCC} = 5V	-	15	20	Ω
	PWM Source Resistance	V_{VCC} = 5V	-	15	20	Ω
	VCCGI PWM Leakage Current	V_{VCCGI_PWM}=5.5V	-	-	100	nA
LOAD LINE						
	Load Line Range		0	–	15	mΩ
Scott spec	Input Offset Voltage Between VCCGI_CSP and VCCGI_CSN	All temperature and voltage range	-5	–	5	mV
PROTECTION						
	Under-voltage Protection (UVP)	V_{VCC} =4.5 ~5.5V	65	70	75	%
	UVP Debounce TIme		-	25	-	µs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC} =4.5 ~5.5V	120	130	135	%
	OVP Debounce TIme		-	2	-	µs
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, IOUT=0A, PFM	-	25	50	µA
		V_{IN} =12.6V, V_{OUT} =1V, I_{OUT} = 250mA ~ 3000mA	85	-	-	%
		V_{IN} =12.6V, V_{OUT} =0.6V, I_{OUT} = 15mA ~ 55mA	65	-	-	%
		V_{IN} =12.6V, V_{OUT} =1V, I_{OUT} = 25A	-	75	-	%

12.4 [V3] VCCRAM Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VCCRAM} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V3)			Unit
			Min	Typ	Max	
PWM CONTROLLER						
	Switching Frequency	VCCRAM_FSW_SEL[1:0]=00h	-	600	-	kHz
		VCCRAM_FSW_SEL[1:0]=01h	-	300	-	kHz
		VCCRAM_FSW_SEL[1:0]=10h	-	500	-	kHz
		VCCRAM_FSW_SEL[1:0]=11h (default)	-	800	-	kHz
	Switching Frequency Accuracy	V_{VCC} =4.5 ~5.5V, V_{VSYS} =5.4~21V	-10	-	10	%
	Minimum Off Time	V_{VCC} = 4.5 ~ 5.5V, V_{VSYS} =5.4~21V	-	200	230	ns
	Minimum Controllable On Time	V_{VCC} = 4.5 ~ 5.5V, V_{VSYS} =5.4~21V	-	100	130	ns
	PWM Sink Resistance	V_{VCC} = 5V	-	15	20	Ω
	PWM Source Resistance	V_{VCC} = 5V	-	15	20	Ω
	VCCGI PWM Leakage Current	V_{VCCGI_PWM}=5.5V	-	-	100	nA
PWM OUTPUT VOLTEGE						
	Output Voltage Tolerance In PFM mode	V_{OUT}=1.05V , I_{OUT}<10mA, L, COUT conditions refer to Typicial Application Circuit	-20	5	20	mV
	Output Voltage Tolerance In PWM mode	V_{OUT}=1.05V ,I_{OUT}=3A~4.5A, L, COUT conditions refer to Typicial Application Circuit	-20	-	20	mV
V_DC(1%)	Output Voltage Accuracy	T_A= 25°C, V_{VCCRAM}= 1.05V	-1	-	1	%
	Output Voltage Load Regulation	V_{VCC} = 5V, V_{VIN} = 5V, I_{OUT}=0.5A to 4.5A (-1mV/A)	-	4	-	mV
	Output Voltage Line Regulation	V_{VCC} = 5V, V_{VIN} = 3.3V to 5V, I_{OUT}=0.5A (0.4mV/V)	-	0.7	-	mV
	Output Voltage Temperature Regulation	V_{VCC} = 5V, V_{VIN} = 5V, I_{OUT}=0.5A, T_A = -40~85°C (| 0.2 | mV/10°C)	-	1.3	-	mV
V_AC(4%)	Load Transient Drop Voltage	Tr=2.5A/µs, I_{OUT}=1A~3A and 1.35A~4.5A, L, COUT conditions refer to Typicial Application Circuit	-	-	40	mV
	Load Transient Overshoot Voltage	Tf=2.5A/µs, I_{OUT}=3A~1A and 4.5A~1.35A, L, COUT conditions refer to Typicial Application Circuit	-	-	40	mV
	Output Step Ramp Rate (DVS)	VCCRAM_SLEW[1:0]=00h (default)	-	10	-	mV/µs
		VCCRAM_SLEW[1:0]=01h	-	15	-	mV/µs
		VCCRAM_SLEW[1:0]=10h	-	20	-	mV/µs

12.4 [V3] VCCRAM Electrical Characteristics (Cont.)

These specifications apply over V_{VCC} = 5V, V_{VCCRAM} = 1.05V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V3)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTEGE						
		VCCRAM_SLEW[1:0]=11h	-	25	-	mV/μs
	Output Step Ramp Rate Accuracy	V_{VCC} = 5V, V_{VIN} = 5V	-10	-	10	%
	Output Voltage Soft-start Ramp Up Time	VCCRAM_RAMP[1:0]=00h (default)	-	1.25	-	ms
		VCCRAM_RAMP[1:0]=01h	-	5	-	ms
		VCCRAM_RAMP[1:0]=10h	-	10	-	ms
		VCCRAM_RAMP[1:0]=11h	-	20	-	ms
	Output Voltage Soft-start Ramp Up Time Accuracy		-10	-	10	%
	Output Discharge Resistance	BUCK3_DIS[1:0]=01h (default)	–	100	150	Ω
		BUCK3_DIS[1:0]=10h	–	200	–	Ω
		BUCK3_DIS[1:0]=11h	–	500	–	Ω
		BUCK3_DIS[1:0]=00h	1	–	–	kΩ
	Feedback Leakage Current	V_{VCCRAM_FBP} = 5.5V, or V_{CCRAM_FBN}=0V	-100	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)	V_{VCC}= 4.5 ~ 5.5V	65	70	75	%
	UVP Debounce TIme		-	25	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC}= 4.5 ~ 5.5V	120	130	135	%%
	OVP Debounce TIme			2	-	μs
		The second phase, junction temperature Rising	-	150	-	℃
		Hysteresis	-	50	-	
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, IOUT=0A, PFM	-	25	50	μA
		V_{SYS}=5V, V_{OUT}=1.05V, I_{OUT}=40 ~ 80mA	83	-	-	%
		V_{SYS}=5V, V_{OUT}=1.05V, I_{OUT}=3 ~ 4.5A	-	80	-	%

12.5 [V4] V1P8A Electrical Characteristics

These specifications apply over V_{1P8A_IN}= 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8858(V4)			Unit
				Min	Typ	Max	
PWM CONTROLLER							
	Switching Frequency	V_{VCC}=5V, V_{VSYS}=8.4V	V1P8A_FSW_SEL[1:0]=00h	-	3	-	MHz
			V1P8A_FSW_SEL[1:0]=01h (default)	1.8	2	2.2	MHz
			V1P8A_FSW_SEL[1:0]=10h	-	1	-	MHz
			V1P8A_FSW_SEL[1:0]=11h	-	4	-	MHz
	Switching Frequency Accuracy	V_{VCC}=4.5 ~5.5V, V_{VSYS}=5.4~21V		-10	-	10	%
	Maximum Duty Cycle			100	-	-	%
	Minimum Controllable On Time			-	60	80	ns
	High-side MOSFET On Resistance	V_{V1V8_IN}=3.3V		-	55	-	mΩ
	Low-side MOSFET On Resistance	V_{V1V8_IN}=3.3V		-	40	-	mΩ
	Input Leakage Current	V8 is off, $V_{V1.8A\_IN}$=5.5V		-	-	1	µA
	LX Leakage Current	$V_{V1.8A\_LX}$=5.5V, V_{V1V8_IN}=5.5V		-	-	1	µA
	Zero Current Offset			-10	-	4	mV
	PFM Current Limit	Vin=3.3V, Vout=1.8V, Fsw=2MHz		-	0.5	-	A
PWM OUTPUT VOLTEGE							
	Output Voltage Tolerance In PFM mode	V_{OUT}=1.8V , I_{OUT}=50mA, L, COUT conditions refer to Typicial Application Circuit		-	5	18	mV
	Output Voltage Tolerance In PWM mode	V_{OUT}=1.8V ,I_{OUT}=3A, L, COUT conditions refer to Typicial Application Circuit		-	-	18	mV
V_DC(1%)	Output Voltage Accuracy	T_A= 25°C, V_{OUT}=1.8V		-0.8	-	0.8	%
	Output Voltage Load Regulation	V_{V1V8_IN}=3.3V, I_{OUT}=0.5A to 3A (-1mV/A)		-	2.5	-	mV
	Output Voltage Line Regulation	V_{V1V8_IN}=3.3V to 5V, I_{OUT}=0.5A (0.4mV/V)		-	0.7	-	mV
	Output Voltage Temperature Regulation	V_{V1V8_IN}=3.3V, I_{OUT}=0.5A, T_A= -40~85°C (| 0.2 | mV/10°C)		-	2.5	-	mV
V_AC(4%)	Load Transient Drop Voltage	Tr=2.5A/µs, I_{OUT}=0.9A to 3A, Refer to the typical circuit		-	-	72	mV
	Load Transient Overshoot Voltage	Tf=2.5A/µs, I_{OUT}=3A to 0.9A, Refer to the typical circuit		-	-	72	mV
	Output Step Ramp Rate (DVS)		V1P8A_SLEW[1:0]=00h (default)	-	10	-	mV/µs
			V1P8A_SLEW[1:0]=01h	-	15	-	mV/µs
			V1P8A_SLEW[1:0]=10h	-	20	-	mV/µs

12.5 [V4] V1P8A Electrical Characteristics (Cont.)

These specifications apply over V_{1P8A_IN}= 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8858(V4)			Unit
				Min	Typ	Max	
PWM OUTPUT VOLTEGE (CONT.)							
		V1P8A_SLEW[1:0]=11h		-	25	-	mV/μs
	Output Step Ramp Rate Accuracy			-10	-	10	%
	Output Voltage Soft-start Ramp Up Time	Delay time, from enable command to start ramping up	V1P8A_RAMP[1:0]=00h (default)	-	1.25	-	ms
			V1P8A_RAMP[1:0]=01h	-	10	-	ms
			V1P8A_RAMP[1:0]=10h	-	20	-	ms
			V1P8A_RAMP[1:0]=11h	-	40	-	ms
	Output Voltage Soft-start Ramp Up Time Accuracy			-10	-	10	%
	Output Discharge Resistance	BUCK4_DIS[1:0]=01h (default)		–	100	150	Ω
		BUCK4_DIS[1:0]=10h		–	200	–	Ω
		BUCK4_DIS[1:0]=11h		–	500	–	Ω
		BUCK4_DIS[1:0]=00h		1	–	–	kΩ
	Feedback Leakage Current	V_{V1V8_FBP} = 5.5V		-	-	100	nA
PROTECTION							
	Under-voltage Protection (UVP)	V_{VCC}= 4.5 ~ 5.5V		65	70	75	%
	UVP Debounce Time			-	25	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%		-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC}= 4.5 ~ 5.5V		120	130	135	%%
	OVP Debounce Time				2	-	μs
I_{OCP4}	High-side MOSFET Over-current-Protection(OCP)	V_{VCC}= 4.5 ~ 5V		3.5	4	4.5	A
	OCP Debounce Time			-	2	-	μs
	Thermal Shutdown Protection	The first phase, junction temperature Rising		-	120	-	°C
		Hysteresis		-	20	-	°C
		The second phase, junction temperature Rising		-	150	-	°C
		Hysteresis		-	50	-	°C
EFFICIENCY							
	Efficiency (Refer to the typical circuit)	Quiescent Current, I_{OUT}=0A, PFM		-	25	50	μA
		V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=15mA, SOiX mode, total power loss		-	3.92	-	mW
		V_{SYS}=5V, V_{OUT}=1.8V, I_{OUT}=50 ~ 100mA		-	90	-	%
		V_{SYS}=5V, V_{OUT}=1.8V, I_{OUT}=1.5 ~ 3A		-	85	-	%

12.6 [V5] V1P2A Electrical Characteristics

These specifications apply over V_{1P2A_IN}= 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8858(V5)			Unit
				Min	Typ	Max	
PWM CONTROLLER							
	Switching Frequency	V_{VCC} =5V, V_{VSYS} =8.4V	V1P2A_FSW_SEL[1:0]=00h		3		MHz
			V1P2A_FSW_SEL[1:0]=01h (default)	1.8	2	2.2	MHz
			V1P2A_FSW_SEL[1:0]=10h		1		
			V1P2A_FSW_SEL[1:0]=11h		4		
	Switching Frequency Accuracy	V_{VCC} =4.5 ~5.5V, V_{VSYS} =5.4~21V		-10	-	10	%
	Maximum Duty Cycle			100	-	-	%
	Minimum Controllable On Time			-	60	80	ns
	High-side MOSFET On Resistance	V_{V1V8_IN}=3.3V		-	55	-	mΩ
	Low-side MOSFET On Resistance	V_{V1V8_IN}=3.3V		-	40	-	mΩ
	Input Leakage Current	V8 is off, $V_{V1.8A\_IN}$=5.5V		-	-	1	µA
	LX Leakage Current	$V_{V1.8A\_LX}$ =5.5V, $V_{V1V.8\_IN}$=5.5V		-	-	1	µA
	Zero Current Offset			-10	-	4	mV
	PFM Current Limit	V_{IN}=3.3V, V_{OUT}=1.8V, F_{SW}=2MHz		-	0.5	-	A
PWM OUTPUT VOLTEGE							
	Output Voltage Tolerance In PFM mode	V_{OUT}=1.2V , I_{OUT}=10mA, L, C_{OUT} conditions refer to Typicial Application Circuit		-	5	12	mV
	Output Voltage Tolerance In PWM mode	V_{OUT}=1.2V ,I_{OUT}=2.5A, L, COUT conditions refer to Typicial Application Circuit		-	-	12	mV
V_DC(1%)	Output Voltage Accuracy	T_A = 25°C, V_{OUT}=1.2V		-0.8	-	0.8	%
	Output Voltage Load Regulation	V_{V1P2A_IN} =3.3V, I_{OUT}=0.5A to 2.5A (-1mV/A)		-	2	-	mV
	Output Voltage Line Regulation	V_{V1P2A_IN} =3.3V to 5V, I_{OUT}=0.5A (0.4mV/V)		-	0.7	-	mV
	Output Voltage Temperature Regulation	V_{V1P2A_IN} =3.3V, I_{OUT}=0.5A, T_A = -40~85°C (| 0.2 | mV/10°C)		-	1.3	-	mV
V_AC(4%)	Load Transient Drop Voltage	Tr=2.5A/µs, I_{OUT}=0.75A to 2.5A, Refer to the typical circuit		-	-	48	mV
	Load Transient Overshoot Voltage	Tf=2.5A/µs, I_{OUT}=2.5A to 0.75A, Refer to the typical circuit		-	-	48	mV

12.6 [V5] V1P2A Electrical Characteristics (Cont.)

These specifications apply over V_{1P2A_IN}= 5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V5)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTEGE (Cont.)						
	Output Step Ramp Rate (DVS)	V1P2A_SLEW[1:0]=00h (default)	-	10	-	mV/μs
		V1P2A_SLEW[1:0]=01h	-	15	-	mV/μs
		V1P2A_SLEW[1:0]=10h	-	20	-	mV/μs
		V1P2A_SLEW[1:0]=11h	-	25	-	mV/μs
	Output Step Ramp Rate Accuracy		-10	-	10	%
	Output Voltage Soft-start Ramp Up Time	V1P2A_RAMP[1:0]=00h (default)	-	1.25	-	ms
		V1P2A_RAMP[1:0]=01h	-	10	-	ms
		V1P2A_RAMP[1:0]=10h	-	20	-	ms
		V1P2A_RAMP[1:0]=11h	-	40	-	ms
	Output Voltage Soft-start Ramp Up Time Accuracy		-10	-	10	%
	Output Discharge Resistance	BUCK5_DIS[1:0]=01h (default)	-	100	150	Ω
		BUCK5_DIS[1:0]=10h	-	200	-	Ω
		BUCK5_DIS[1:0]=11h	-	500	-	Ω
		BUCK5_DIS[1:0]=00h	1	-	-	kΩ
	Feedback Leakage Current	V_{V1V2_FBP} = 5.5V	-	-	100	nA
PROTECTION						
	Under-voltage Protection (UVP)	V_{VCC}= 4.5 ~ 5.5V	65	70	75	%
	UVP Debounce TIme		-	25	-	μs
	UVP enable delay time	Extend time when regulate voltage reach 100%,	-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC}= 4.5 ~ 5.5V	120	130	135	%%
	OVP Debounce TIme			2	-	μs
I_{OCP3}	High-side MOSFET Over-current-Protection(OCP)	V_{V1V8_IN} =3.3V	3.5	4	4.5	A
	OCP Debounce TIme		-	2	-	μs
	Thermal Shutdown Protection	The first phase, junction temperature Rising	-	120	-	°C
		Hysteresis	-	20	-	°C
		The second phase, junction temperature Rising	-	150	-	°C
		Hysteresis	-	50	-	°C
EFFICIENCY						
	Efficiency (Refer to the typical circuit)	Quiescent Current, IOUT=0A, PFM	-	25	50	μA
		VIN=3.3V, VOUT=1.2V, IOUT=3mA, S0iX mode, total power loss	-	0.95	-	mW
		VSYS=5V, VOUT=1.2V, IOUT=10 ~ 50mA	-	84	-	%
		VSYS=5V, VOUT=1.2V, IOUT=1.5 ~ 2.5A	-	80	-	%

12.7 [V6] VDDQ Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VDDQ} = 1.1V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V6)			Unit
			Min	Typ	Max	
PWM OUTPUT VOLTAGE						
	Output Voltage Tolerance In PFM mode	I_{OUT}=150mA, V_{VDDQ}=1.1V, L, COUT conditions refer to Typicial Application Circui	-	5	22	mV
	Output Voltage Tolerance In PWM mode	I_{OUT}=7A, V_{VDDG}=1.1V, L, COUT conditions refer to Typicial Application Circuit	-	-	22	mV
	Transient Drop Voltage	V_{VDDQ}=1.1V, I_{OUT}=2.1A~7A, tr=2.5A/µs	-	-	44	mV
	Transient Overshoot Voltage	V_{VDDQ}=1.1V, I_{OUT}=7A~2.1A, tf=2.5A/µs	-	-	44	mV
V_DC(1%)	Output Voltage Accuracy	T_A = 25°C, V_{OUT}=1.05V	-0.8	-	0.8	%
	Output Voltage Load Regulation	V_{IN}=8.4V, I_{OUT}=1A to 5A (-1mV/A)	–	4	–	mV
	Output Voltage Line Regulation	V_{IN}=8.4V to 21V, I_{OUT}=1A (0.4mV/V)	–	5	–	mV
	Output Voltage Temperature Regulation	V_{IN}=8.4V, I_{OUT}=1A, T_A = -40~85°C (| 0.2 | mV/10°C)	–	2.7	–	mV
	Output Step Ramp Rate (DVS)	VDDQ_SLEW[1:0]=00h (default)	-	10	-	mV/µs
		VDDQ_SLEW[1:0]=01h	-	15	-	mV/µs
	Output Step Ramp Rate (DVS)	VDDQ _SLEW[1:0]=10h	-	20	-	mV/µs
		VDDQ_SLEW[1:0]=11h	-	25	-	mV/µs
	Output Step Ramp Rate Accuracy		-10	-	10	%
	Output Voltage Soft-start Ramp Up Time	VDDQ_RAMP[1:0]=00h (default)	-	1.25	-	ms
		VDDQ _RAMP[1:0]=01h	-	5	-	ms
		VDDQ _RAMP[1:0]=10h	-	10	-	ms
		VDDQ _RAMP[1:0]=11h	-	20	-	ms
	Output Voltage Soft-start Ramp Up Time Accuracy		-10	-	10	%
	Output Discharge Resistance	BUCK6_DIS[1:0]=01h (default)	–	100	150	Ω
		BUCK6_DIS[1:0]=10h	-	200	-	Ω
		BUCK6_DIS[1:0]=11h	-	500	-	Ω
		BUCK6_DIS[1:0]=00h	1	-	-	kΩ
	Feedback Leakage Current	V_{VNN_FBP} = 5.5V	–	–	100	nA

12.7 [V6] VDDQ Electrical Characteristics (Cont.)

These specifications apply over V_{VCC} = 5V, V_{VDDQ} = 1.1V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8858(V6)			Unit
				Min	Typ	Max	
PWM GATE DRIVER							
	Switching Frequency	V_{VCC} = 5V, V_{SYS} =8.4V	VDDQ_FSW_SEL[1:0]=00h (default)	-	600	-	kHz
			VDDQ_FSW_SEL[1:0]=01h	-	300	-	kHz
			VDDQ_FSW_SEL[1:0]=10h	-	500	-	kHz
			VDDQ_FSW_SEL[1:0]=11h	-	800	-	kHz
	Switching Frequency Accuracy	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V		-10	–	10	%
	Minimum Off Time	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V		–	200	230	ns
	Minimum Controllable On Time	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} =5.4~21V		–	100	130	ns
	PWM Sink Resistance	V_{VCC} =5V		–	15	20	Ω
	PWM Source Resistance	V_{VCC} =5V		–	15	20	Ω
	VNN_PWM Leakage Current	V_{VNN_PWM}=5.5V		–		100	nA
PROTECTION							
	Under-voltage Protection (UVP)	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} = 5.4~21V		65	70	75	%
	UVP Debounce TIme			-	25	-	µs
	UVP enable delay time	Extend time when regulate voltage reach 100%		-	0	-	ms
	Over-voltage Protection (OVP)	V_{VCC} = 4.5V ~ 5.5V, V_{VSYS} = 5.4~21V		120	130	135	%
	OVP Debounce Time				2	-	µs
EFFICIENCY							
		Quiescent Current, IOUT=0A, PFM		-	25	50	µA
	Efficiency of VDDQ	V_{VDDQ} =1.1V, I_{OUT} = 5A		-	80	-	%
		V_{SYS} =12.6V, V_{VDDQ} =1.2V, I_{OUT} = 200mA ~ 1300mA		83	-	-	%
		V_{VSYS} = 8.4V, V_{VDDQ}=1.2V, IOUT=10mA, S0iX mode, total power loss			2.97		W

12.8 [V7] VPP Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VPP_OUT} = 2.5V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V7)			Unit
			Min	Typ	Max	
REGULATOR OUTPUT						
	Output Voltage Accuracy	V_{VPP_IN} = 3.3V, V_{VPP_OUT} = 2.5V, T_A = 25°C	-12.5	-	12.5	mV
	Output Voltage Load/Temperature Regulation	I_{OUT} =4.5mA to 1000mA, T_A = -40~85°C	-	12.5	-	mV
	Output Load Transient Drop Voltage	Tr=200ns, IOUT=4.5mA to 1000mA, Refer to the typical circuit	-	-	-100	mV
	Output Load Transient Overshoot Voltage	Tf=200ns, IOUT=4.5mA to 1000mA, Refer to the typical circuit	-	-	100	mV
	Dropout Voltage	I_{OUT}=700mA	-	300	-	mV
	Output Discharge Resistance	VPP_DIS[1:0]=01h (default)	-	100	150	Ω
		VPP_DIS[1:0]=10h	-	200	-	Ω
		VPP_DIS[1:0]=11h	-	500	-	Ω
		VPP_DIS[1:0]=00h	1	-	-	kΩ
	Output Noise	f=100 to 100kHz	-	100	-	μV_{RMS}
	Power-Supply Rejection Ration (PSRR)	f=10kHz	40	-	-	dB
T_{SS}	Soft-Start Time	Total time (delay+Ramp)	-	1.25	-	ms
	Current Limit	V25U LDO	-	1.2	-	A
	Under Voltage Protection (UVP)		65	70	75	%
	UVP Debounce TIme		-	2	-	µs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	0.5	-	ms
	Output Voltage Soft-start	Total time (delay+Ramp)	0.9	1	1.1	ms
SWITCH OUTPUT						
	Switch On Resistance	Powered by V1V8_FBP internally, Iout=1A	-	32	45	mΩ
T_{SS}	Soft-Start Time	Total time (delay+Ramp)	-	100	-	µs
	Over Current-Protection		2	3	4	A
	Input Leakage Current	Loss from V1V8_FBP	-	-	1	µA

12.9 [V8] VTT Electrical Characteristics

These specifications apply over V_{VTT_IN} = 1.2V, V_{VTT_OUT} = 0.6V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858(V8)			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_Q	Quiescent Current	I_{OUT}=0mA	-	25	30	µA
I_{SD}	Shutdown Current	I_{OUT}=0mA	-	-	1	µA
R_{DIS}	Output Discharge Resistance	VTT_DIS[1:0]=01h (default)	–	100	150	Ω
		VTT_DIS[1:0]=10h	–	200	–	Ω
		VTT_DIS[1:0]=11h	–	500	–	Ω
		VTT_DIS[1:0]=00h	1	–	–	kΩ
	Output Step Ramp Rate	Exit Connected Standby Mode	-	-	35	µs
T_{SS}	Soft-Start Time	Total time (delay+Ramp)	-	-	35	µs
OUTPUT VOLTAGE						
V_{OUT}	Output Voltage Range	0mA < I_{OUT} <600mA, T_A = -40~85°C, VDDQ=1.1V	522	550	578	mV
		0mA < I_{OUT} <600mA, T_A = -40~85°C, VDDQ=1.15V	546	575	604	MV
		0mA < I_{OUT} <600mA, T_A = -40~85°C, VDDQ=1.2V	570	600	630	mV
SUPPLY CURRENT						
	Output Voltage Accuracy	V_{VTT_IN} = 1.1/1.15/1.2V, 0mA < I_{OUT} <600mA, T_A= -40~85°C	-5	-	5	%
V_{TRAN}	AC Output Transient Voltage	Output voltage set to any voltage. I_{OUT} =27mA to 100mA to 27mA, t_R = t_F = 0.1µs	-	-	-	mV
PSRR	Ripple Rejection	C_{OUT} =4.7µF, I_{OUT} =100mA, f =1kHz	-	70	-	dB
		C_{OUT} =4.7µF, I_{OUT} =100mA, f =10kHz	-	63	-	dB
		C_{OUT} =4.7µF, I_{OUT} =100mA, f =100kHz	-	35	-	dB
V_{NOISE}	Output Noise	f =10 to 100kHz, C_{OUT} =4.7µF, I_{OUT} =100mA.	-	100	–	$µV_{RMS}$
DROPOUT VOLTAGE						
V_{DROP}	Dropout Voltage	V_{VTT_OUT} = 1.2V, I_{OUT} = 100mA, T_J = 25°C	-	-	-	mV
		V_{VTT_OUT} = 1.2V, I_{OUT} = 100mA, T_J = -40 to 85°C	-	-	-	mV
Current Limit Protection						
I_{LIM}	Current-Limit Level	Source and Sink, T_J = -40 to 85°C	1	-	1.5	A
	Under-voltage Protection (UVP)	V_{VTT_IN} =1.1~1.35V	40	50	60	%
	UVP Debounce TIme		-	2	-	µs
	UVP enable delay time	Extend time when regulate voltage reach 100%	-	100	-	µs

12.10 VSYS & POK & Logic Control Electrical Characteristics

These specifications apply over V_{VCC} = 5V, V_{VSYS} = 8.4V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		APW8858(VSYS&POK)			Unit
				Min	Typ	Max	
VCC UNDER VOLTAGE LOCKOUT (UVLO)							
V_{CC_UVLO}	VCC UVLO Threshold Voltage	VCC Rising		-	4	4.2	V
		VCC Falling		-	3.6	-	V
	VCC UVLO Threshold Debounce Time			-	100	-	µs
VSYS UNDER VOLTAGE LOCKOUT (UVLO)							
	VSYS UVLO Threshold Voltage	VSYS Rising, T_A = 25°C		-	5.3	5.38	V
		VSYS Falling		-	5.2	-	V
	VSYS UVLO Threshold Debounce Time			-	4	10	µs
POK							
	RSM_RST# Leakage Current	$V_{RSM\_RST\#}$=5V when RSM_RST# is de-asserted		-	0.1	1	µA
	RSM_RST# De-assertion Blanking Time	From all ANDed gate condition meet to RSM_RST# goes high (Default, OTP adjustable)		-	10	-	ms
	RSM_RST# Assertion Blanking Time	PMIC_EN go low or VOUT below 90% ro RSM_RST# goes low		-	5	10	µs
	VPCH_PWROK Threshold Voltage	VPCH_PWROK in from lower (VPCH_PWROK goes high)		84	87	90	%
		VPCH_PWROK out from normal (VPCH_PWROK goes high)		125	130	135	%
	VPCH_PWROK Leakage Current	V_{PCH_PWROK} = 5V		-	0.1	1	µA
	VPCH_PWROK Low Voltage	V_{PCH_PWROK} =4mA during de-assertion		-	-	0.6	V
	VPCH_PWROK Assertion Delay Time	All VOUTs reach their POK threshold to VPCH_PWROK assertion	PWROKDELAY[2:0]=000b	-	2.5	-	ms
			PWROKDELAY[2:0]=001b	-	5	-	ms
			PWROKDELAY[2:0]=010b	-	10	-	ms
			PWROKDELAY[2:0]=011b	-	15	-	ms
			PWROKDELAY[2:0]=100b	-	20	-	ms
			PWROKDELAY[2:0]=101b	-	50	-	ms
			PWROKDELAY[2:0]=110b	-	75	-	ms
			PWROKDELAY[2:0]=111b (Default)	-	100	-	ms
	VPCH_PWROK Assertion Delay Time Accuracy			-20	-	20	%
	VPCH_PWROK De-assertion Delay Time	SLP_S3_L H->L edge or any VOUT reaches non-POK threshold to VPCH_PWROK de-assertion		-	5	10	µs
IRQ#							
	Leakage Current	$V_{IRQ\#}$= 5V		-	0.1	1	µA
	Low Voltage	I_{SINK} =4mA		-	0.5	1	V

12.10 VSYS & POK & Logic Control Electrical Characteristics (Cont.)

These specifications apply over V_{VCC} = 5V, V_{VSYS} = 8.4V, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	APW8858 (VSYS&POK)			Unit
			Min	Typ	Max	
PMIC_EN / SLP_S0_L / SLP_S3_L / SLP_S4_L						
	Input Logic Threshold	Voltage rising	-	-	1.3	V
		Voltage falling	0.4	-	-	V
	Leakage Current	Voltage=5V	-	0.1	1	μA
t_{DCTL}	debounce time		-	2	-	μs
VDDQ_SEL						
	Input Logic Threshold 1		-	-	0.3	V
	Input Logic Threshold 2		0.55	0.6	0.65	V
	Input Logic Threshold 3		1	1.1	1.2	V
	Input Logic Threshold 4		1.5	1.65	1.8	V
	Input Logic Threshold 5		2.5	2.65	2.8	V
	Input Logic Threshold 6		3	3.15	3.3	V
	Output setting current	-40~85℃	9	10	11	μA

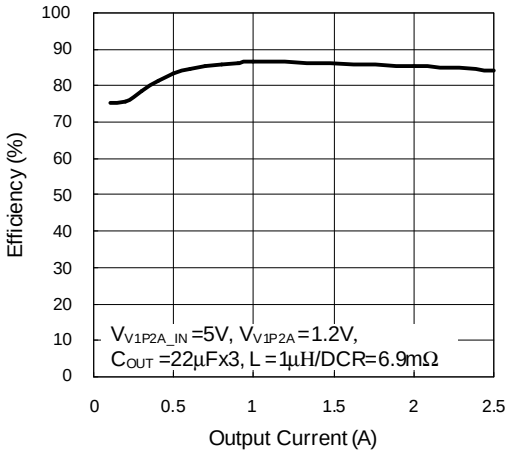
12.11 I2C Electrical Characteristics

Timing characteristics for I2C Interface signals over recommended operating conditions (unless otherwise noted).

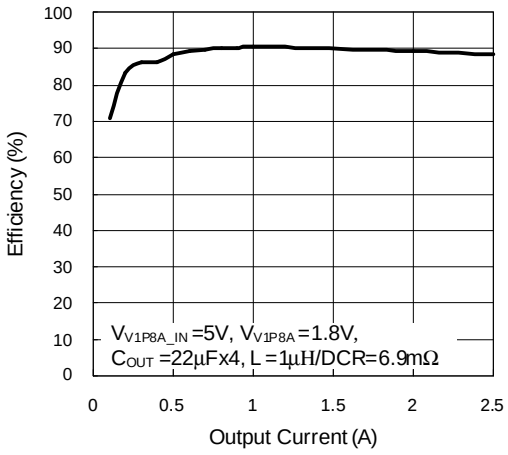
Symbol	Parameter	Fast Speed Plus		Fast Speed		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	Frequency, SCL	-	1	-	0.4	MHz
$t_{W(H)}$	Pulse Duration, SCL High	260	-	600	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low	500	-	1300	-	ns
t_r	Rise Time, SCL and SDA	-	-	20+0.1 C_L(pF)	300	ns
tf	Fall Time, SCL and SDA	1	10	20+0.1 C_L(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	10	-	100	-	ns
t_{hold1}	Hold Time, SCL to SDA	0	70	-	900	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition	500	-	1300	-	ns
t_{setup2}	Setup Time, SCL to Start Condition	500	-	-	-	ns
t_{hold2}	Hold Time, Start condition to SCL	200	-	600	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition	160	-	-	-	ns
C_L	Load Capacitance for Each Bus Line	-	100	-	400	pF
t_{VD_DATA}	Data Valid Time	-	-	-	900	ns
t_{VD_ACK}	Data Valid Acknowledge Time	-	-	-	900	ns

12.12 Typical Operating Characteristics

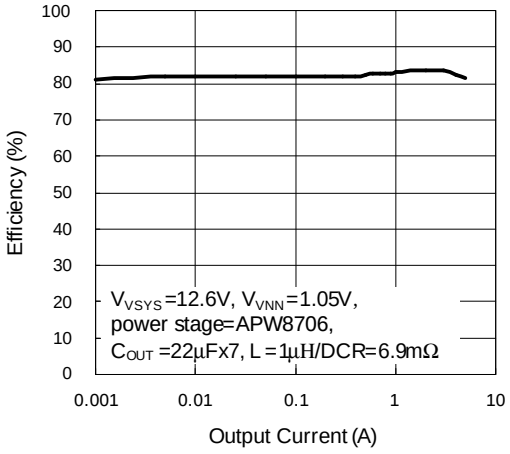
V1P2A Efficiency vs. Output Current



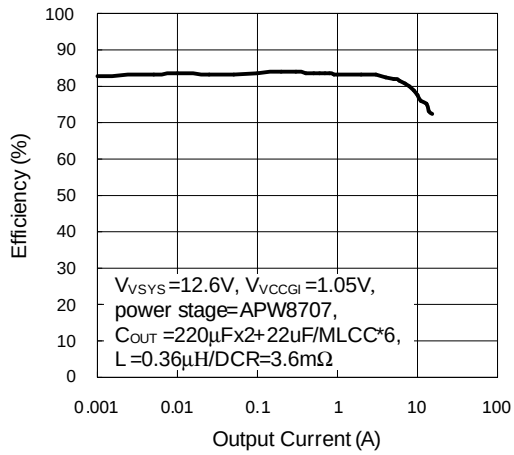
V1P8A Efficiency vs. Output Current



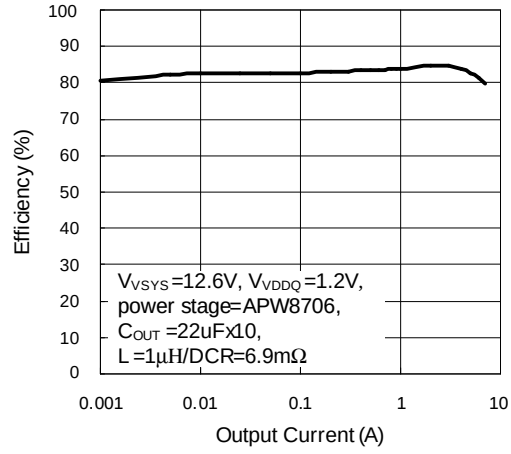
VNN Efficiency vs. Output Current



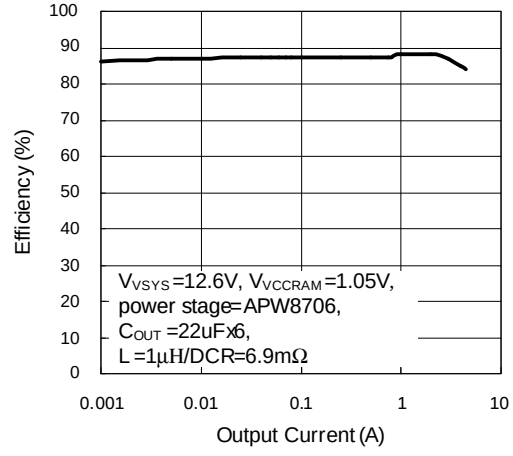
VCCGI Efficiency vs. Output Current



VDDQ Efficiency vs. Output Current



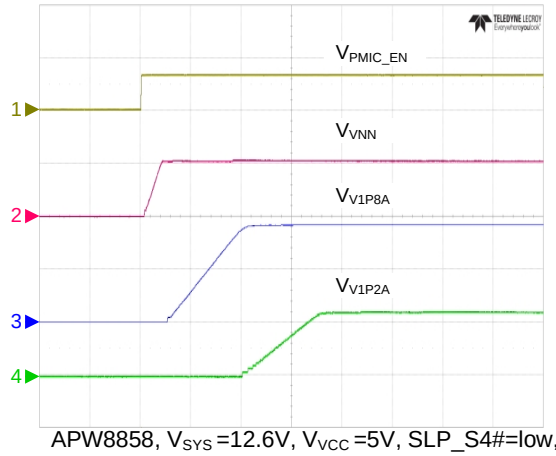
VCCRAM Efficiency vs. Output Current



12.13 Operating Waveforms

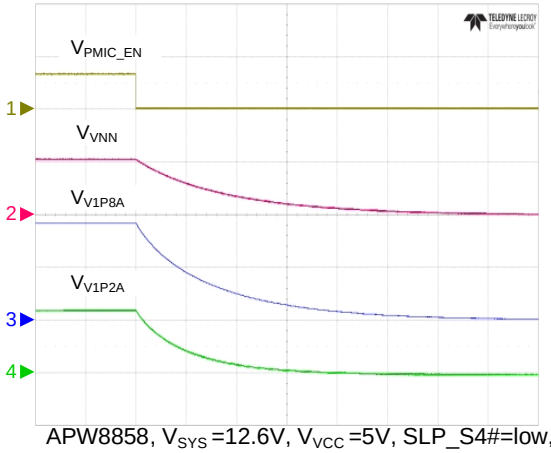
The test condition is T_A= 25°C unless otherwise specified.

Turn On Response (part 1)



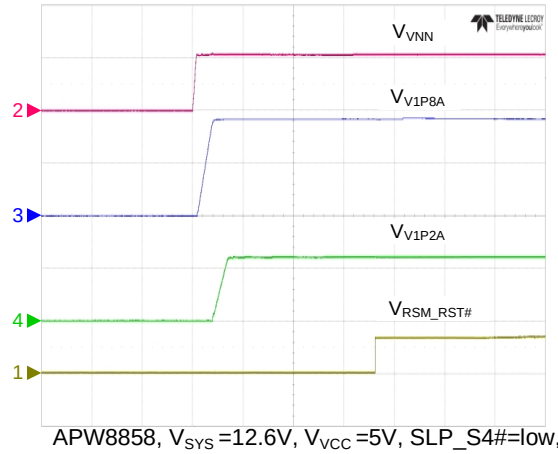
APW8858, V_{SYS} =12.6V, V_{VCC} =5V, SLP_S4#=low, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: V_{PMIC_EN}, 5V/Div, DC
CH2: V_{VNN}, 1V/Div, DC
CH3: V_{V1P8A}, 1V/Div, DC
CH4: V_{V1P2A}, 1V/Div, DC
TIME: 1ms/Div

Turn Off Response (part 1)



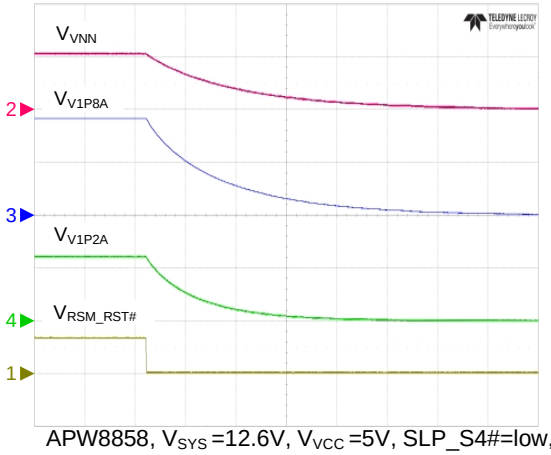
APW8858, V_{SYS} =12.6V, V_{VCC} =5V, SLP_S4#=low, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: V_{PMIC_EN}, 5V/Div, DC
CH2: V_{VNN}, 1V/Div, DC
CH3: V_{V1P8A}, 1V/Div, DC
CH4: V_{V1P2A}, 1V/Div, DC
TIME: 10ms/Div

Turn On Response (part 2)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, SLP_S4#=low, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{RSM\_RST\#}$, 5V/Div, DC
CH2: V_{VNN}, 1V/Div, DC
CH3: V_{V1P8A}, 1V/Div, DC
CH4: V_{V1P2A}, 1V/Div, DC
TIME: 5ms/Div

Turn Off Response (part 2)

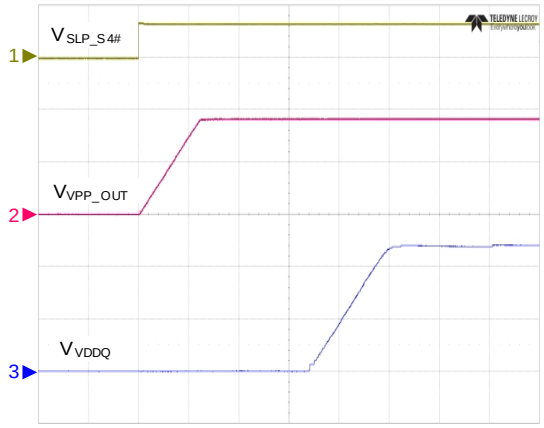


APW8858, V_{SYS} =12.6V, V_{VCC} =5V, SLP_S4#=low, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{RSM\_RST\#}$, 5V/Div, DC
CH2: V_{VNN}, 1V/Div, DC
CH3: V_{V1P8A}, 1V/Div, DC
CH4: V_{V1P2A}, 1V/Div, DC
TIME: 10ms/Div

12.13 Operating Waveforms (Cont.)

The test condition is T_A= 25°C unless otherwise specified.

S4# Turn On Response

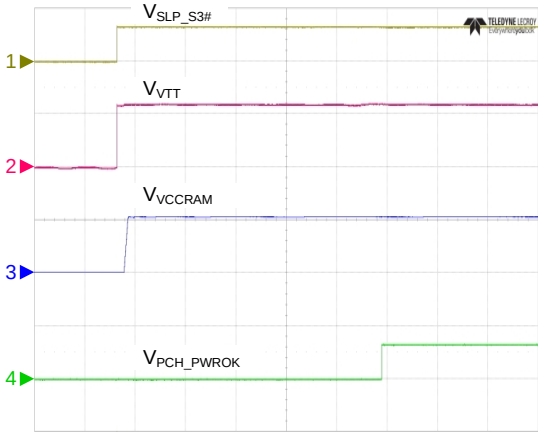


APW8858, V_{SYS}=12.6V, V_{VCC}=5V, PMIC_EN=high, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{SLP\_S4\#}$, 5V/Div, DC
CH2: V_{VPP_OUT}, 1V/Div, DC
CH3: V_{VDDQ}, 500mV/Div, DC
TIME: 1ms/Div

S4# Turn Off Response

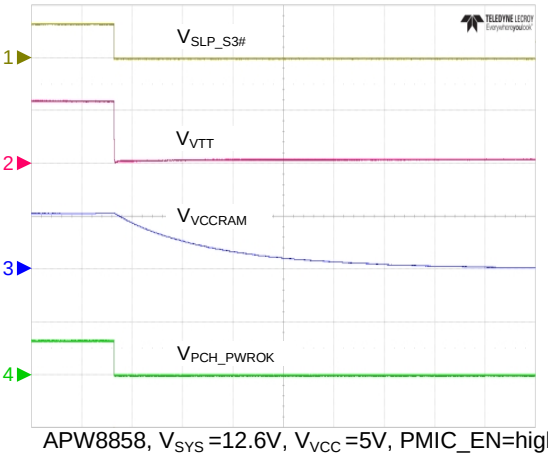
APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S3#=low, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{SLP\_S4\#}$, 5V/Div, DC
CH2: V_{VPP_OUT}, 1V/Div, DC
CH3: V_{VDDQ}, 500mV/Div, DC
TIME: 20ms/Div

S3# Turn On Response (part 1)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{SLP\_S3\#}$, 5V/Div, DC
CH2: V_{VTT}, 500mV/Div, DC
CH3: V_{VDDQ}, 1V/Div, DC
CH4: V_{PCH_PWROK}, 5V/Div, DC
TIME: 20ms/Div

S3# Turn Off Response (part 1)

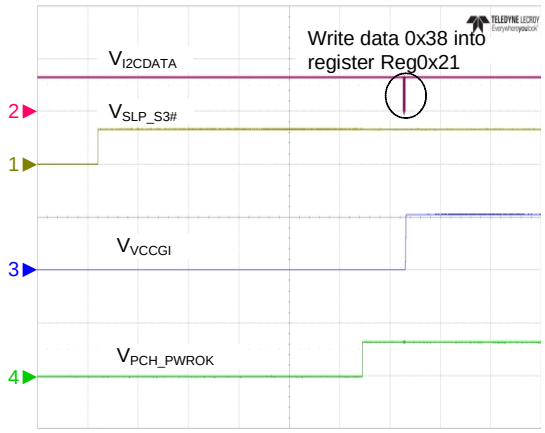


APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, VRs no load, the other settings refer to Typical Application Circuit
CH1: $V_{SLP\_S3\#}$, 5V/Div, DC
CH2: V_{VTT}, 500mV/Div, DC
CH3: V_{VDDQ}, 1V/Div, DC
CH4: V_{PCH_PWROK}, 5V/Div, DC
TIME: 20ms/Div

12.13 Operating Waveforms (Cont.)

The test condition is T_A= 25°C unless otherwise specified.

S3# Turn On Response (part 2)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, write data 0x38 into Reg0x21, VRs no load, other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S3\#}$, 5V/Div, DC

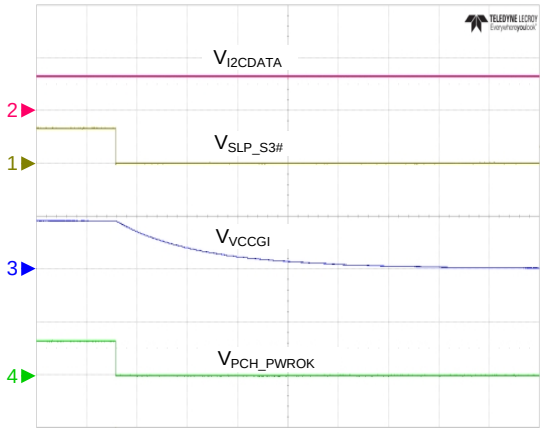
CH2: $V_{I2CDATA}$, 5V/Div, DC

CH3: V_{VCCGI}, 1V/Div, DC

CH4: V_{PCH_PWROK}, 5V/Div, DC

TIME: 20ms/Div

S3# Turn Off Response (part 2)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, write data 0x38 into Reg0x21, VRs no load, other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S3\#}$, 5V/Div, DC

CH2: $V_{I2CDATA}$, 5V/Div, DC

CH3: V_{VCCGI}, 1V/Div, DC

CH4: V_{PCH_PWROK}, 5V/Div, DC

TIME: 50ms/Div

S0# Turn On Response (part 1)

APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VNN load=10mA, the other VRs no load, the other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S0\#}$, 5V/Div, DC

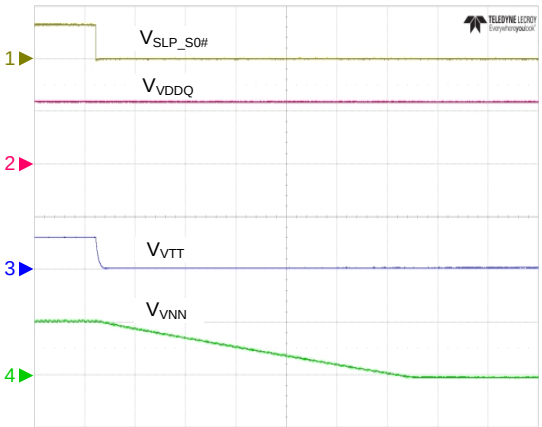
CH2: V_{VDDQ}, 1V/Div, DC

CH3: V_{VTT}, 1V/Div, DC

CH4: V_{VNN}, 1V/Div, DC

TIME: 200µs/Div

S0# Turn Off Response (part 1)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VNN load=10mA, the other VRs no load, the other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S0\#}$, 5V/Div, DC

CH2: V_{VDDQ}, 1V/Div, DC

CH3: V_{VTT}, 1V/Div, DC

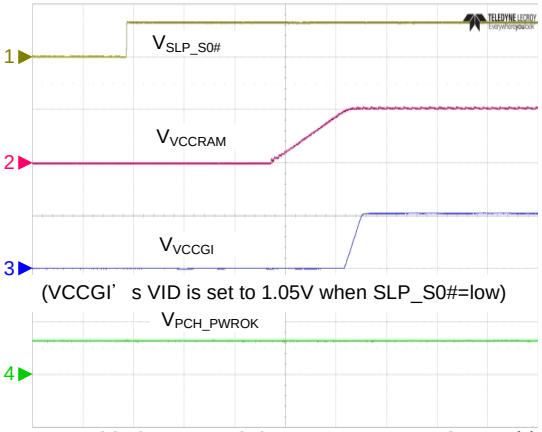
CH4: V_{VNN}, 1V/Div, DC

TIME: 2ms/Div

12.13 Operating Waveforms (Cont.)

The test condition is T_A= 25°C unless otherwise specified.

S0# Turn On Response (part 2)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VCCRAM and VCCGI load=10mA,the other VRs no load, the other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S0\#}$, 5V/Div, DC

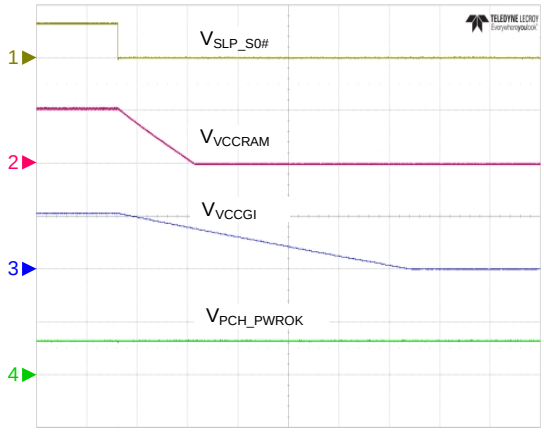
CH2: V_{VDDQ}, 1V/Div, DC

CH3: V_{VTT}, 1V/Div, DC

CH4: V_{VNN}, 1V/Div, DC

TIME: 1ms/Div

S0# Turn Off Response (part 2)



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VCCRAM and VCCGI load=10mA, the other VRs no load, the other settings refer to Typical Application Circuit

CH1: $V_{SLP\_S0\#}$, 5V/Div, DC

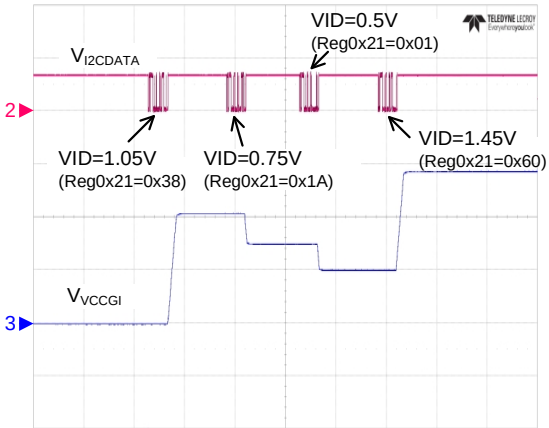
CH2: V_{VDDQ}, 1V/Div, DC

CH3: V_{VTT}, 1V/Div, DC

CH4: V_{VNN}, 1V/Div, DC

TIME: 10ms/Div

VCCGI' s Dynamic Voltage Change



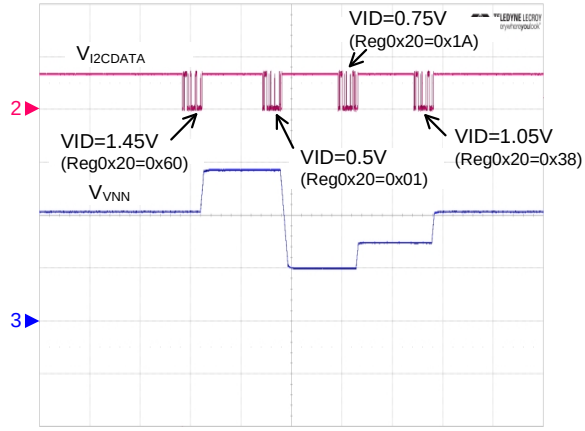
APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VCCGI no load the other VRs no load, the other settings refer to Typical Application Circuit

CH2: $V_{I2CDATA}$, 5V/Div, DC

CH3: V_{VCCGI}, 500mV/Div, DC

TIME: 2ms/Div

VNN' s Dynamic Voltage Change



APW8858, V_{SYS} =12.6V, V_{VCC} =5V, PMIC_EN=high, SLP_S4#=high, SLP_S3#=high, VCCGI no load the other VRs no load, the other settings refer to Typical Application Circuit

CH2: $V_{I2CDATA}$, 5V/Div, DC

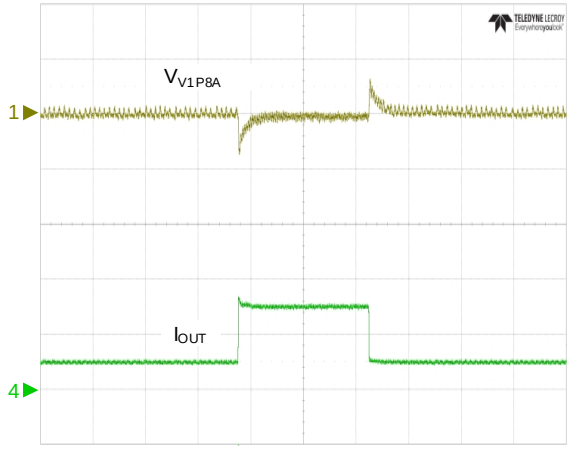
CH3: V_{VNN}, 500mV/Div, DC

TIME: 2ms/Div

12.13 Operating Waveforms (Cont.)

The test condition is T_A= 25°C unless otherwise specified.

V1P8A Load Transient Response



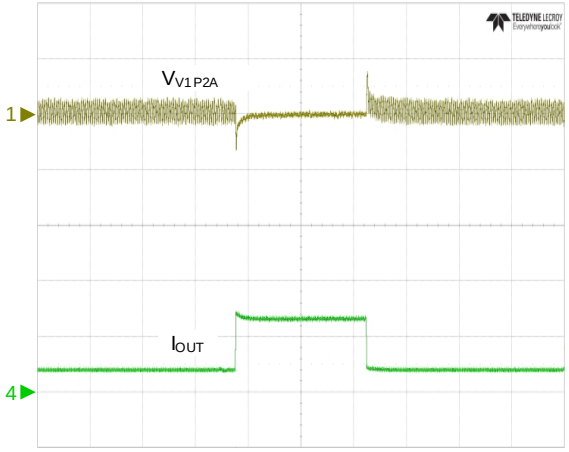
V_{V1P8A_IN} =5V, V_{V1P8A} =1.8V, L=1µH, C_{OUT} =22µF*4, I_{OUT}=0.9A-3A-0.9A, slew rate=2.5A/µs

CH1: V_{V1P8A}, 50mV/Div, offset=1.8V

CH4: I_{OUT}, 2A/Div, DC

TIME: 100µs/Div

V1P2A Load Transient Response



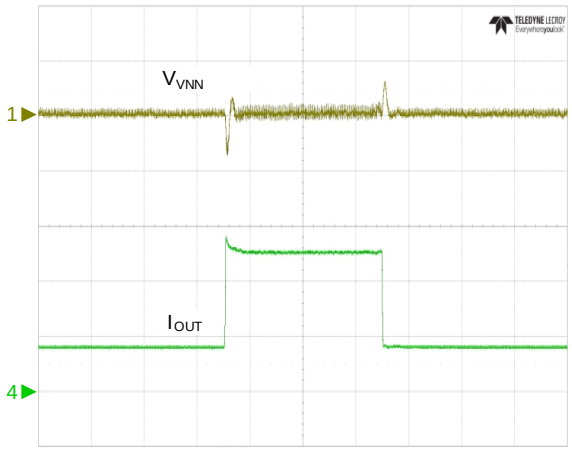
V_{V1P8A_IN} =5V, V_{V1P2A} =1.2V, L=1µH, C_{OUT} =22µF*3, I_{OUT}=0.75A-2.5A-0.75A, slew rate=2.5A/µs

CH1: V_{V1P2A}, 50mV/Div, offset=1.2V

CH4: I_{OUT}, 2A/Div, DC

TIME: 100µs/Div

VNN Load Transient Response



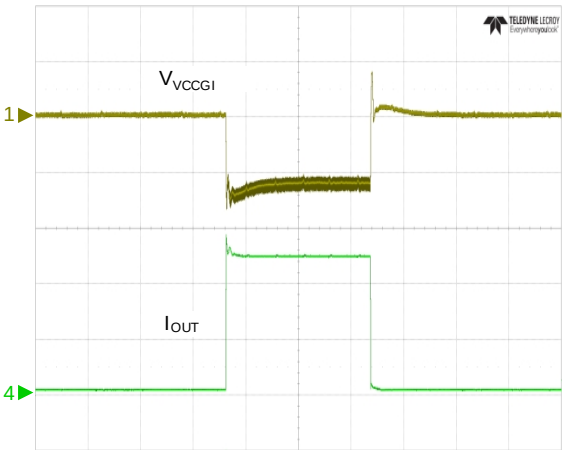
V_{VSYS} =12.6V, V_{VNN} =1.05V, L=1µH, C_{OUT} =22µF*7, I_{OUT}=1.5A-5A-1.5A, slew rate=3.5A/µs

CH1: V_{VNN}, 50mV/Div, offset=1.05V

CH4: I_{OUT}, 2A/Div, DC

TIME: 50µs/Div

VCCGI Load Transient Response



V_{VSYS} =12.6V, V_{VCCGI} =1.05V, L=0.36µH, C_{OUT} =220µF*2+22µF*6, Load Line function is activated with 6mΩ setting, I_{OUT}=1A-25A-1A, slew rate=24A/µs

CH1: V_{VCCGI}, 100mV/Div, offset=1.05V

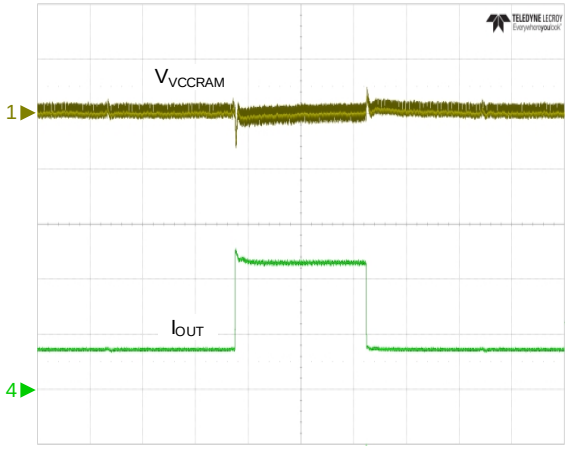
CH4: I_{OUT}, 5A/Div, DC

TIME: 200µs/Div

12.13 Operating Waveforms (Cont.)

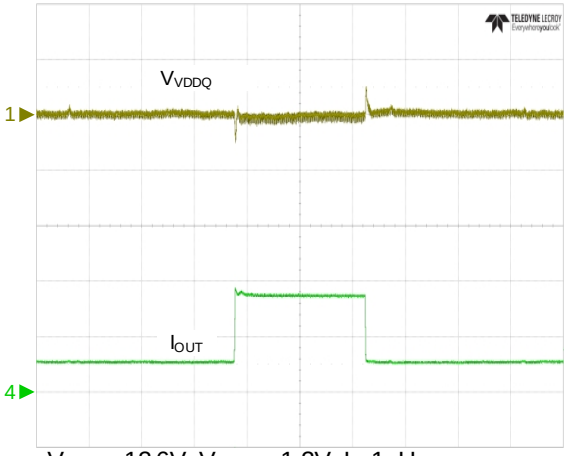
The test condition is T_A= 25°C unless otherwise specified.

VCCRAM Load Transient Response



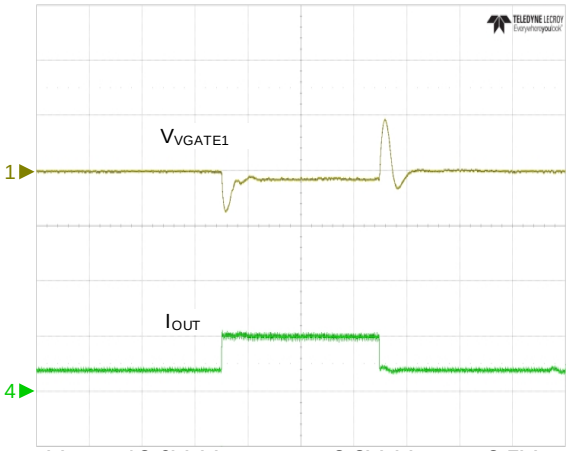
V_{VSYS}=12.6V, V_{VCCRAM}=1.05V, L=1µH,
C_{OUT} =22µF*6,
I_{OUT}=1.35A-4.5A-1.35A, slew rate=2.5A/µs
CH1: V_{VCCRAM}, 50mV/Div, offset=1.05V
CH4: I_{OUT}, 2A/Div, DC
TIME: 100µs/Div

VDDQ Load Transient Response



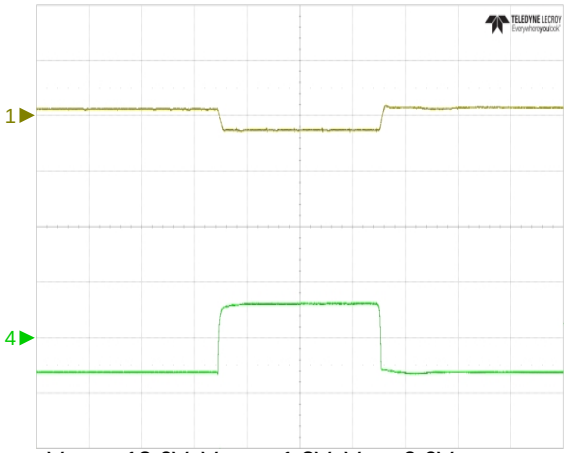
V_{VSYS}=12.6V, V_{VDDQ} =1.2V, L=1µH,
C_{OUT} =22µF*10,
I_{OUT}=2.1A-7A-2.1A, slew rate=2.5A/µs
CH1: V_{VDDQ}, 50mV/Div, offset=1.2V
CH4: I_{OUT}, 4A/Div, DC
TIME: 100µs/Div

VGATE1 Load Transient Response



V_{VSYS} =12.6V, $V_{VPP\_LDO\_IN}$ =3.3V, V_{VGATE1}=2.5V,
C_{OUT} =10µF*2,
I_{OUT}=0.3A-1A-0.3A, slew rate=2.5A/µs
CH1: V_{VGATE1}, 100mV/Div, offset=2.5V
CH4: I_{OUT}, 1A/Div, DC
TIME: 50µs/Div

VTT Load Transient Response



V_{VSYS} =12.6V, V_{VDDQ} =1.2V, V_{VTT}=0.6V,
C_{OUT} =10µF*2, I_{OUT}=(-0.6A)-0.6A-(-0.6A), slew rate=2.5A/µs
CH1: V_{VTT}, 100mV/Div, offset=0.6V
CH4: I_{OUT}, 1A/Div, DC
TIME: 10µs/Div

13. Register Description

13.1 Register Map

Register Name	Register Address	Bits								Read/Write/Read Only State	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
VENDORID	0x00	1	0	1	0	1	1	0	0	R	0xAC
REVID	0x01	0	0	0	0	0	0	0	0	R	0x00
IRQ	0x02	0	0	0	0	0	0	0	0	R/W	0x00
IRQ_MASK	0x03	1	1	1	1	1	1	1	1	R/W	0xFF
PMICSTAT	0x04	0	0	0	0	0	0	0	0	R	0x00
OFFONSRC	0x05	0	0	0	0	0	0	0	0	R/W	0x00
BUCK1CTRL	0x20	0	0	1	1	1	0	0	0	R/W	0x38
BUCK2CTRL	0x21	0	0	0	0	0	0	0	0	R/W	0x00
BUCK3CTRL	0x22	0	0	0	0	1	1	0	0	R/W	0x0C
BUCK4CTRL	0x25	0	0	0	0	1	1	0	0	R/W	0x0C
BUCK5CTRL	0x26	0	0	0	0	1	1	0	0	R/W	0x0C
BUCK6CTRL	0x27	0	0	0	0	0	0	0	0	R/W	0x00
DISCHCTRL1	0x40	0	1	0	1	0	1	0	1	R/W	0x55
DISCHCTRL2	0x41	0	0	0	0	0	1	0	1	R/W	0x05
POK_DELAY	0x43	0	0	0	0	0	1	1	1	R/W	0x07

13.2 7-bit VID Encoding

0000000 = 0.00V	0100000 = 0.81V	1000000 = 1.13V	1100000 = 1.45V
0000001 = 0.50V	0100001 = 0.82V	1000001 = 1.14V	1100001 = RSVD
0000010 = 0.51V	0100010 = 0.83V	1000010 = 1.15V	1100010 = RSVD
0000011 = 0.52V	0100011 = 0.84V	1000011 = 1.16V	1100011 = RSVD
0000100 = 0.53V	0100100 = 0.85V	1000100 = 1.17V	1100100 = RSVD
0000101 = 0.54V	0100101 = 0.86V	1000101 = 1.18V	1100101 = RSVD
0000110 = 0.55V	0100110 = 0.87V	1000110 = 1.19V	1100110 = RSVD
0000111 = 0.56V	0100111 = 0.88V	1000111 = 1.20V	1100111 = RSVD
0001000 = 0.57V	0101000 = 0.89V	1001000 = 1.21V	1101000 = RSVD
0001001 = 0.58V	0101001 = 0.90V	1001001 = 1.22V	1101001 = RSVD
0001010 = 0.59V	0101010 = 0.91V	1001010 = 1.23V	1101010 = RSVD
0001011 = 0.60V	0101011 = 0.92V	1001011 = 1.24V	1101011 = RSVD
0001100 = 0.61V	0101100 = 0.93V	1001100 = 1.25V	1101100 = RSVD
0001101 = 0.62V	0101101 = 0.94V	1001101 = 1.26V	1101101 = RSVD
0001110 = 0.63V	0101110 = 0.95V	1001110 = 1.27V	1101110 = RSVD
0001111 = 0.64V	0101111 = 0.96V	1001111 = 1.28V	1101111 = RSVD
0010000 = 0.65V	0110000 = 0.97V	1010000 = 1.29V	1110000 = RSVD
0010001 = 0.66V	0110001 = 0.98V	1010001 = 1.30V	1110001 = RSVD
0010010 = 0.67V	0110010 = 0.99V	1010010 = 1.31V	1110010 = RSVD
0010011 = 0.68V	0110011 = 1.00V	1010011 = 1.32V	1110011 = RSVD
0010100 = 0.69V	0110100 = 1.01V	1010100 = 1.33V	1110100 = RSVD
0010101 = 0.70V	0110101 = 1.02V	1010101 = 1.34V	1110101 = RSVD
0010110 = 0.71V	0110110 = 1.03V	1010110 = 1.35V	1110110 = RSVD
0010111 = 0.72V	0110111 = 1.04V	1010111 = 1.36V	1110111 = RSVD
0011000 = 0.73V	0111000 = 1.05V	1011000 = 1.37V	1111000 = RSVD
0011001 = 0.74V	0111001 = 1.06V	1011001 = 1.38V	1111001 = RSVD
0011010 = 0.75V	0111010 = 1.07V	1011010 = 1.39V	1111010 = RSVD
0011011 = 0.76V	0111011 = 1.08V	1011011 = 1.40V	1111011 = RSVD
0011100 = 0.77V	0111100 = 1.09V	1011100 = 1.41V	1111100 = RSVD
0011101 = 0.78V	0111101 = 1.10V	1011101 = 1.42V	1111101 = RSVD
0011110 = 0.79V	0111110 = 1.11V	1011110 = 1.43V	1111110 = RSVD
0011111 = 0.80V	0111111 = 1.12V	1011111 = 1.44V	1111111 = RSVD

13.3 Vendor ID Register Table

Address	0x00							
Field Name	VENDORID [7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VENDORID [7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power On Default	1	0	1	0	1	1	0	0
Bit Name	**Bit Definition**							
VENDORID [7:0]	8-bit vendor ID resister programmed by vendor in manufacturing. Vendors should use the same ID they use for their SVID controllers.							

13.4 Rev ID Register Table

Address	0x01							
Field Name	REVID							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD		MAJREV[2:0]			MINREV[2:0]		
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
MAJREV[2:0]	Major Si revision ID. First stepping to start at 000. To be incremented with each new mask stepping. 000 = A 001 = B 010 = C 011 = D 100 = E 101 = F 110 = G 111 = H							
MINREV[2:0]	Minor Si revision ID. First stepping to start at 000. To be incremented with metal change. This field is set to 000 when a major revision is made. 000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7							

13.5 IRQ Register Table

Address	0x02							
Field Name	IRQ							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	RSVD				ONOFFSRC	RSVD	DIETEMP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit Name	**Bit Definition**							
RSVD	-							
ONOFFSRC	Shutdown event interrupt. Set by PMIC and cleared by host. This bit when the PMIC shuts down. 0 = Cleared 1 = Shutdown event logged If the MONOFFSRC bit is set to 0, the setting of this bit will result in the assertion of IRQ# pin, signaling an interrupt to the host. The host clears this by writing a 1 to this register. However, the bit cannot be cleared by host if shutdown event (except COLDOFF) is still present. Writing a 0 to this bit has no effect.							
RSVD	-							
DIETEMP	PMIC Die Temp Interrupt. Set by PMIC and cleared by host. The PMIC sets this bit whenever the PMIC die temp crosses the max temp threshold (rising and falling). 0 = Cleared 1 = PMIC Die Temp Threshold crossed (rising and falling) If the MDIETEMP bit is set to 0, the setting of this bit will result in the assertion of IRQ# pin, signaling an interrupt to the host. The host clears this by writing a 1 to this register. Writing a 0 to this bit has no effect.							

13.6 IRQ_MASK Register Table

Address	0x03							
Field Name	IRQ_MASK							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	RSVD				MONOFFSRC	RSVD	MDIETEMP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	1	1	1	1	1	1	1	1
Bit Name	**Bit Definition**							
RSVD	-							
MONOFFSRC	Shutdown event interrupt mask. Set and cleared by host. Setting this bit masks the ONOFFSRC interrupt and prevents the assertion of the PMIC interrupt pin (IRQ#). 0 = interrupt unmasked 1 = interrupt masked							
RSVD	-							
MDIETEMP	PMIC Die Temp interrupt mask. Set and cleared by host. Setting this bit masks the DIETEMP interrupt and prevents the assertion of the PMIC interrupt pin (IRQ#). 0 = interrupt unmasked 1 = interrupt masked							

13.7 RESETIRQ1 Register Table

Address	0x04							
Field Name	PMICSTAT							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD							SDIETEMP
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
SDIETEMP	PMIC Die Temp status. Set and cleared by PMIC 0 = PMIC temp below critical threshold. 1 = PMIC temp above critical threshold.							

13.8 OFFONSRC Register Table

Address	0x05							
Field Name	OFFONSRC							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD				COLDOFF	UVLO	OCP	CRITTEMP
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
COLDOFF	Set by PMIC, cleared by host. Host writes a 1 to this bit to clear this bit. 0= cleared 1= PMIC was shut down by host via PMIC_EN pin.							
UVLO	Set by PMIC, cleared by host. Host writes a 1 to this bit to clear this bit. Note: This bit cannot be cleared by host if UVLO event is still present 0 = cleared 1 = PMIC was shut down due to a UVLO event (VSYS < 5.4V). The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.							
OCP	Set by PMIC, cleared by host. Host writes a 1 to this bit to clear this bit. Note: This bit cannot be cleared by host if OCP event is still present 0 = cleared 1= PMIC shut down due to OCP event. The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.							
CRITTEMP	Set by PMIC, cleared by host. Host writes a 1 to this bit to clear this bit. Note: This bit cannot be cleared by host is CRITTEMP event is still present 0 = cleared 1= PMIC shut down due to PMIC at critical temp. The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.							

13.9 BUCK1CTRL Register Table

Address	0x20							
Field Name	BUCK1CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD	BUCK1_VID[6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	1	1	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
BUCK1_VID [6:0]	Set by host. This field sets the BUCK1 nominal regulator operating voltage. Note: 0V is a valid setting and all power goods must stay high when VID is set to 0x00h. See section 13.2 for VID encoding. All power goods must stay high when transitioning in and out of S0iX.							

13.10 PWRSRCINT Register Table

Address	0x21							
Field Name	BUCK2CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD	BUCK2_VID[6:0]						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
BUCK2_VID[6:0]	set by host. This field sets the BUCK2 nominal regulator operating voltage. Note: 0V is a valid setting and all power goods must stay high when VID is set to 0x00h. See section 13.2 for VID encoding. All power goods must stay high when transitioning in and out of S0iX.							

13.11 BUCK3CTRL Register Table

Address	0x22							
Field Name	BUCK3CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD				BUCK3_VID[1:0]		MODE	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	1	0	0
Bit Name	**Bit Definition**							
RSVD	-							
BUCK3_VID[1:0]	Set and cleared by host. This field sets the BUCK3 nominal regulator operating voltage. 00 = 1.100V 01 = 1.075V 10 = 1.000V 11 = 1.050V (default)							
MODE	VR MODE bit – set and cleared by host. 0 – AUTO Mode – VR adjusts its operating mode (PWM / PFM) based on load current to maximize efficiency over load current range. 1 – Forced PWM Mode - VR to operate in PWM mode only.							
RSVD	-							

13.12 BUCK4CTRL Register Table

Address	0x25							
Field Name	BUCK4CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD				BUCK4_VID[1:0]		MODE	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	1	1	0	0
Bit Name	**Bit Definition**							
RSVD	-							
BUCK4_VID[1:0]	Set and cleared by host. This field sets the BUCK4 nominal regulator operating voltage. 00 = 1.880V 01 = 1.850V 10 = 1.830V 11 = 1.800V (default)							
MODE	VR MODE bit – set and cleared by host. 0 – AUTO Mode – VR adjusts its operating mode (PWM / PFM) based on load current to maximize efficiency over load current range. 1 – Forced PWM Mode - VR to operate in PWM mode only.							
RSVD	-							

13.13 BUCK5CTRL Register Table

Address	0x26							
Field Name	BUCK5CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD				BUCK5_VID[1:0]		MODE	RSVD
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	1	0	1	0	1	0
Bit Name	**Bit Definition**							
RSVD	-							
BUCK5_VID[1:0]	Set by host. This field sets the BUCK5 nominal regulator operating voltage. 00 = 1.10 01 = 1.15 10 = 1.24V 11 = 1.20V (default)							
MODE	VR MODE bit – set and cleared by host. 0 – AUTO Mode – VR adjusts its operating mode (PWM / PFM) based on load current to maximize efficiency over load current range. 1 – Forced PWM Mode - VR to operate in PWM mode only.							
RSVD	-							

13.14 BUCK6CTRL Register Table

Address	0x27							
Field Name	BUCK6CTRL							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD						MODE	RSVD
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0
Bit Name	**Bit Definition**							
RSVD	-							
MODE	VR MODE bit – set and cleared by host. 0 – AUTO Mode – VR adjusts it operating mode (PWM / PFM) based on load current to maximize efficiency over load current range. 1 – Forced PWM Mode - VR to operate in PWM mode only.							
RSVD	-							

13.15 DISCHCTRL1 Register Table

Address	0x40							
Field Name	DISCHCTRL1							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	BUCK4_DIS		BUCK3_DIS		BUCK2_DIS		BUCK1_DIS	
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	1	0	1	0	1	0	1
Bit Name	**Bit Definition**							
BUCK4_DIS	Buck4 discharge resistance setting when Buck4 is disabled: 00 = function disabled (Hi Z >1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi Z when VR is enabled.							
BUCK3_DIS	Buck3 discharge resistance setting when Buck3 is disabled: 00 = function disabled (Hi Z >1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi Z when VR is enabled.							
BUCK2_DIS	Buck2 discharge resistance setting when Buck2 is disabled: 00 = function disabled (Hi Z >1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi Z when VR is enabled.							
BUCK1_DIS	uck1 discharge resistance setting when Buck1 is disabled: 00 = function disabled (Hi Z >1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi Z when VR is enabled.							

13.16 DISCHCTRL2 Register Table

Address	0x41							
Field Name	DISCHCTRL2							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD				BUCK6_DIS		BUCK5_DIS	
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	0	1
Bit Name	**Bit Definition**							
RSVD	-							
BUCK6_DIS	Buck6 discharge resistance setting when Buck6 is disabled: 00 = function disabled (Hi Z > 1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi-Z when VR is enabled.							
BUCK5_DIS	Buck5 discharge resistance setting when Buck5 is disabled: 00 = function disabled (Hi Z > 1k) 01 = 100 Ω 10 = 200 Ω 11 = 500 Ω Note: Discharge resistor must be hi-Z when VR is enabled.							

13.17 POK_DELAY Register Table

Address	0x43							
Field Name	POK_DELAY							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RSVD					PWROKDELAY[2:0]		
Read/Writ	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	1	1	1
Bit Name	**Bit Definition**							
RSVD	-							
PWROKDELAY[2:0]	Programmable all rails stable to PCH_PWROK delay: 000 = 2.5 ms 001 = 5.0 ms 010 = 10 ms 011 = 15 ms 100 = 20 ms 101 = 50 ms 110 = 75 ms 111 = 100 ms (Default) Note: The delay tolerance for the above settings should < +/-20%.							

14.Function Description

14.1 VR Function Description

Soft-Start

All VRs are equipped soft-start function, when enable signal of each VR is activated, an internal soft start ramps the output voltage at a certain rate. This allows the output voltage to ramp up gradually, eliminating overshoot and excessive inrush current.

Over Voltage Protection (OVP)

The over voltage protection circuitry monitors the feedback voltage to prevent the output from accidentally exceeding the desired set point. Once the feedback voltage exceeds typically 130% of the set point voltage, the high/low side MOSFETs turn off and internal latch circuitry is activated. This insures protection of the load damage and circuit reset is only achieved either by pulling low VDDQ_SEL below 0.3V or cycling VCC power off then on.

Over Current Protection (OCP) and Under Voltage Protection (UVP)

The each output of VRs is protected against gradual over current or sudden short on its output. When inductor current peak value exceeds the set threshold an internal over-current protection is activated which turns off the high side and low side MOSFETs. Once the output voltage drops below a typical threshold of 70% of the output set point value, both high side and low side MOSFETs turn off and an internal latch circuit is initiated.

When any of OCP or UVP is activated, the IC will be latch off. To release the latch-off is to pull low VDDQ_SEL below 0.3V or to cycle VCC power off then on.

Output Discharge

When any one of VR1~VR6 is shut down, both Upper and Lower MOSFETs will be turned off and an internal MOSFET with about 100/200/500 ohms (I^2C programmable) Rds-on discharges the output via its FBP pin. The VTT and VPP also discharge the output via the output pin in shutdown mode.

When VNN, VCCGI, VCCRAM or VDDQ is shut down, the PWM signal pin will be low level and both high side and low side MOSFETs turn off while an internal discharge device Rds-on resided at FBP pin turns on to discharge the output voltage.

Memory Type Support

In order to support different type of memory, ex., DDR3L or DDR4, the VDDQ, V18U_25U and VTT output voltage level will be changed in response to VDDQ_SEL voltage level. An external pull low resistor, RVDDQ_SEL, on VDDQ_SEL pin can set the VDDQ_SEL voltage level due to a 10μA current source flowing out of VDDQ_SEL. During power on after VSYS rises above 3.6V APW8858 keeps sampling VDDQ_SEL's voltage to decide which VDDQ_SEL state is selected. The VDDQ_SEL state is hold the moment that VNN_POK asserts. There are totally 5 states of selectable voltage conditions as below as well as if this pin is pulled below 0.3V threshold using an external small signal MOSFET. If any fault event occurs, it is suggested to pull VDDQ_SEL pin below 0.3V to clear internal IRQ registers.

Table 4. VDDQ_SEL State

VDDQ_SEL State	Suggested R_{VDDQ_SEL}, ±1% tol.	V_{VDDQ}	V_{V18U_25U}	V_{VTT}	Usage
1	using an external MOSFET to pull low < 0.3V	off	off	off	Reset fault event
2	60.4kΩ	1.15V	off	off	3DXPoint
3	110kΩ	1.1V	1.8V	off	LPDDR4
4	165kΩ	1.2V	1.8V	0.6V	LPDDR3/DDR4RS/DDR4E
5	267kΩ	1.2V	2.5V	0.6V	DDR4
6	316kΩ	1.35V	off	0.675V	DDR3L

14.1 VR Function Description(Cont.)

POK Output

There are two POK pins to indicate power good conditions: RSMRST# and PCH_PWROK.

The two POK pins are open drain outputs that will switch high via an external pull up resistor. It can be pulled up to a maximum voltage of up to 5.5V. The POK assertion and de-assertion are controlled in the following conditions, as shown as below table.

Table 5. POK Assertion and De-assertion Conditions

Power Good	Qualifying Signals (Logical AND)	Note
RSMRST#	VSYS_UVLO (V_{VSYS}>5.4V) THERMTRIP#=1 PMIC_EN=1 BUCK1 (VNN) Power Good (see note) BUCK4 (V1P8A) Power Good BUCK5 (V1P2A) Power Good	This signal must immediately de-assert at loss of any of the qualifying signals, or at the occurrence of a fault condition. THERMTRIP# is treated as de-asserted until the first de-assertion of RSMRST#. BUCK1 Power Good is only a part of the RSMRST# power good tree until the first assertion of PCH_PWROK after PMIC EN L à H transition. If BUCK1 is disabled its Power Good is masked and not part of the RSMRST# power good tree.
PCH_PWROK	UVLO (V_{VSYS}>5.4V) THERMTRIP#=1 PMIC_EN=1 RSMRST#=1 SLP_S4#=1 SLP_S3#=1 GATE1 (V1P8U) BUCK1 (VNN) Power Good (see note) BUCK6 (VDDQ) Power Good BUCK2 (VCCGI) Power Good (see note) BUCK3 (VCCRAM) Power Good	This signal must immediately de-assert at loss of any of the qualifying signals, or at the occurrence of a fault condition. S0 à S0iX: SLP_S0# goes low and PCH_PWROK stays high. In S0iX PCH_PWROK only goes low if fault condition or power loss occurs. THERMTRIP# is treated as de-asserted until the first de-assertion of RSMRST#. BUCK1 Power Good becomes part of the PCH_PWROK tree only after the first assertion of PCH PWROK and stays part of this PWROK tree until the next (PMIC_EN L à H) If BUCK1 and BUCK2 are disabled, their Power Goods are to be masked and not part of the PCH_PWROK power good tree.

14.1 VR Function Description(Cont.)

Interrupt And Masks

The APW8858 keeps monitoring any occurrence of fault event during normal operation and report it to the embedded controller (EC) via the assertion of IRQ# pin. As shown as below diagram, the fault events will be reported are: hot temperature(T_J>120°C), Critical Temperature(T_J>150°C), V1P8A OCP, V1P2A OCP and VSYS_UVLO(V_{VSYS}<5.4V). When any one of these fault events occurs, IRQ# will be pulled low by an internal N-MOSFET. When IRQ# does not assert, the IRQ# is pulled high by an external pull-high resistor which is connected to an external pull-high power source.

During IRQ# assertion, system host can investigate these bits as below diagram revealed. A mask bit, MONOFFSRC or MDIETEMP is provided to mask ONOFFSRC or DIETEMP. When ONOFFSRC or DIETEMP is masked, the IRQ# will not assert when the relative masked fault event occurs.

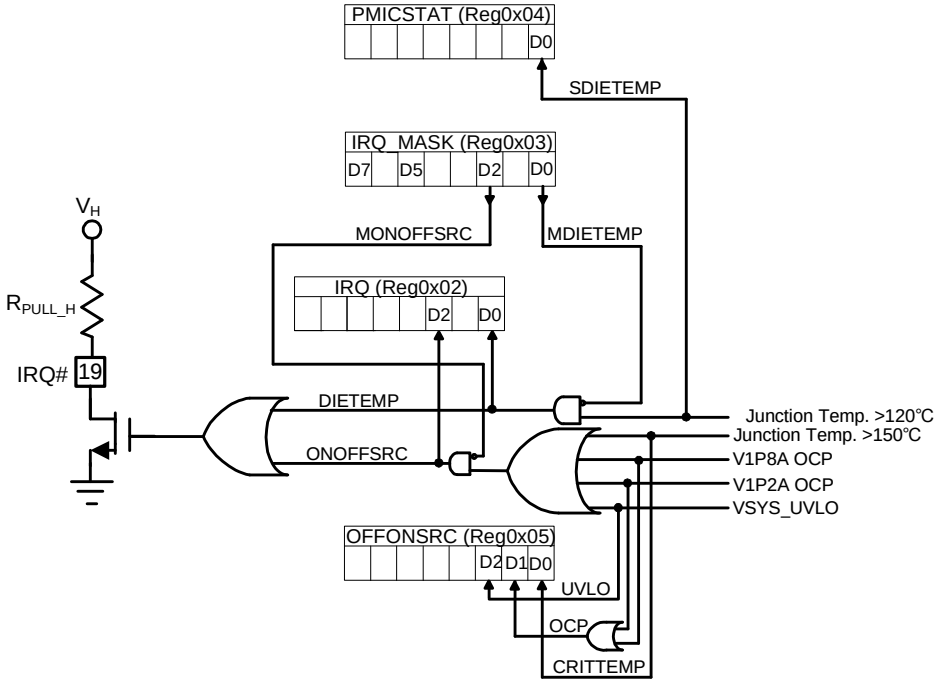


Figure 1. IRQ Architecture Block Diagram

14.2 I²C Function Description

I²C Overview

APW8858 is a slave-only device that is mastered by the SoC. It resides off the SoC's I2C. The slave device implemented on APW8858 side is an asynchronous implementation and will support the fast speed mode (1MHz). Some of the main features for the I²C slave are:

- APW8858 is accessed using a 7-bit addressing scheme.
- I²C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.
- The interface draws as minimum power when not actively reading/writing registers.
- Interface implementation is asynchronous.

Slave Address

APW8858 supports the standard I²C read and write functions. The configuration register space is divided to 15-byte partitions. APW8858 supports three 7-bit device addresses to access each of the 15 byte partitions. The 7-bit device address is "1011110" in default.

Protocol

Reads from PMIC registers follow the "combined protocol" as described in the I²C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different high-speed and fast-speed transaction format/protocol

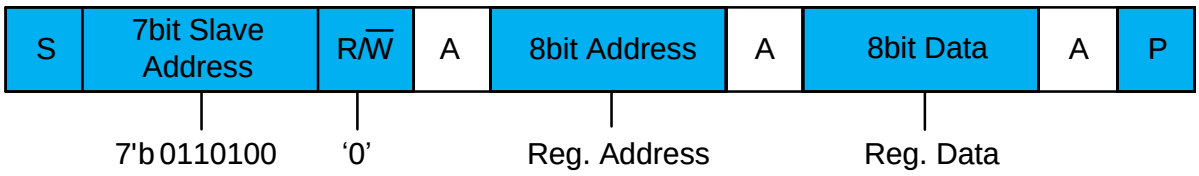


Figure 2. I²C Fast Speed / Fast Speed Plus Single Byte Write

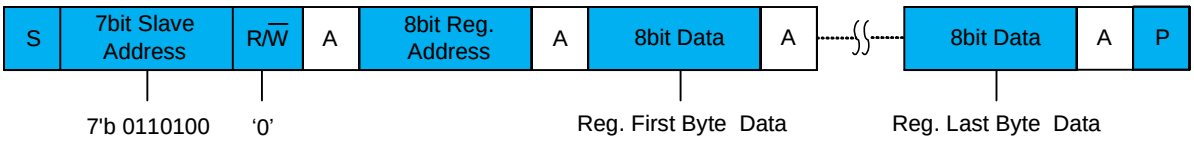


Figure 3. I²C Fast Speed / Fast Speed Plus Multiple Byte Write

14.2 I²C Function Description(Cont.)

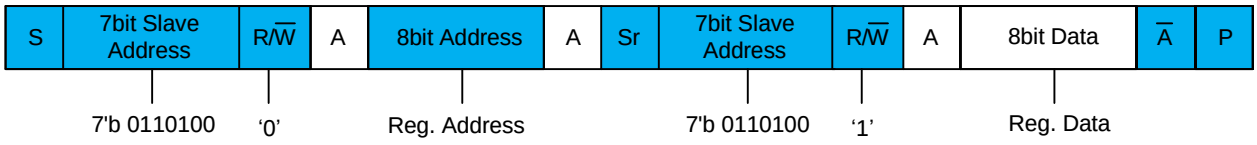


Figure 4. I²C Fast Speed / Fast Speed Plus Single Byte Read

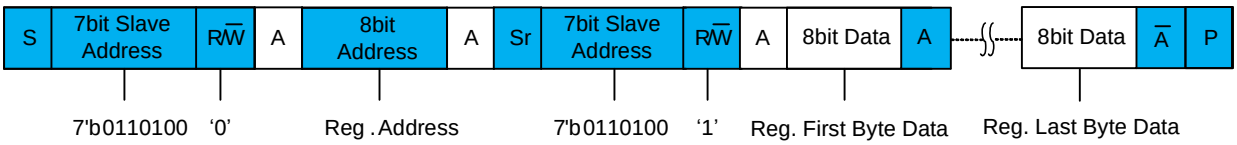


Figure 5. I²C Fast Speed / Fast Speed Plus Multiple Byte Read

Master to Slave

Slave to Master

A = Acknowledge (SDA LOW)

$\overline{A}$ = Not Acknowledge (SDA HIGH)

S = START Condition

Sr = Repeated START Condition

P = STOP Condition

15.Application Information

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

For PWM converter, the inductor value (L) determines the sum of the inductor ripple currents, ΔI_{P-P}, and affects the load transient response. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approximated by:

$$\Delta I_{P-P} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator, although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

15.Application Information(Cont.)

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET. The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current.

Load Line Function

APW8858 implements a load line function in VCCGI voltage regulator. The load line function virtually mimics a load line behavior as depicted as the Figure 2. In order to achieve load line function, the APW8858 uses an RC network, R9 and C45, to sense VCCGI Inductor's current. The RC value should meet the following equation (1) to acquire high current sensing accuracy and to minimize voltage under-shoot or over-shoot of VCCGI during load steps.

L5/RDCR=R9*C45 -----(1) (refer to the Figure 3)

When an inductor of VCCGI is selected, the LL slope can now be calculated based on the inductor's DCR value.

LL Slope=$\Delta V_{VCCGI}/\Delta I_{OUT}$ = RDCR*R11/R10*M ----(2) (refer to the Figure 3)

Where, M is the internal current mirror gain which is 6.

For example, L=0.36µH, DCR=3mΩ, and LL slope=6mΩ is desired.

Assuming C45=0.1µF, apply equation (1) , we can get R9=1.2kΩ
According to equation (2), the R11/R10 must be 1 based on LL slope=6mΩ.
Assuming R11=1kΩ, we can get R10=1kΩ.

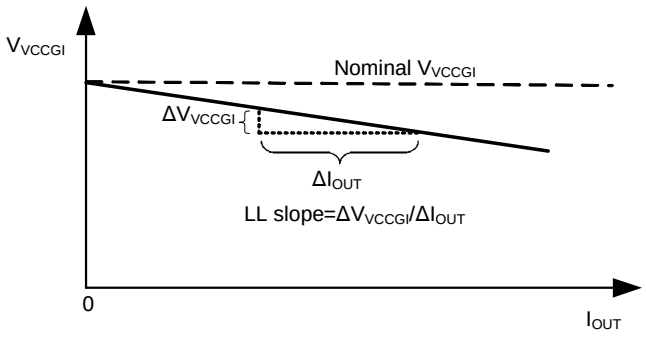


Figure 2. V_{VCCGI} Curve with Load Line Function

15.Application Information(Cont.)

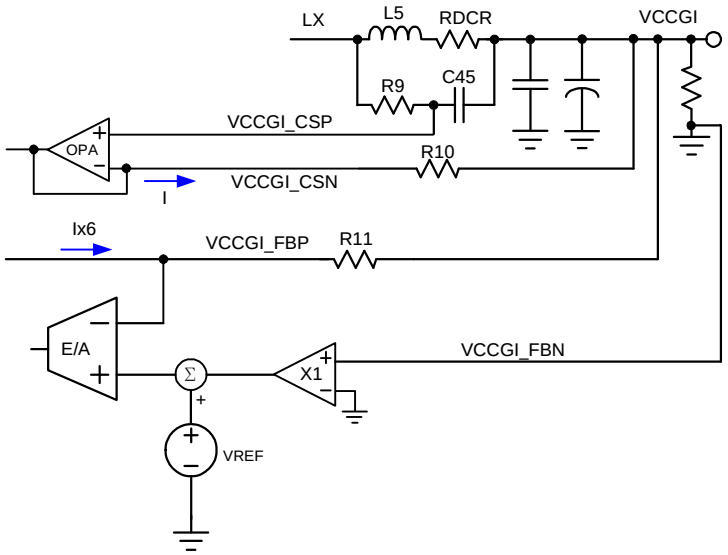
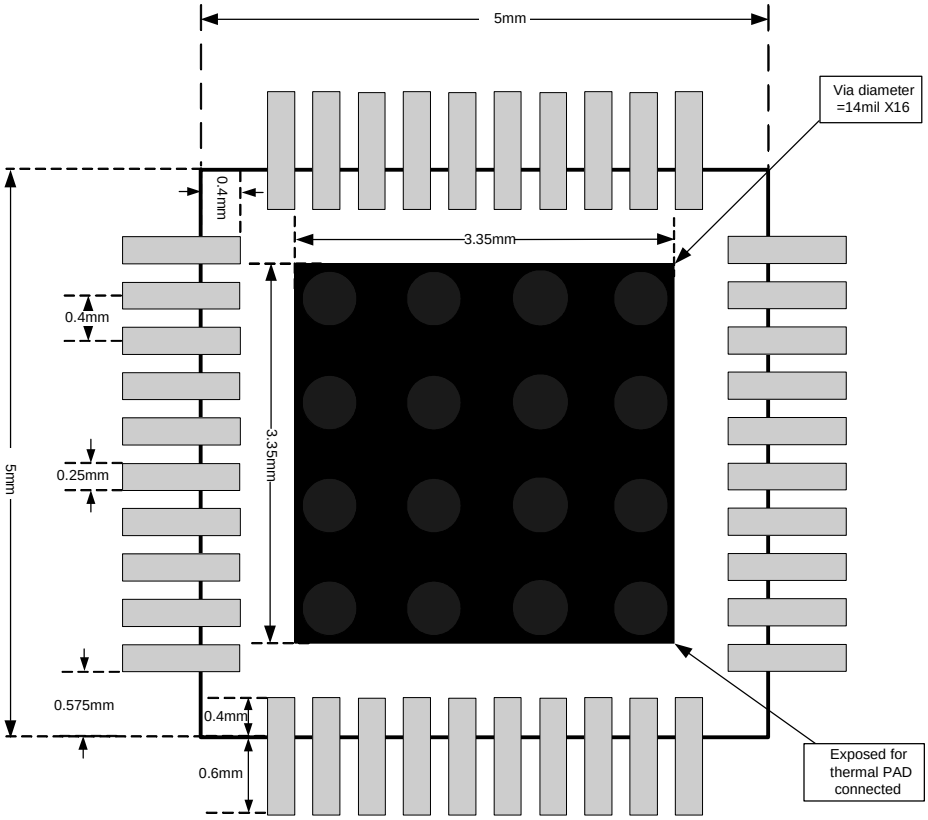


Figure 3. Load Line RC network.

Recommended Minimum Footprint



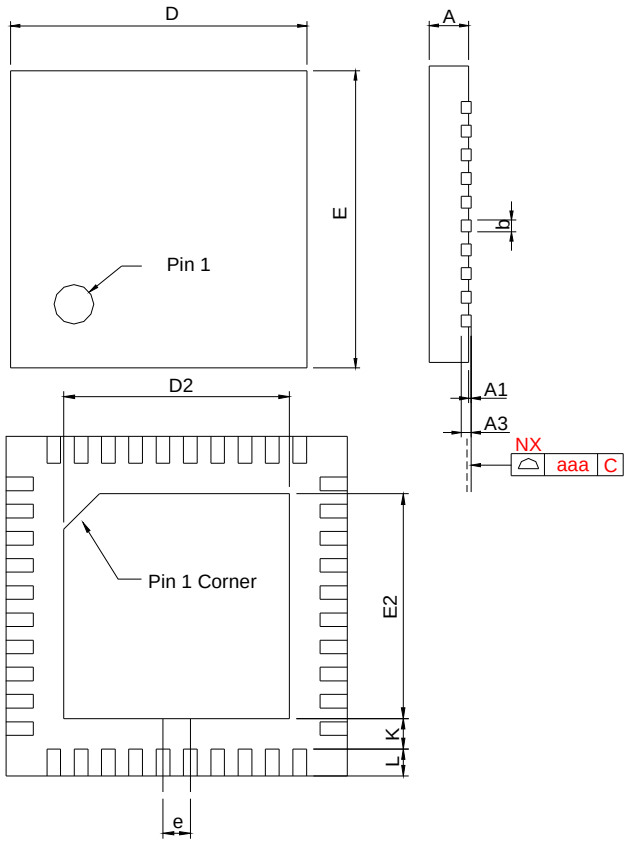
15.Application Information(Cont.)

Layout Consideration

Signal Name	Description	Layout Guidelines
PGND (Thermal Pad)	IC's analog ground.	Connect the GND pad to GND plane through several vias directly.
Each of VR's Input Pins (VSYS, V1P8A_IN, V1P2A_IN, VPP_SW_IN, VPP_LDO_IN)	All VR's input voltage pins.	Place the input capacitors on each of the VR's input pins with low impedance to GND and low impedance to the each of VR's input pins.
Each of PWM VR's LX pins (V1P8A_LX, V1P2A_LX)	These are the connections to the mid point of the power stage consisting of the high- and low-side switch. The output inductor is connected here.	Connect to the output inductor with a short wire. For higher efficiency requirement, the inductor and LX pins should be as close as possible, and the trace resistance from LX pin to inductor should be less than 10mOhm is recommended. Ideally, route the high current path like LX pins to inductors and inductors to output capacitors on the top layer is recommended.
Each of PWM VR's output voltage feedback pins (VNN_FBP, VCCGI_FBP, VCCRAM_FBP, V1P8A_FBP, V1P2A_FBP, VDDQ_FBP)	Voltage feedback pin for each of VR.	The pins are high impedance and sensible to noise from the switch node. The positive feedback signal should be tied to the V+ pad of the output capacitor directly. The feedback pin could be routed to the input capacitor on the load side for remote sense. Coupling from fast switching signals must be avoided.
VR's negative feedback pins (VNN_FBN, VCCGI_FBN)		The pins are high impedance and sensible to noise from the switch node. The negative feedback signal should be tied to the V- pad of the output capacitor directly.
VSYS, VCC	APW8858 input supply voltage.	Connect the input capacitors from VSYS to GND and VCC to GND for noise decoupling. The capacitors and VSYS, VCC pins should be as close as possible.
VNN_PWM, VCCGI_PWM, VCCRAM_PWM, VDDQ_PWM	The gate driver outputs of VNN, VCCGI, VCCRAM and VDDQ.	The traces of PWM signal from the gate driver output pins to the APW870x should be short to eliminate the parasitical capacitance; the parasitical capacitance less than 80pF is recommended.
VTT_IN		This VTT_IN pin is the power supply input pin of VTT LDO and should be connected with VDDQ's output. It happens the neighbor pin is VDDQ_FBP which is also VDDQ's output. However, **DO NOT** connect VTT_IN pin with VDDQ_FBP pin directly. Both VTT_IN and VDDQ_FBP must have their own dedicated path which leads to the output capacitors positive terminal of VDDQ. The VDDQ_FBP is a feedback pin of VDDQ converter and is sensitive to voltage droop, so the VTT_IN is not supposed to draw current directly from VDDQ_FBP pin. Connect VTT_IN with VDDQ output via a trace capable of carrying at least 1A with less than 10mV drop.

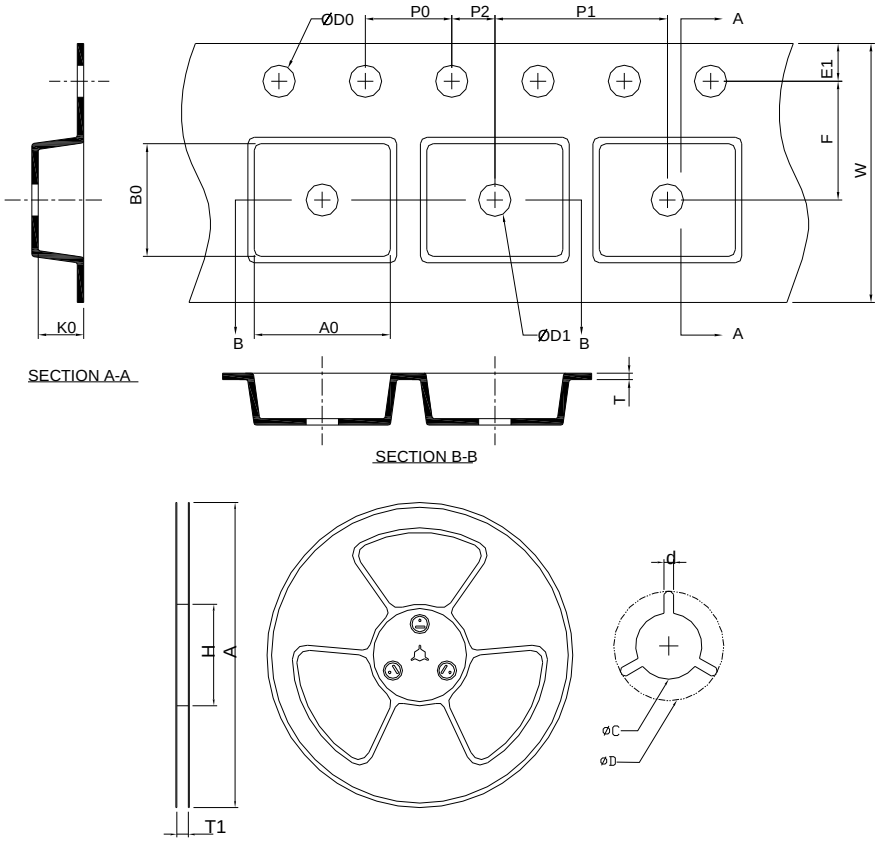
16.Package Information

TQFN5x5-40



SYMBOL	TQFN5*5-40			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	4.90	5.10	0.193	0.201
D2	3.20	3.50	0.126	0.138
E	4.90	5.10	0.193	0.201
E2	3.20	3.50	0.126	0.138
e	0.40 BSC		0.016 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

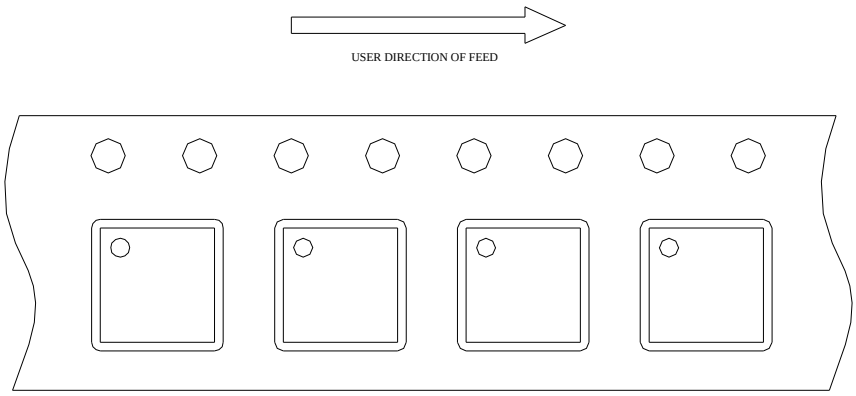
(mm)

Devices Per Unit

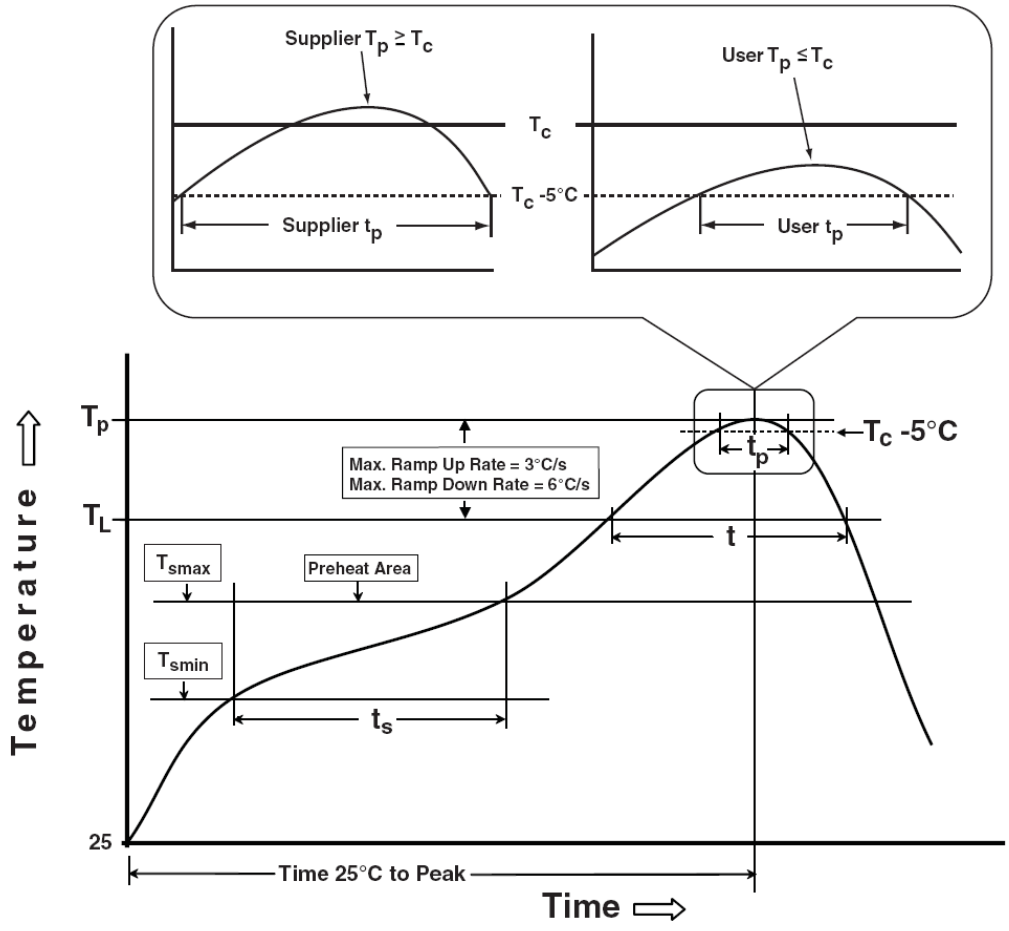
Package Type	Unit	Quantity
TQFN5x5	Tape & Reel	2500

Taping Direction Information

TQFN5x5-40



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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