Datasheet

FS9912

8-bit MCU with 4k program ROM,
128-byte data RAM,
1 low nosie OPAMP,
8-ch 14-bit ADC and 4 × 16LCD drive

Fortune SEMICONDUCTOR CORPORATION

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Contents

1. General Description

The FS9912 is a high performance, low cost CMOS 8-bit single chip microcontroller with embedded a 4kx16 bits ROM, an 8-channel 14-bit fully differential input analog to digital converter, low noise amplifier, and 4x16 LCD driver.

The FS9912 is best suited for applications such as low cost, high performance digital thermometer, ear thermometer, scale, barometer, and hygrometer.

2. Features

- 8-bit microcontroller, 37 single word instructions
- Embedded 4k x 16 program memory, 128-byte data memory
- Voltage operation ranges from 2.4V to 3.6V, 4MHz crystal oscillator
- Operation current is less than 2mA, sleep mode current is about 1μA (LVR disable).
- Low voltage reset (LVR) function mask option. FS9912R_nnnV LVR enable, FS9912_nnnV LVR disable.
- 8-level deep hardware stacks
- 5 Interrupt sources (external: 2, internal: 3)
- 8-channel 14-bit ADC (±400mV input range, ±2LSB linearity error) with 40Hz output rate
- Embedded charge pumper and voltage regulator (4V regulated output)
- Embedded bandgap voltage reference (typical 1.2V±50mV, 100ppm/°C)
- Low noise (1μV Vpp without chopper, 0.5μV Vpp with chopper, 0.1Hz~1Hz) OPAMPs with chopper controller
- 16-bit bidirectional I/O port and buzzer output
- Dual 24-bit programmable timers
- 4 x 16 LCD driver (3V Vpp)
- Watchdog timer

3. Applications

- Ear thermometer
- Thermometer/Hygrometer
- Scale/ Barometer

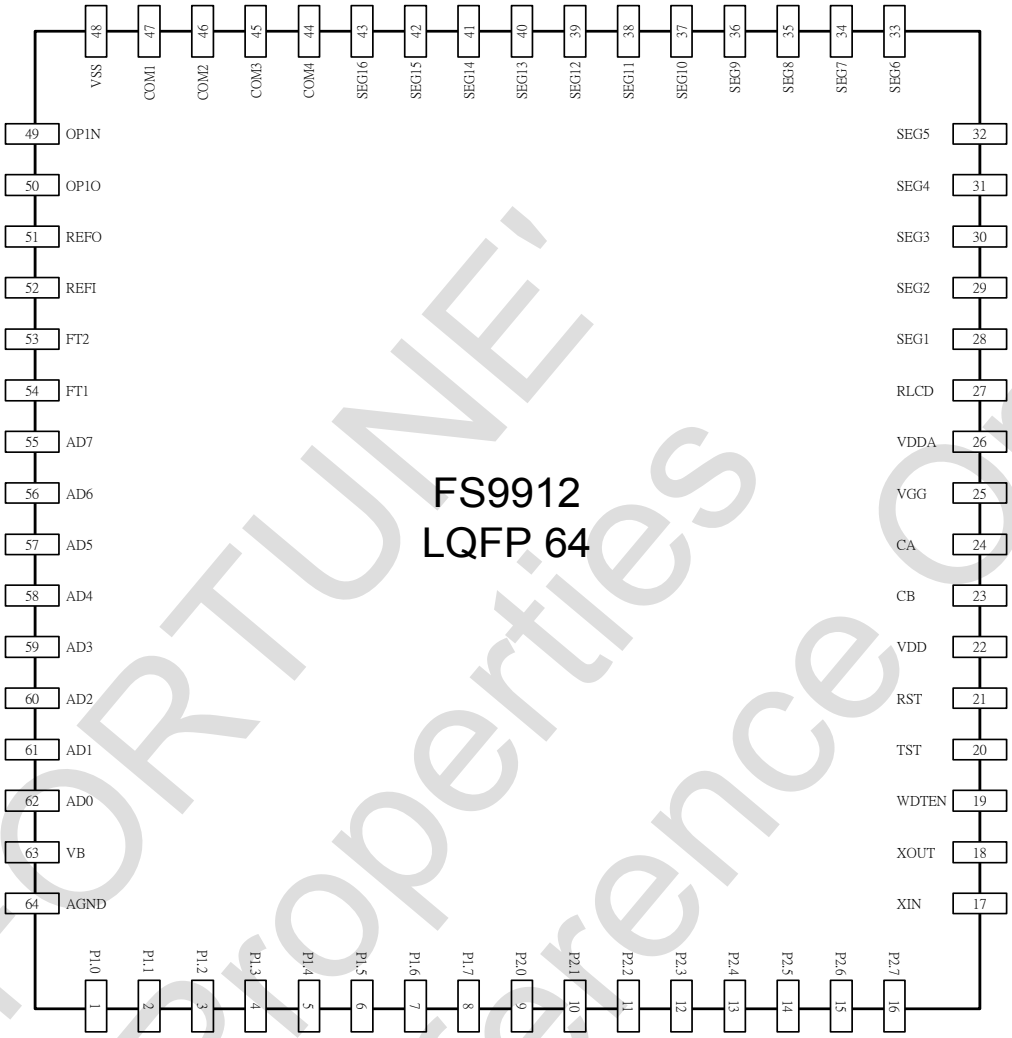
4. Ordering Information

Product Number	Package Type
FS9912-nnnV	Dice form, or 64-pin LQFP
FS9912R-nnnV	Dice form, or 64-pin LQFP

Note1: Code number (nnnV) is assigned for customer; ”nnn” = 001~999; ”V” means Version = A~Z.

Note2: FS9912R_nnnV means LVR enable, FS9912_nnnV means LVR disable.

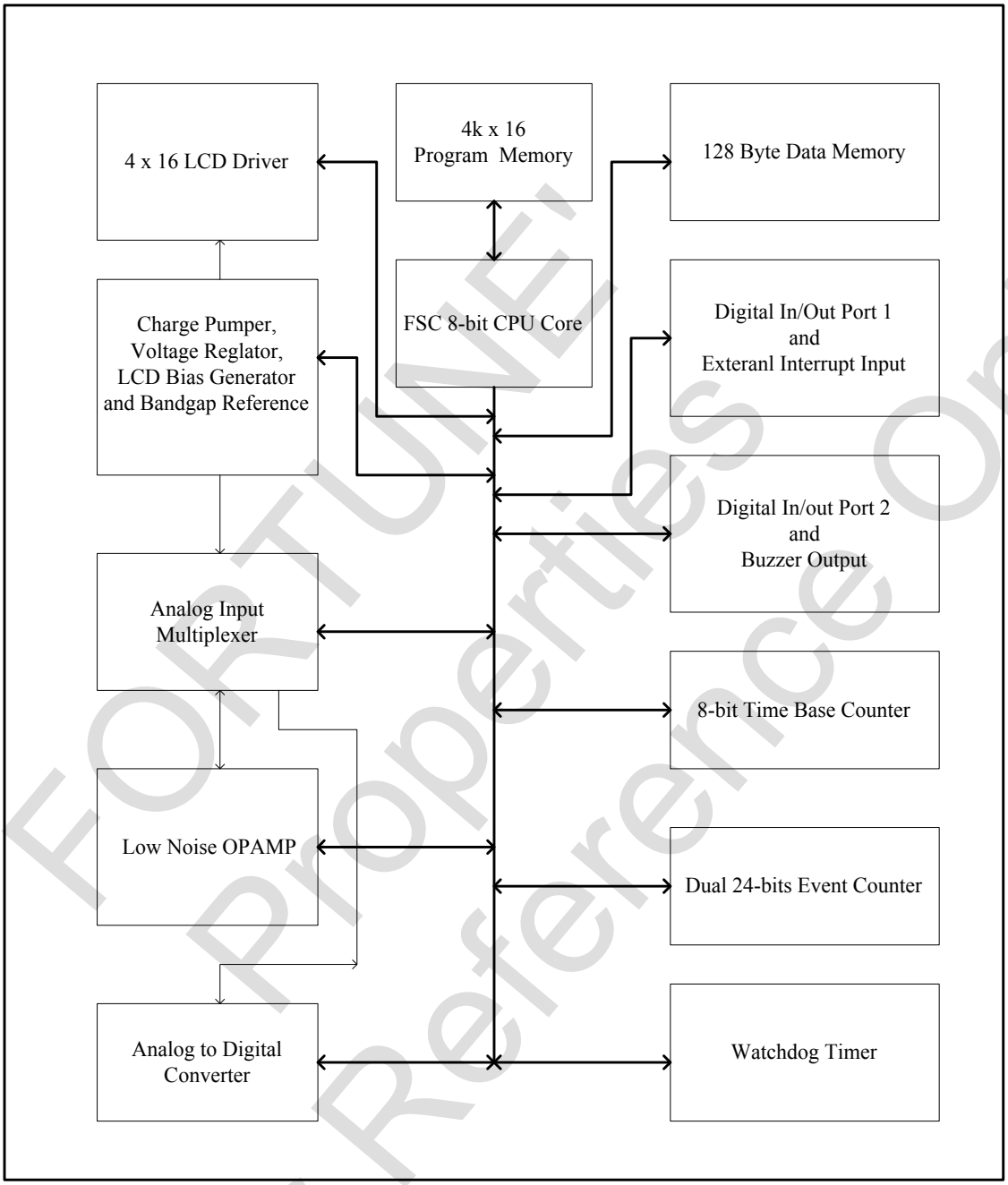
5. Pin Configuration



6. Pin Description

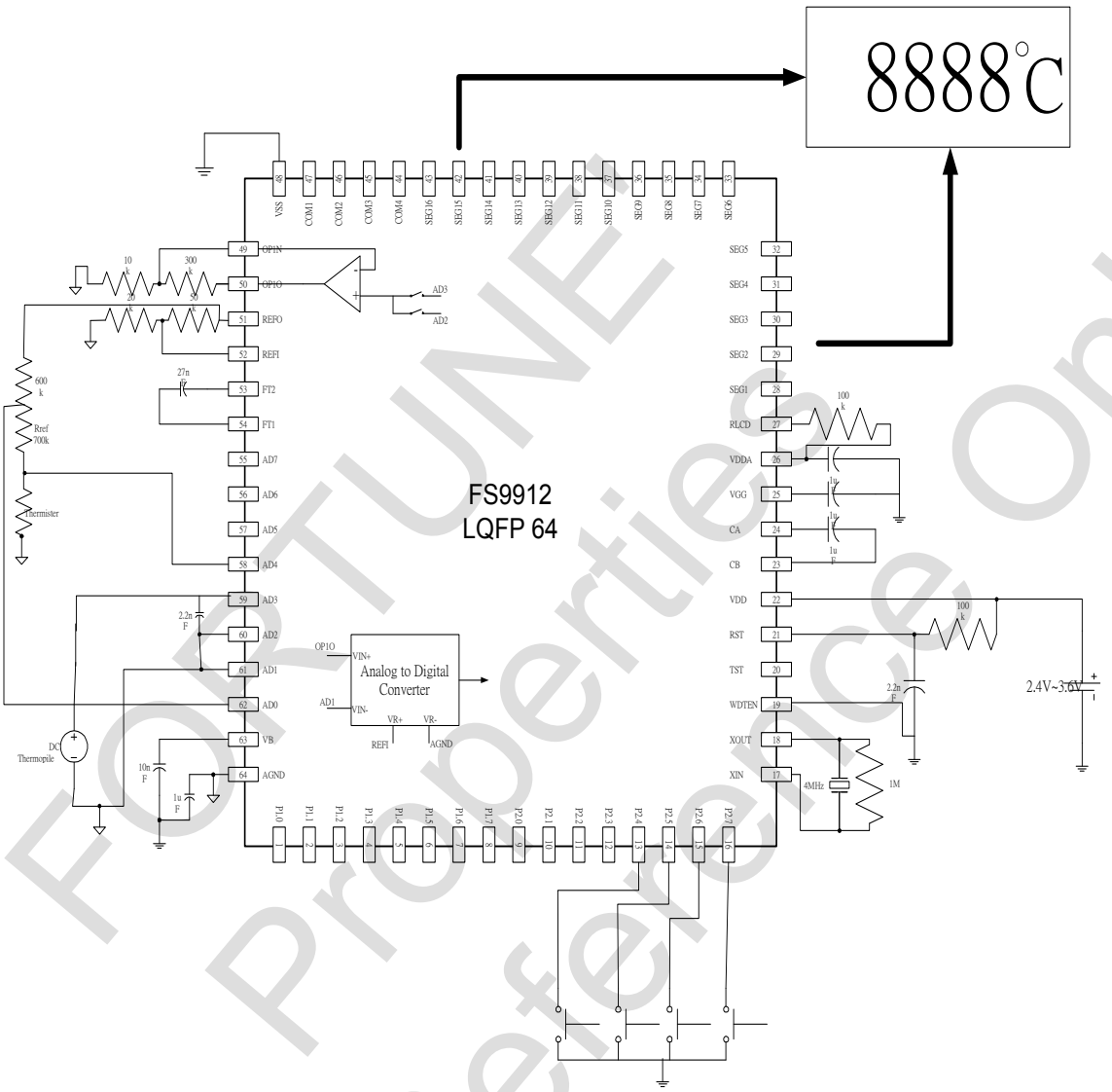
Name	In/Out	Pin No	Description
VDD	I	22	Positive Power Supply
VSS	I	48	Negative Power Supply
AGND	I/O	64	Analog Ground
CB	I/O	23	Charge Pump Capacitor Negative Connection
CA	I/O	24	Charge Pump Capacitor Positive Connection
VGG	I/O	25	Charge Pump Voltage
VDDA	I/O	26	Analog Power Output
RLCD	I/O	27	LCD Bias Voltage Input
XIN	I	17	4MHz Oscillator Input
XOUT	O	18	4MHz Oscillator Output
P1.0~P1.7	I/O	1~8	I/O Port 0
P2.0~P2.7	I/O	9~16	I/O Port 1
SEG1~SEG16	O	28~43	LCD Segment Driver Output
COM1~COM4	O	47~44	LCD Common Driver Output
AD0~AD7	I	62~55	Analog Input Channel
REFO	O	54	Bandgap Reference Output
REFI	I	55	ADC Reference Voltage Input
OP1N	I	49	OPAMP 1 Negative Input
OP1O	I	50	OPAMP 1 Output
FT1, FT2	I/O	54,53	ADC Pre-Filter Capacitor Connection
VB	I	63	Analog Circuit Bias Current Input
RST	I	21	CPU Reset
TST	I	20	Testing Mode
WDTEN	I	19	Watchdog Timer Enable Control

7. Functional Block Diagram

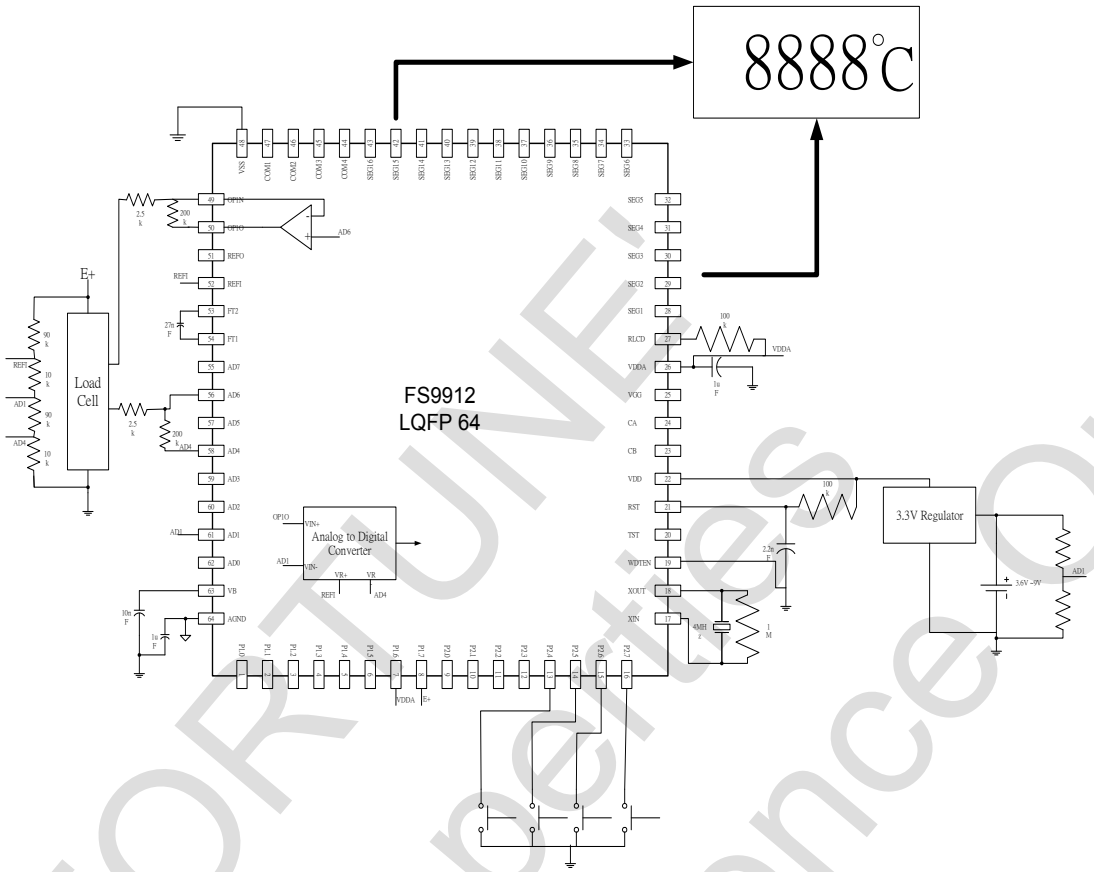


8. Typical Application Circuit

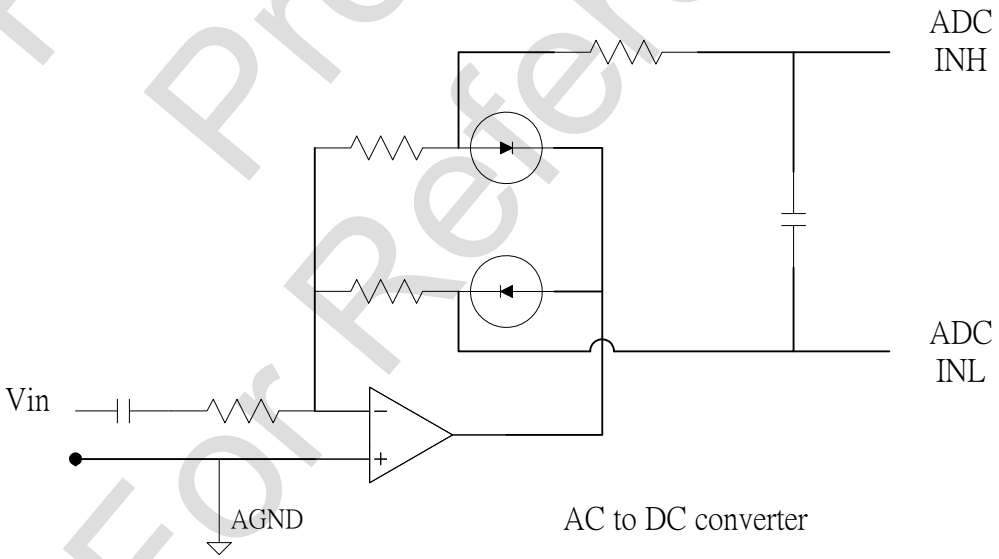
8.1 Application Circuit of Ear Thermometer



8.2 Application Circuit of Scale (Load Cell)



8.3 Reference Circuit of AC To DC Converter



9. Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage to Ground Potential	-0.3 to 5.0	V
Applied Input/Output Voltage	-0.3 to VDD+0.3	V
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C
Soldering Temperature, Time	260°C, 10 Sec	

10. Electrical Characteristics

10.1 DC Characteristic (Unless otherwise specified VDD=3V，Ta=25℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDD	Recommend Operation Power Voltage		2.4		3.6	V
IDD	Supply Current	CPU, ADC On		1.5		mA
IPO1	Power-off Supply Current	At Power Off, LVR disable		1		μA
IPO2	Power-off Supply Current	At Power Off, LVR enable		2		μA
VIH	Digital Input High Voltage		VDD-0.5			V
VIL	Digital Input Low Voltage				0.5	V
Ipu	Pull up Current	Vin=0		5	10	μA
IOH	High Level Output Current	VOH=0.9xVDD		1		mA
IOL	High Level Output Current	VOL=0.1xVDD		2		mA
AGND	Analog Ground Voltage			VDD/2		V
VDDA	Analog Power			4		V
VREF	Build in Reference Voltage	To AGND		1.20		V
VCREF	Build in Reference Voltage Supply Voltage Coefficient	VDD=2.4~3.6	-2000		+2000	ppm/V
TCREF	Build in Reference Voltage Temperature Coefficient	Ta=0~50℃		100		ppm/℃
VLBAT	Low Battery Detector Voltage			2.4		V
FLCD	LCD Frame Frequency			32		Hz
VLCD	LCD Pk-Pk Driver Voltage		2.8	3	3.2	V

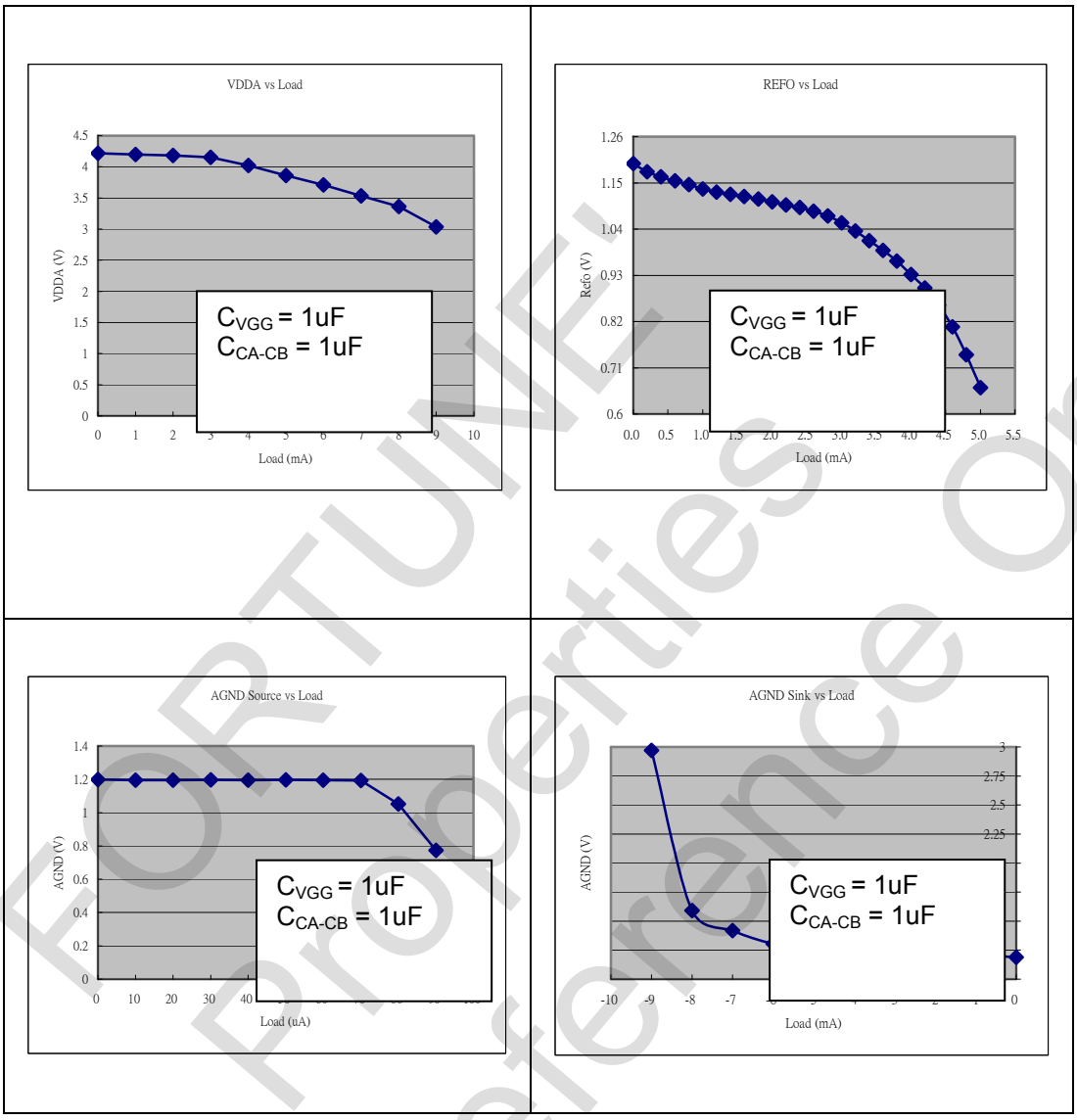
10.2 ADC Characteristic (Unless otherwise specified VDD=3V，Ta=25℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VAIN	ADC Differential Input Range		AGND-0.4	0	AGND+0.4	V
VRFIN	ADC Reference Input Range		0.25		0.5	V
	Resolution			±15625		Counts
	ADC Linearity Error	VRFIN=0.44V	-0.1	0	+0.1	mV
	ADC Input Offset Voltage With Zero Cancellation	VRFIN=0.44V VAIN=0		0		V

10.3 OPAMP Characteristic (Unless otherwise specified VDD=3V，Ta=25℃)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Input Offset			1		mV
	Input Offset Voltage with Zero Cancellation	Rs<100		2		V
	Input Offset Voltage with Chopper	Rs<100		20		V
	Input Offset Drift with Zero Cancellation	-20℃<T_A<+50℃		30		nV/℃
	Input Reference Noise	Rs=100 , 0.1Hz~1Hz		1.0		Vpp
	Input Reference Noise with Chopper	Rs=100 , 0.1Hz~1Hz		0.5		Vpp
	Input Bias Current			10	30	pA
	Input Bias Current with Chopper			100	300	pA
	Input Common Mode Range		0.5		2.4	V
	Output Voltage Range		0.5		2.4	V
	Chopper Clock Frequency			1k		Hz
	Capacitor Load			50	100	pF

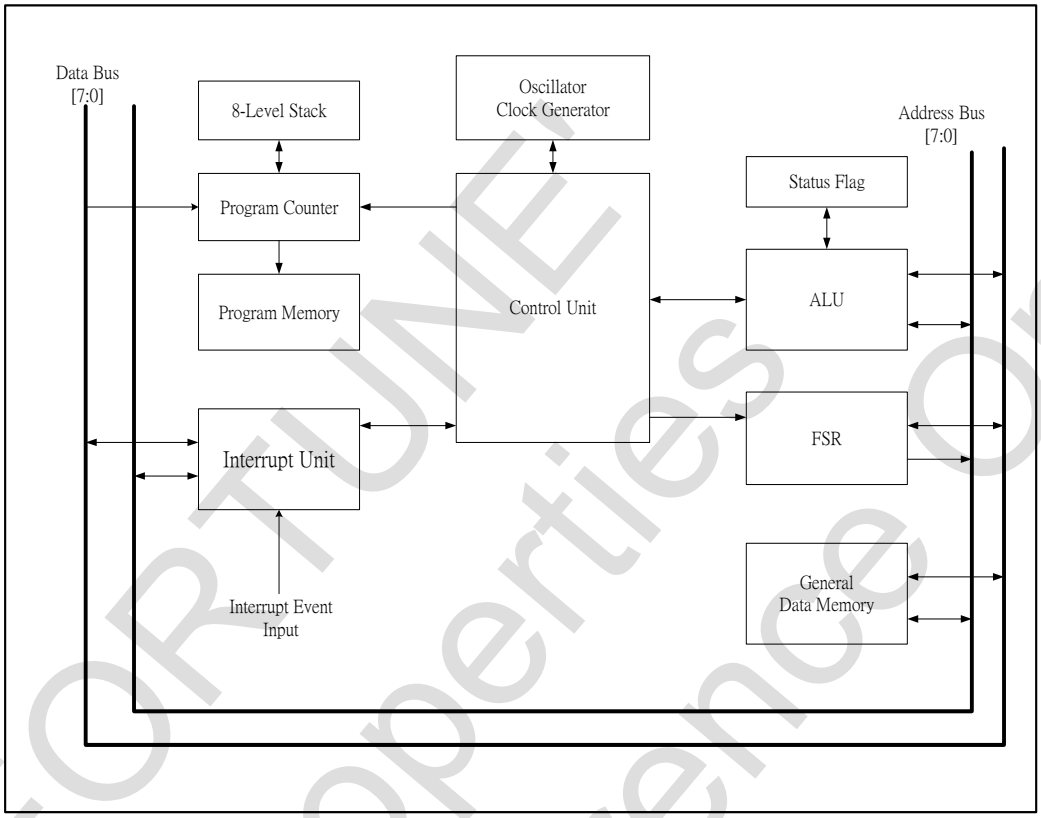
10.4 Typical Performance Characteristics



11. unction Description

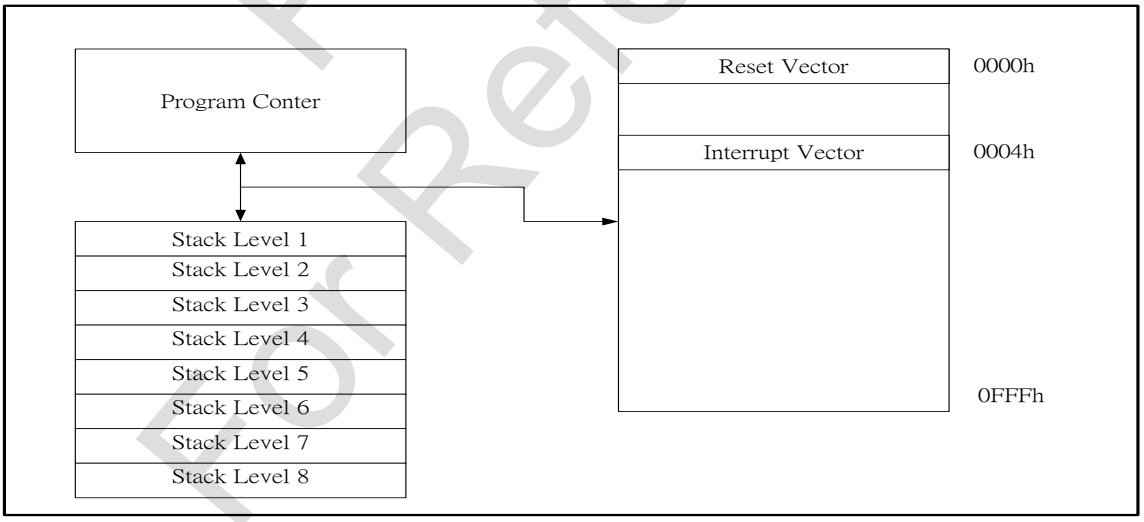
11.1 CPU Core

11.1.1 CPU Core Block Diagram



11.1.2 Program Memory Organization

FS9912 CPU has a 12-bit program counter capable of address an 4k x 16 program memory space. The reset vector is at 0000h and the interrupt vector is at 0004h.



11.1.3 Data Memory Organization

The data memory is partitioned into three parts. The address 00h~07h areas are system special registers, like indirect address, indirect address pointer, status register, working register, interrupt flag, interrupt control register. The address 08h~7Fh areas are peripheral special registers, like I/O ports, timer, ADC, signal conditional network control register, LCD driver… .The address 80h~FFh areas are general data memory.

Name	Address	Content							
IND0	00h	Uses contents of FSR0 to address data memory							
IND1	01h	Uses contents of FSR1 to address data memory							
FSR0	02h	Indirect data memory, address point 0							
FSR1	03h	Indirect data memory, address point 1							
STATUS	04h				PD	TO		C	Z
WORK	05h	WORK register							
INTF	06h				TMIF	PCIF	ADIF	E1IF	E0IF
INTE	07h	GIE			TMIE	PCIE	ADIE	E1IE	E0IE
	08h~7Fh	Peripheral special registers							
	80h~FFh	General data Memory							

- IND0, IND1: indirect addressing mode address
- FSR0, FSR1: indirect addressing mode point
- PD: Power Down Flag. Cleared by writing 0 or power-on reset. Set by sleep instruction
- TO: Watch Dog Time Out Flag. Cleared by writing 0 or power-on reset. Set by Watch Dog Time Out
- C: Carry Flag
- Z: Zero Flag
- E0IF, E0IE: PT1.0 external interrupt flag and enable.
- E1IF, E1IE: PT1.1 external interrupt flag and enable.
- ADIF, ADIE: Analog to digital converter interrupt flag and enable.
- PCIF, PCIE: Program counter interrupt flag and enable.
- TMIF, TMIE: 8-bit Timer interrupt flag and enable.
- GIE: Global interrupt enable.

11.1.4 System Special Register Description

11.1.4.1 Indirect Addressing IND0 and FSR0 Register

The IND0 register is not a physical register. Addressing the IND0 (00h) will cause an indirect addressing. Any instruction using the IND0 register actually accesses data pointed to by the FSR0 register.

A simple program to clear RAM 80h-FFh using indirect addressing is shown in following:

```
      MOVLW  080h
      MOVWF  FSR0
NEXT: CLRF   IND0
      INCFSZ  FSR0, 1
      GOTO NEXT
```

11.1.4.2 Status Register

- C： bit 1 R/W Carry Flag or (~Borrow).
- Z： bit 0 R/W Zero Flag, set if ALU operation is zero. Reset otherwise.

Two simple examples to illustrate the relation between carry flag and arithmetic instructions.

```
Example 1
M (80h) = 3Fh   M (81h) = F0h   WORK = 99h
ADDWF   80h, 1    ; 3Fh+99h=D8h   DC=1, C=0, Z=0
ADDWF   81h, 1    ; F0h+99h=89h   DC=0, C=1, Z=0
SUBWF   80h, 1    ; 3Fh-99h=A6h DC=1, C=0, Z=0
SUBWF   81h, 1    ; F0h-99h=57h DC=0, C=1, Z=0
```

Example 2 16-bit add: {M (83h), M (82h)} = {M (83h), M (82h)} + {M (81h), M (80h)} 16-bit sub: {M (83h), M (82h)} = {M (83h), M (82h)} - {M (81h), M (80h)}

add:
MOVFW 80h
ADDWF 82h, 1
MOVFW 81h
ADDWFC 83h, 1
 	
sub:
MOVFW 80h
SUBWF 82h, 1
MOVFW 81h
SUBWFC 83h, 1

11.1.4.3 Interrupt Flag INTF and Interrupt enable register INTE

The interrupt enable register (INTE) records individual interrupt request .When Interrupt event occur and Interrupt enable bit =1 , the interrupt flag will be set。The global interrupt enable bit (GIE) will enable CPU interrupt procedure. When GIE=1 and any interrupt flag is set, CPU interrupt procedure would be executed. CPU interrupt procedure executes GIE reset and CALL 0004h.

Note. When interrupt signal happened within Instruction Duty Cycle, the CPU must wait and till Instruction Duty Cycle end of this program then produce an “Interrupt Flag” before go into next step.

11.1.5 Instruction Set

Instruction	Operation	Cylce	Flag
NOP	No operation	1	None
CLRF f	f=0	1	Z
ADDWF f, d	d=f+W	1	C, Z
INCF f, d	d=f+1	1	Z
INCFSZ f, d	d=f+1 skip if d=0	1,2	None
DECF f, d	d=f-1	1	Z
DECFSZ f, d	d=f-1 skip if d=0	1,2	None
SUBWF f, d	d=f-W	1	C, Z
COMF f, d	d=~f	1	Z
MOVWF f	f=W	1	None
MOVFW f	W=f	1	None
ADDWFC f, d	d=f+W+C	1	C, Z
ANDWF f, d	d=f&W	1	Z
IORWF f, d	d=f|W	1	Z
XORWF f, d	d=f^W	1	Z
RLF f, d	C, d [7:0]=f [7:0], C	1	C
SUBWFC f, d	d=f-W- (~C)	1	C, Z
RRF f, d	d [7:0], c=C, f [7:0]	1	C
ADDLW k	W=k+W	1	C, Z
SUBLW k	W=k-W	1	C, Z
ANDLW k	W=k&W	1	Z
IORLW k	W=k|W	1	Z
XORLW k	W=k^W	1	Z
MOVLW k	W=k	1	None
RETLW k	RETURN and W=k	2	None
CALL k	Push PC+1 and GOTO k	2	None
GOTO k	PC=k	2	None
RETFIE	Pop PC and GIE=1	2	None
RETURN	Pop PC	2	None

HALT	Stop uP clock	1	None
SLEEP	Stop OSC	1	PD
CLRWDT	Clear watch dog timer	1	None
ADDPCW	PC=PC+1+{6{W [7], W [6:0]}	2	None
BCF f, b	f [b]=0	1	None
BSF f, b	f [b]=1	1	None
BTFSC f, b	Skip if f[b]=0	1,2	None
BTFSS f, b	Skip if f[b]=1	1,2	None

- f : memory address (0h ~ FFh)
- w: work register
- k : literal field , constant data or label
- d: destination select : d=0 store result in W, d=1: store result in memory address f.
- b: bit select(0~7)
- M(f): the content of memory address f
- PC: program counter

11.1.6 Instruction Description

NOP	**No Operation**
Syntax	NOP
Operation	No Operation
Status Affected	None
Description	No operation. NOP is used for one instruction cycle delay.

CLRF	**Clear f**
Syntax	CLRF f
Operation	0 => M (f)
Status Affected	1=> Z
Description	Reset memory address f content.

ADDWF	**Add W to f**
Syntax	ADDWF f, d
Operation	W + M (f) => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCF	**Increment f**
Syntax	INCF f, d
Operation	M (f) + 1 => (destination)
Status Affected	Z
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

INCFSZ	**Increment f, skip if zero**
Syntax	INCFSZ f, d
Operation	M (f) + 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is incremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

DECF	**Decrement f**
Syntax	DECF f, d
Operation	M (f) - 1 => (destination)

Status Affected	Z
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

DECFSZ	**Decrement f, skip if zero**
Syntax	DECFSZ f, d
Operation	M (f) - 1 => (destination), skip if result is zero
Status Affected	None
Description	M (f) is decremented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f). If the result is 0, then the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

SUBWF	**Subtract W from f**
Syntax	SUBWF f, d
Operation	M (f) + NOT (W) + 1 => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f),

COMF	**Complement f**
Syntax	COMF f, d
Operation	NOT (M (f)) => M (f)
Status Affected	Z
Description	M (f) is complemented. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f)

MOVWF	**Move W to f**
Syntax	MOVWF f
Operation	W => M (f)
Status Affected	None
Description	Move data from the W register to M (f).

MOVFW	**Move f to W**
Syntax	MOVFW f
Operation	M (f) => W
Status Affected	None
Description	Move data from M (f) to the W register.

ADDWFC	**Add W, f and Carry**
Syntax	ADDWFCf, d
Operation	W + M (f) + C => (destination)
Status Affected	DC, C, Z
Description	Add the content of the W register, M (f) and Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ANDWF	**And W and f**
Syntax	ANDWF f, d
Operation	W AND M (f) => (destination)
Status Affected	Z
Description	AND the content of the W register with M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

IORWF	**Inclusive OR W and f**
Syntax	IORWFf, d
Operation	W OR M (f) => (destination)
Status Affected	Z
Description	Inclusive OR the content of the W register and M (f). If d is 0, the result is stored in

	the W register. If d is 1, the result is stored back in M (f).

XORWF	**Exclusive OR W and f**
Syntax	XORWF f, d
Operation	W XOR M (f) => (destination)
Status Affected	Z
Description	Exclusive OR the content of the W register and M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RLF	**Rotate left M (f) through Carry**
Syntax	RLF f, d
Operation	M (f) [6:0], C => (destination)
Status Affected	C
Description	M (f) is rotated one bit to the left through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

SUBWFC	**Subtract W and Carry from f**
Syntax	SUBWFC f, d
Operation	M (f) + NOT (W) + C => (destination)
Status Affected	DC, C, Z
Description	Subtract the content of the W register from M (f). If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

RRF	**Rotate right M (f) through Carry**
Syntax	RRF f, d
Operation	C, M (f) [7:1] => (destination)
Status Affected	C
Description	M (f) is rotated one bit to the right through the Carry bit. If d is 0, the result is stored in the W register. If d is 1, the result is stored back in M (f).

ADDLW	**ADD literal to W**
Syntax	ADDLW k
Operation	W + k => W
Status Affected	DC, C, Z
Description	Add the content of the W register and the eight-bit literal "k". The result is stored in the W register.

SUBLW	**Subtract literal from W**
Syntax	SUBLW k
Operation	k + NOT (W) + 1 => W
Status Affected	DC, C, Z
Description	Subtract the eight-bit literal "k" from the content of the W register. The result is stored in the W register.

ANDLW	**AND literal with W**
Syntax	ANDLW k
Operation	W AND k => W
Status Affected	Z
Description	AND the content of the W register with the eight-bit literal "k". The result is stored in the W register.

IORLW	**Inclusive OR literal with W**
Syntax	IORLW k
Operation	W OR k => W
Status Affected	Z
Description	Inclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

XORLW	Exclusive OR literal with W
Syntax	XORLW k
Operation	W XOR k => W
Status Affected	Z
Description	Exclusive OR the content of the W register and the eight-bit literal "k". The result is stored in the W register.

MOVLW	Move literal to W
Syntax	MOVLW k
Operation	k => W
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register.

RETLW	Return and move literal to W
Syntax	RETLW k
Operation	k => W [Top Stack] => PC Pop Stack
Status Affected	None
Description	Move the eight-bit literal "k" to the content of the W register. The program counter is loaded from the top stack, then pop stack.

CALL	Subroutine CALL
Syntax	CALL k
Operation	Push Stack PC + 1 => [Top Stack] k => PC
Status Affected	None
Description	Subroutine Call. First, return address PC + 1 is pushed onto the stack. The immediate address is loaded into PC.

GOTO	Unconditional Branch
Syntax	GOTO k
Operation	k => PC
Status Affected	None
Description	The immediate address is loaded into PC.

Return	Return from Subroutine
Syntax	RETURN
Operation	[Top Stack] => PC Pop Stack
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack.

RETFIE	Return from Interrupt
Syntax	RETFIE
Operation	[Top Stack] => PC Pop Stack 1 => GIE
Status Affected	None
Description	The program counter is loaded from the top stack, then pop stack. Setting the GIE bit enables interrupts.

ADDPCW	ADD W to Program Counter
Syntax	ADDPCW
Operation	PC + 1 + W => PC
Status Affected	None
Description	The relative address PC + 1 + W is loaded into PC. The working register must less than 80h (128d).

HALT	Stop CPU Core Clock
Syntax	HALT
Operation	CPU Stop
Status Affected	None
Description	CPU clock is stopped. Oscillator is running. CPU can be waked up by internal and external interrupt sources.

SLEEP	Oscillator stop
Syntax	SLEEP
Operation	CPU oscillator is stopped
Status Affected	PD
Description	CPU oscillator is stopped. CPU can be waked up by external interrupt sources.

PS. Please make sure all interrupt flags are cleared before running SLEEP; "NOP" command must follow HALT and SLEEP commands.

CLRWDT	Clear watch dog timer counter
Syntax	CLRWDT
Operation	Watch dog timer counter will reset
Status Affected	None
Description	CLRWDT instruction will reset watch dog timer counter.

BSF	Bit Set f
Syntax	BSF f, b
Operation	1 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is set to 1.

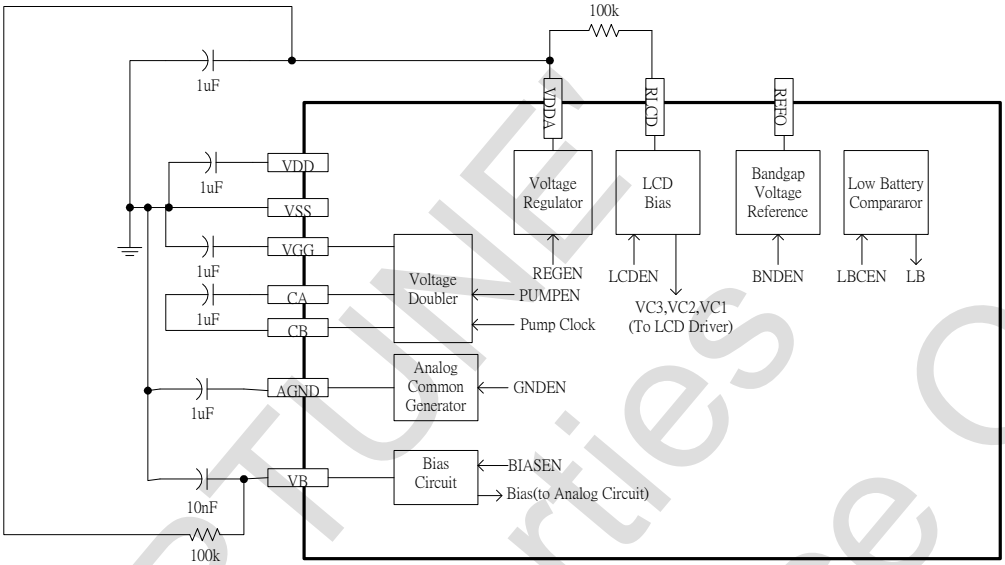
BCF	Bit Clear f
Syntax	BCF f, b
Operation	0 => M (f) [b]
Status Affected	None
Description	Bit b in M (f) is reset to 0.

BTFSC	Bit Test skip if Clear
Syntax	BTFSCf, b
Operation	Skip if M (f) [b] = 0
Status Affected	None
Description	If bit 'b' in M (f) is 0, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

BTFSS	Bit Test skip if Set
Syntax	BTFSSf, b
Operation	Skip if M (f) [b] = 1
Status Affected	None
Description	If bit 'b' in M (f) is 1, the next fetched instruction is discarded and a NOP is executed instead making it a two-cycle instruction.

11.2 Power System

Address	Name	Content							
02CH	NETD	PUMPEN		LBCEN	BNDEN	LCDEN	REGEN	GNDEN	BIASEN
02DH	SVD								LB

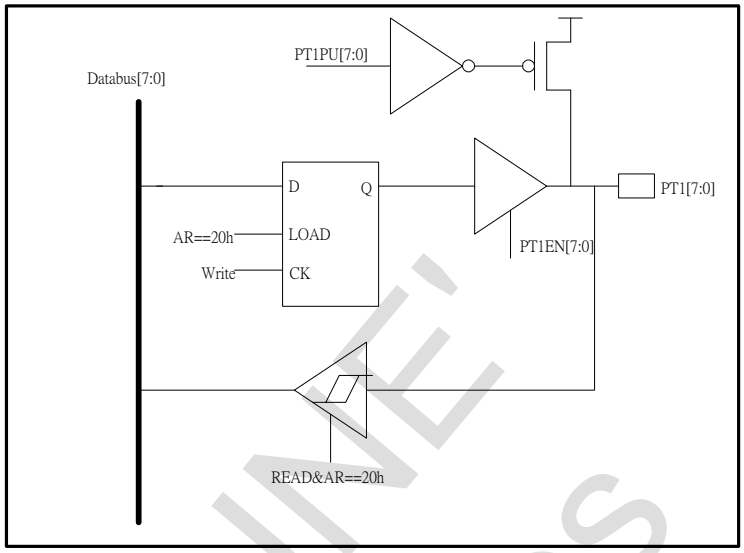


- BIASEN=1 will start the bias circuit of the analog circuit. When power on reset, BIASEN is 0
- GNDEN=1 will start the internal analog common generator circuit, and the AGND voltage is about (vdd, vss)/2.
- PUMPEN=1 will start the voltage doubler circuit. VGG voltage is about 2VDD.
- PMPS (PT2MR [0]) will set the voltage doubler operation frequency: 0 is 2.7kHz, and 1 is 10kHz.
- REGEN=1 will start the internal voltage regulator. VDDA voltage is about 4V.
- LCDEN=1 will start the LCD driver bias circuit. The LCD bias voltages are RLCD, 2/3RLCD, 1/3RLCD, and vss respectively.
- BNDEN=1 will start the internal bandgap voltage reference. The output voltage (REFO, AGND) is about 1.2V.
- LBCEN=1 will start the low battery check comparator. The comparator inputs are VDD and REFO respectively, and the low battery check voltage is about 2.4V.

11.3 I/O Port

11.3.1 I/O Port1(PT1)

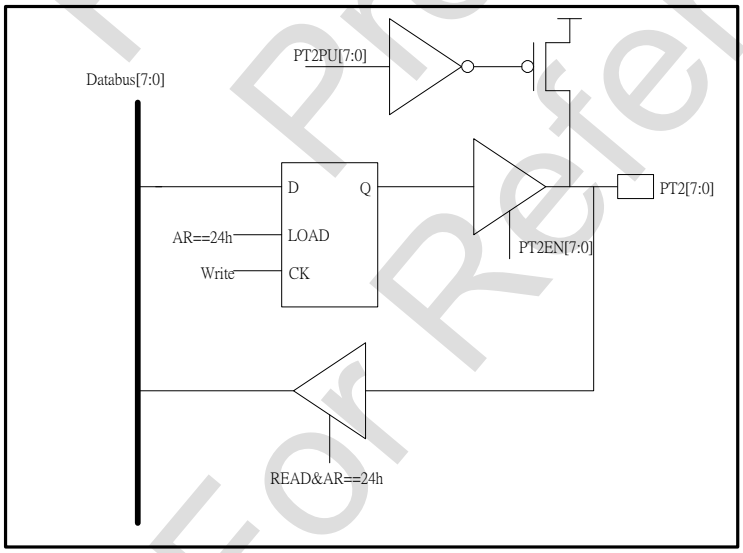
Address	Name	Content							
020H	PT1	PT1 [7:0]							
021H	PT1EN	PT1EN [7:0]							
022H	PT1PU	PT1PU [7:0]							
023H	PT1MR					E1M1	E1M0	E0M1	E0M0



- PT1 is I/O port with pull-up resistor enable control.
- PT1EN [N] =0: PT1 [N] is as input port, 1: PT1 [N] is as output port, system reset is 0.
- PT1PU [N]=0: PT1 [N] without pull-up resistor, 1: PT1 [N] with pull-up resistor, system reset is 0.
- PT1 [1] PT1 [0] can be as external interrupt sources. Interrupt mode is controlled by E1M, E0M. 00:
- negative edge, 01: positive edge, 10&11: interrupt when change.
- PT1 has Schmitt-trigger input

11.3.2 I/O Port2 (PT2)

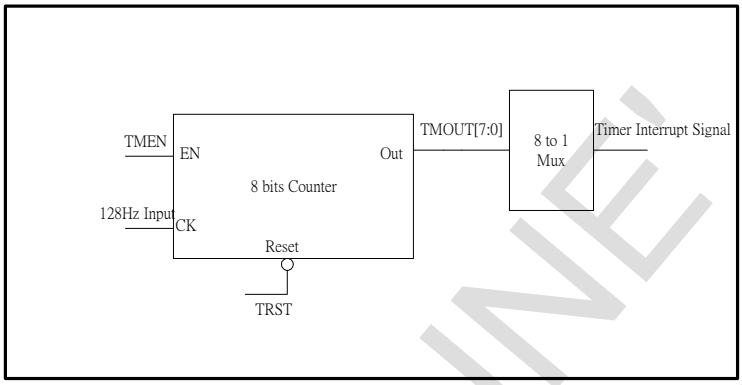
Address	Name	Content							
024H	PT2	PT2 [7:0]							
025H	PT2EN	PT2EN [7:0]							
026H	PT2PU	PT2PU [7:0]							
027H	PT2MR	BPE2	BPE1			OPC1	OPC0	BPS	PMPS



- PT2 is I/O ports with pull-up resistor enable control.
- PT2EN [N] =0: PT2 [N] is as input port, 1: PT2 [N] is as output port, system reset is 0.
- BPE2 =1 & PT2EN [7]=1: PT2 [7] as buzzer output. BPE1=1 & PT2EN [6]=1: PT2 [6] as inverter buzzer
- output. BPS=1: buzzer frequency=4kHz, BPS=0 buzzer frequency=2.7kHz.

11.4 8 Bits Timer

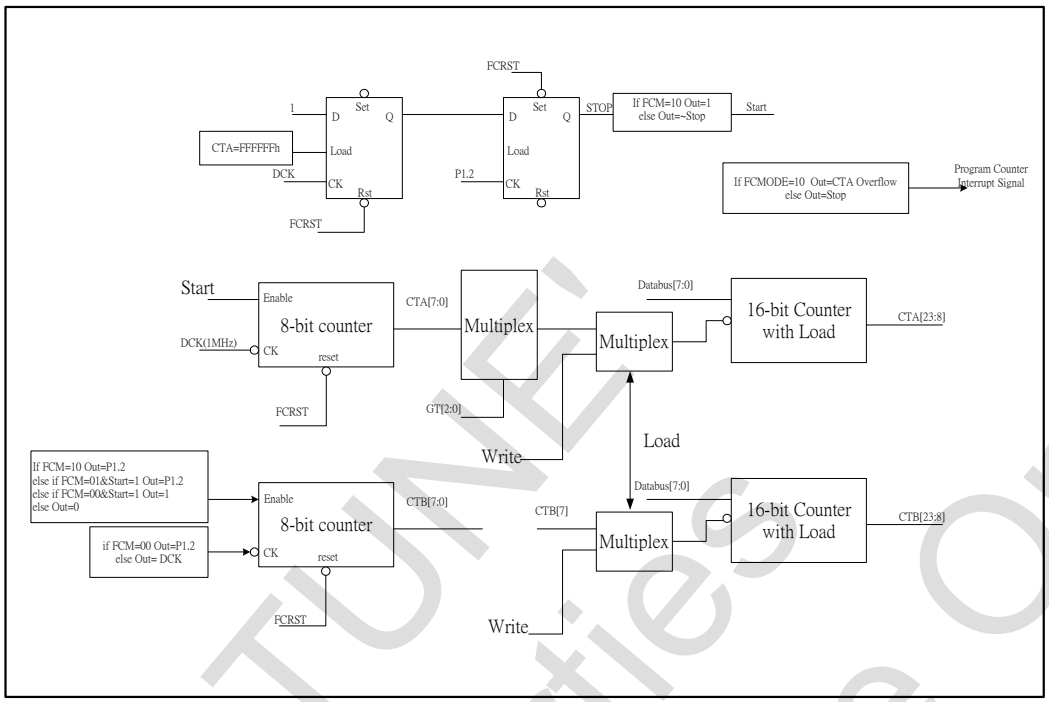
Address	Name	Content							
00CH	TMOUT	TMOUT [7:0]							
00DH	TMCON	TRST	WTS2	WTS1	WTS0	TMEN	INS2	INS1	INS0



- Write a “0” to bit 7 of address 0Dh, the CPU will send a low pulse to TRST and reset the 8-bit counter. Then read bit 7 of 0DH to get “1”.
- TMEN=1, the 8-bit counter will be enabled. TMEN=0, the 8-bit counter will stop.
- INS [2:0] selects timer interrupt source. The selection codes are as follows, 000: TMOUT [0], 001 TMOUT [1], 010: TMOUT [2], 011: TMOUT [3], 100: TMOUT [4], 101: TMOUT [5], 110: TMOUT [6], 111: TMOUT [7].
- TMOUT [7:0] is the output of the 8-bit counter. It is read-only.

11.5 Dual 24 Bit Programmable Counter

Address	Name	Content							
014H	CTAH	CTA [23:16]							
015H	CTAM	CTA [15:8]							
016H	CTAL	CTA [7:0]							
017H	CTBH	CTB [23:16]							
018H	CTBM	CTB [15:8]							
019H	CTBL	CTB [7:0]							
01AH	FQCON		LOAD	FCM1	FCM0	FCRST	GT2	GT1	GT0



- Under modes FCM=00 and 01, we can set Load=1 to load data into CTA [23:8] and simultaneously set GT. When Load=0 and FCRST=1, CTA and CTB will start counting after the first positive edge signal from input PT1.2. The counters will not stop counting until CTA overflows and after the first positive edge signal from input PT1.2, and then the system will send out an interrupt signal. Therefore, we can count the cycles of PT1.2 input signal to calculate the high-resolution frequency and duty cycle of the low frequency input signal by the following calculation approach.
- Under mode FSM=10, CTA and CTB start counting when FCRST=1. The counters will not stop counting until CTA overflows, and then the system will send out an interrupt signal. The calculating flows and methods are described as follows:

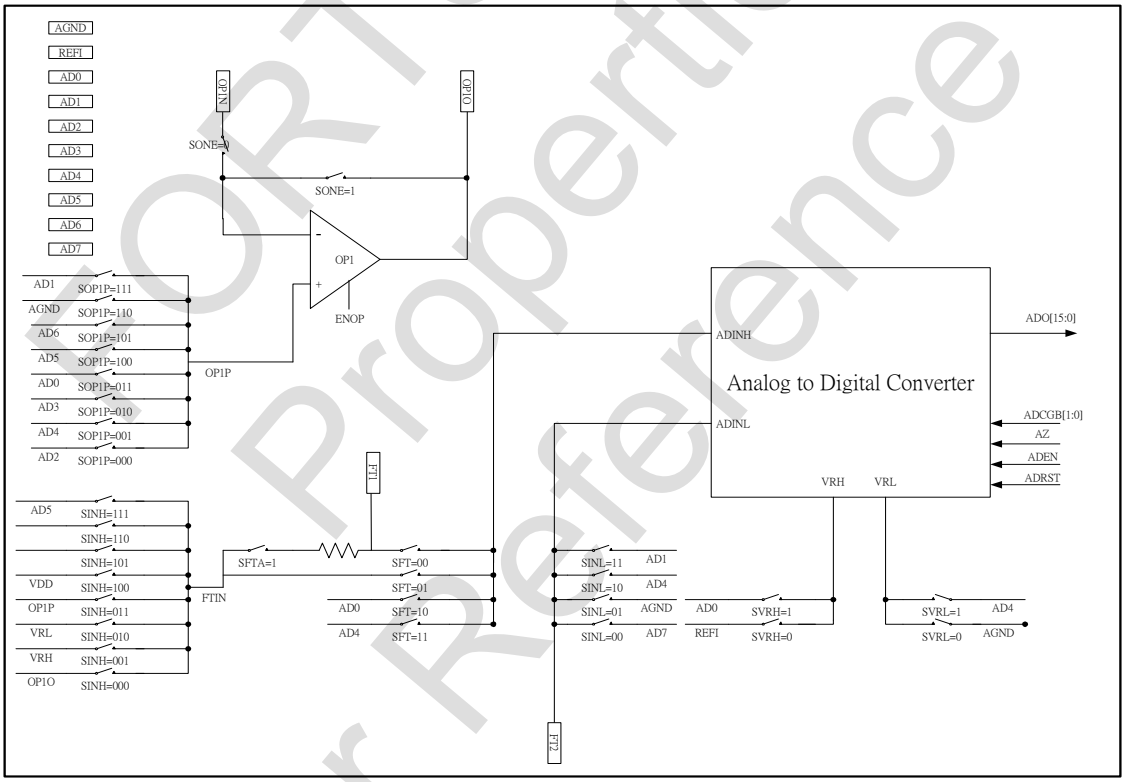
A. Frequency Measurement Mode: FCM=00
   a. Load=1, FCRST=0
   b. Write 14h and 15h to CTA [23:8] to set initial value of CTAI.
   c. Set GT [2:0] to select the length of counter CTA. GT=000 sets CTA [23:8] as a 16-bit counter and CTA [7] is as the clock input; CTA [23:0] is a 24-bit counter. GT=111 sets CTA [23:8] as a 16-bit counter and CTA [0] is as the clock input; {CTA [23:8], CTA[0]} is set as a 17-bit counter.
   d. Gate Time = (1000000h-CTAI x 256) x 1us … if GT=000
   e. Set LOAD=0, FCRST=1, and P1.2 frequency starts measuring.
   f. Wait till positive edge of P1.2, then Start=1 and CTA and CTB start counting.
   g. Wait till CTA overflows and at the next positive edge of P1.2, then Start=0 and CTA and CTB stop counting.
   h. When the CPU receives interrupt signal, the CPU will read CTA and CTB. Here CTA is the reference clock counter, and CTB is the input clock counter
   i. Frequency of P1.2 is 1MHz x CTB/(CTA+CTAI). Go to “a” for next measurement.

B. Duty Cycle Measurement Mode: FCM=01
   a. Load=1, FCRST=0
   b. Write 14h and 15h to CTA [23:8] to set initial value of CTAI.
   c. Set GT [2:0] to select the length of counter CTA. GT=000 sets CTA [23:8] as a 16-bit counter and CTA [7] is as the clock input; CTA [23:0] is a 24-bit counter. GT=111 sets CTA [23:8] as a 16-bit counter and CTA [0] is as the clock input; {CTA [23:8], CTA [0]} is set as a 17-bit counter.
   d. Gate Time = (1000000h-CTAI x 256) x 1us … if GT=000

e. Set LOAD=0, FCRST=1, and P1.2 frequency starts measuring.
f. Wait till positive edge of P1.2, then Start=1 and CTA and CTB start counting.
g. Wait till CTA overflows and at the next positive edge of P1.2, then Start=0 and CTA and CTB stop counting.
h. When the CPU receives interrupt signal, the CPU will read CTA and CTB. Here CTA is the reference clock counter, and CTB counts when P1.2=1.
i. The duty cycle of P1.2 is 100% x CTB/(CTA+CTAI). Go to “a” for next measurement.

C. Timer Mode: FCM=10
a. Load=1, FCRST=0
b. Write 14h and 15h to CTA [23:8] to set initial value of CTAI.
c. Set GT [2:0] to select the length of counter CTA. GT=000 sets CTA [23:8] as a 16-bit counter and CTA [7] is as the clock input; CTA [23:0] is a 24-bit counter. GT=111 sets CTA [23:8] as a 16-bit counter and CTA [0] is as the clock input; {CTA [23:8], CTA [0]} is set as a 17-bit counter.
d. Gate Time = (1000000h-CTAI x 256) x 1us … if GT=000
e. When CTA overflows, then send interrupt signal to the CPU.
f. If CPU receives interrupt signal, then Go to “a”.

11.6 Measurement Part Block Diagram



11.7 ADC

Address	Name	Content							
010H	ADOH	ADO [15:8]							
011H	ADOL	ADO [7:0]							
013H	ADCON						ADRST		
02BH	NETC			ADG1	ADG0	ADEN	AZ		

■ The ADC (analog to digital converter) contains Σ-Δ modulator and digital comb filter. When ADRST=1, comb filter will be enabled. When ADRST=0, the comb filter will be reset. ADEN=1 starts the S-D

modulator.

- ADO is the ADC output. The maximum value is 3D09h and the minimum is C2F7h (-3D09h). FFFF means (-0001).
- The output rate of the ADC is 40Hz. When the output data are updated, the interrupt signal is sent to the CPU. If ADIE=1, then ADIF is set to 1.
- AZ=0 means that the ADC differential inputs are (INH, INL); AZ= 1 means that the ADC differential inputs are (INL,INL). We can use this mode to measure the ADC offset.
- ADCGB [1:0] will set ADC input gain as follows, 00: 2/3, 01: 1, 10: 2, 11: 2 1/3.

11.8 Analog Multiplex

Address	Name	Content							
029H	NETA	SINL1	SINL0	SINH2	SINH1	SINH0	SOP1P2	SOP1P1	SOP1P0
02AH	NETB	SVRH	SVRL		ENOP	SONE	SFTA	SFT1	SFT0

OP1P: OP1 Positive Input

SOP1O	000	001	010	011	100	101	110	111
Select	AD2	AD4	AD3	AD0	AD5	AD6	AGND	AD1

FTIN: Low Pass Filter Input

SINH	000	001	010	011	100	101	110	111
Select	OP1O	VRH	VRL	OP1P	VDD			AD5

ADINL: ADC Negative Input

SINL	00	01	10	11
Select	AD7	AGND	AD4	AD1

4. ADINH: Filter Output, ADC Positive Input

SFT [1:0]	00	01	10	11
Select	FT1	FTIN	AD0	AD4

VRH: ADC Reference Voltage Positive Input

SVRH	0	1
Select	REFI	AD0

VRL: ADC Reference Voltage Negative Input

SVRL	0	1
Select	AGND	AD4

External Filter Control: SFTA=0: FTIN and FT1 open. SFTA=1: FTIN and FT1 short.

11.9 Low Noise OPAMP

Address	**Name**	**Content**							
027H	PT2MR	BPE2,	BPE1			OPC1	OPC0	BPS	PMPS
02AH	NETB	SVRH	SVRL		ENOP	SONE	SFTA	SFT1	SFT0

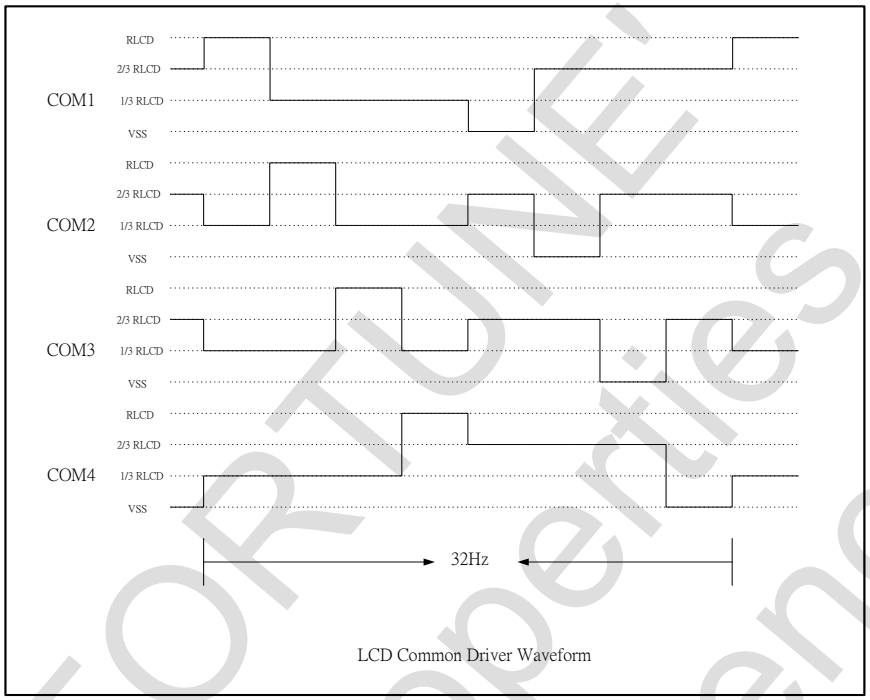
- ENOP is the OPAMP enable control signal
- SONE=1, the output and negative input of OPAMP is short and OPAMP is unit gain buffer.
- OPC can set OP1 input operation mode as follows, 00: +Offset, 01: -Offset, 10: 2KHz chopper frequency, 11: 1KHz Chopper frequency.

11.10 LCD Driver

030H	LCD1	SEG1 [3:0], SEG2 [3:0]
031H	LCD2	SEG3 [3:0], SEG4 [3:0]
032H	LCD3	SEG5 [3:0], SEG6 [3:0]
033H	LCD4	SEG7 [3:0], SEG8 [3:0]

034H	LCD5	SEG9 [3:0], SEG10 [3:0]							
035H	LCD6	SEG11 [3:0], SEG12 [3:0]							
036H	LCD7	SEG13 [3:0], SEG14 [3:0]							
037H	LCD8	SEG15 [3:0], SEG16 [3:0]							
038H	LCDEN								LCDEN

- LCD Common Driver Waveform

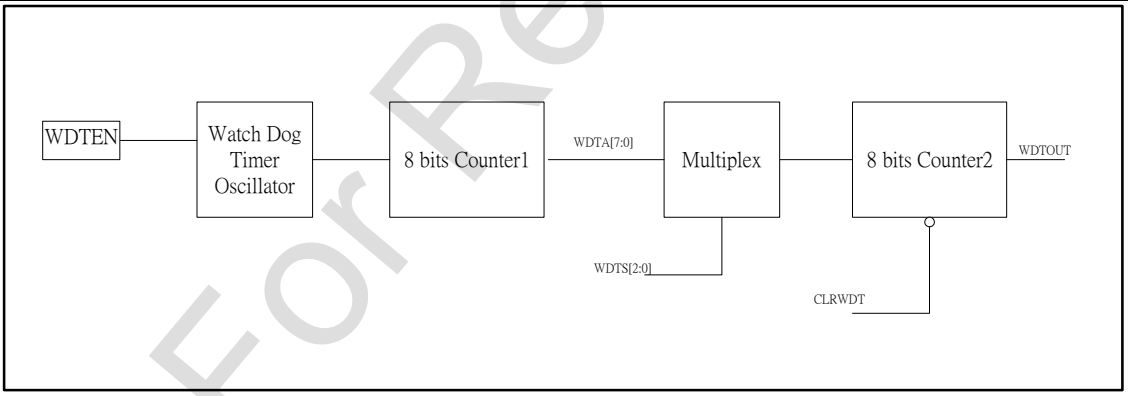


LCD Common Driver Waveform

- LCDEN =1 will start the LCD clock.
- LCD1~LCD8 is the LCD display data area.

11.11 Watch Dog Timer

Address	Name	Content							
04H	STATUS				PD	TO		C	Z
00DH	TMCON	TRST,	WTS2	WTS1	WTS0	TMEN	INS2	INS1	INS0



- WDTEN is an external input pin. It can be connected to VDD and then starts watchdog timer oscillator. If it is floated or connected to VSS, the watchdog timer function will be disabled.
- When WDT Counter 2 overflows, it will send WDTOUT to reset the CPU and set TO flag.

- CLRWDT instruction will reset WDT Counter 2
- WTS [2:0] selects WDT Counter 2 and the code selections are as follows, 000: WDTA [0], 001: WDTA [1], 010: WDTA [2], 011: WDTA [3], 100: WDTA [4], 101: WDTA [5], 110: WDTA [6], 111: WDTA [7].

11.12 Special Register External Reset (Power On Reset) and WDT Reset State

Register Name	FSR0	FSR1	STATUS	WORK	INTF	INTE
Address	02h	03h	04h	05h	06h	07h
External reset	uuuuuuuu	uuuuuuuu	00000000	uuuuuuuu	00000000	00000000
WDT reset	uuuuuuuu	uuuuuuuu	uuuu1uuu	uuuuuuuu	00000000	00000000
Register Name	PT1	PT1EN	PT1PU	PT1MR	PT2	PT2EN
Address	20h	21h	22h	23h	24h	25h
External reset	00000000	00000000	00000000	00000000	00000000	00000000
WDT reset	uuuuuuuu	uuuuuuuu	uuuu1uuu	uuuuuuuu	uuuuuuuu	uuuuuuuu
Register Name	PT2PU	PT2MR	TMOUT	TMCON	NETA	NETB
Address	26h	27h	0Ch	0Dh	29h	2Ah
External reset	00000000	00000000	00000000	10000000	00000000	00000000
WDT reset	uuuuuuuu	uuuuuuuu	00000000	10000000	00000000	00000000
Register Name	NETC	NETD	SVD	ADOH	ADOL	ADCON
Address	2Bh	2Ch	2Dh	10h	11h	13h
External reset	00000000	00000000	00000000	00000000	00000000	00000000
WDT reset	00000000	00000000	00000000	00000000	00000000	00000000
Register Name	CTAH	CTAM	CTAL	CTBH	CTBM	CTBL
Address	014h	015h	016h	017h	018h	019h
External reset	00000000	00000000	00000000	00000000	00000000	00000000
WDT reset	00000000	00000000	00000000	00000000	00000000	00000000
Register Name	FQCON	LCD1	LCD2	LCD3	LCD4	LCD5
Address	1Ah	30h	31h	32h	33h	34h
External reset	00000000	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu
WDT reset	00000000	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu
Register Name	LCD6	LCD7	LCD8	LCDEN		
Address	35h	36h	37h	38h		
External reset	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu		
WDT reset	uuuuuuuu	uuuuuuuu	uuuuuuuu	uuuuuuuu		

- u mean unknown or unchanged

11.13 Application Notes

A HALT and SLEEP Commands

Please make sure all interrupt flags are cleared before running SLEEP; ”NOP” command must follow HALT and SLEEP commands.

```
Example:
MAIN:
   HALT
   NOP
   GOTO MAIN
MAIN_SLEEP:
   CLRF  INTF
   SLEEP
   NOP
   GOTO SYSINI
```

B VDDA Regulator

VDDA Regulator uses Bias Circuit as its bias current, while Bias Circuit uses VDDA power. According to the test so far, when VDD<2.7V, it is easy to got the Start up problem and cause VDDA unable to start up. We strongly recommend our customer doing the following setup when start VDDA Regulator. This setup can make VDDA have one Diode Connection to VDD and start up VDDA Regulator

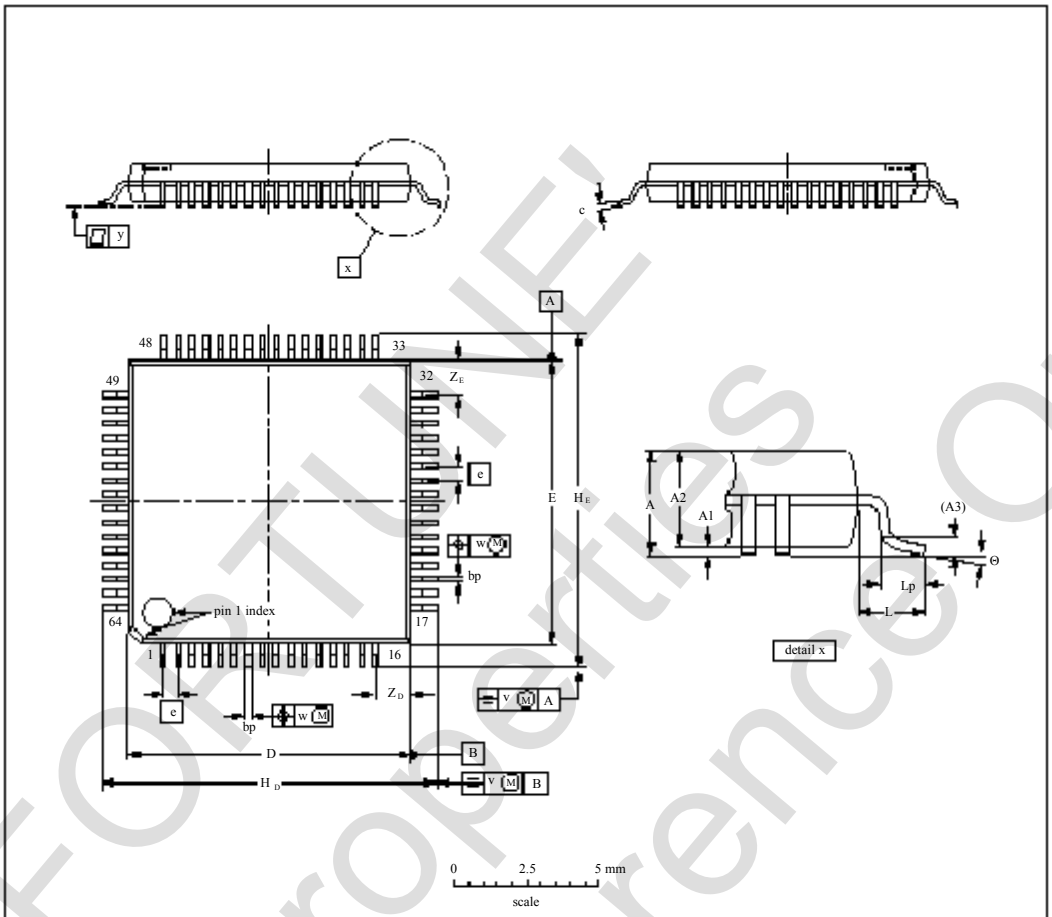
Example:

```
        MOVLW   10001111B
        MOVWF   NETD
        MOVLW   00100000B
        MOVWF   NETA
        MOVLW   00000101B
        MOVWF   NETB
    CALL    DELAY10ms
```

Customer must know how to use FS9912_ICE to test the operating current of the chip, and test actually the operating current of the chip and sleep current for corresponding custom specification. Reference Document: ”FS9912_ICEUserManual_VXX”.

12. Package Outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x1.4 mm

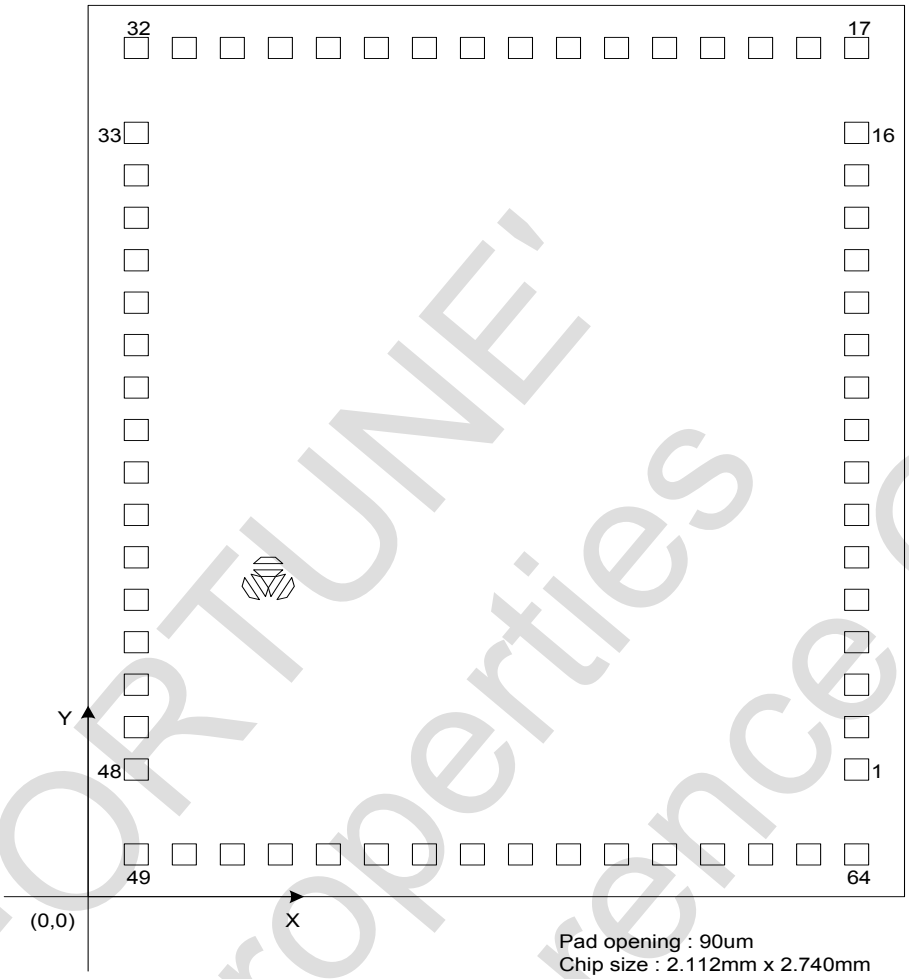


DIMENSIONS (mm are the origlinal dimensions)

UNIT	A max.	A1	A2	A3	bp	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	Lp	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	Θ
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.075	1.45 1.05	1.45 1.05	7 ° 0 °

Note: 1.Plastic or metal protrusions of 0.25 mm maximum per side are not included.

13. Pad Assignment



Substrate should be connected to VSS

14. Pad Coordinate

Pad No.	Name	X [mm]	Y [mm]	Pad No.	Name	X [mm]	Y [mm]
1	P1.0	2.035	0.385	33	SEG6	0.077	2.320
2	P1.1	2.035	0.525	34	SEG7	0.077	2.180
3	P1.2	2.035	0.665	35	SEG8	0.077	2.040
4	P1.3	2.035	0.790	36	SEG9	0.077	1.915
5	P1.4	2.035	0.915	37	SEG10	0.077	1.790
6	P1.5	2.035	1.040	38	SEG11	0.077	1.665
7	P1.6	2.035	1.165	39	SEG12	0.077	1.540
8	P1.7	2.035	1.290	40	SEG13	0.077	1.415
9	P2.0	2.035	1.415	41	SEG14	0.077	1.290
10	P2.1	2.035	1.540	42	SEG15	0.077	1.165
11	P2.2	2.035	1.665	43	SEG16	0.077	1.040
12	P2.3	2.035	1.790	44	COM4	0.077	0.915
13	P2.4	2.035	1.915	45	COM3	0.077	0.790
14	P2.5	2.035	2.040	46	COM2	0.077	0.665
15	P2.6	2.035	2.180	47	COM1	0.077	0.525
16	P2.7	2.035	2.320	48	VSS	0.077	0.385
17	XIN	2.035	2.663	49	OP1N	0.077	0.077
18	XOUT	1.885	2.663	50	OP1O	0.225	0.077
19	WDTEN	1.745	2.663	51	REFO	0.365	0.077
20	TST	1.620	2.663	52	REFI	0.490	0.077
21	RST	1.495	2.663	53	FT2	0.615	0.077
22	VDD	1.370	2.663	54	FT1	0.740	0.077
23	CB	1.245	2.663	55	AD7	0.865	0.077
24	CA	1.120	2.663	56	AD6	0.990	0.077
25	VGG	0.995	2.663	57	AD5	1.115	0.077
26	VDDA	0.870	2.663	58	AD4	1.240	0.077
27	RLCD	0.745	2.663	59	AD3	1.365	0.077
28	SEG1	0.620	2.663	60	AD2	1.490	0.077
29	SEG2	0.495	2.663	61	AD1	1.615	0.077
30	SEG3	0.370	2.663	62	AD0	1.740	0.077
31	SEG4	0.230	2.663	63	VB	1.880	0.077
32	SEG5	0.082	2.663	64	AGND	2.035	0.077

15. Revision History

Ver.	Date	Page	Description
2.9	2003/04/16	27	MOVLW 00100000B MOVWF NETA
3.0	2003/08/29	2	Operation current is less than 2mA, sleep mode current is about 1uA (LVR disable)
		2	Low voltage reset (LVR) function mask option. FS9912R-nnnV LVR enable, FS9912-nnnV LVR disable.
		8	IPO1: Sleep current of FS9912-nnnV IPO2: Sleep current of FS9912R-nnnV
		12	Change circuit drawing from draft to Visio format
3.1	2004/04/05	All	Reformat and correct the contents
3.2	2004/06/23	4	2. Features Correct “Low noise (1mV peak-to-peak without chopper, 0.5mV peak-to-peak with chopper, 0.1Hz~1Hz) OPAMP with chopper controller.” To “Low noise (1μV peak-to-peak without chopper, 0.5μV peak-to-peak with chopper, 0.1Hz~1Hz) OPAMP with chopper controller.”.
3.3	2004/07/26	4	2. Features Correct “Operation current is less than 2mA, sleep mode current is about 1mA (LVR disable).” to “Operation current is less than 2mA, sleep mode current is about 1μA (LVR disable).”.
3.4	2004/10/18	-	1. FSC will switch FS9912R version A to version B from 2004/10/18. The reason is that FSC did some improvement about the ESD immunity and LVR circuit of the FS9912. The FSC’s FS9912R version B test review meeting minutes was accepted by DCC on 2004/9/3. 2. Change the right-top title word of each page: “-Bit” to “–bit”. 3. Change the left-bottom word of each page: “Co” to “Corp”.
3.5	2005/12/02	12	1. Add “Typical Performance Characteristics”.
		35	1. Add “Revision History”.
3.6	2014/05/22	2	Revised company address