

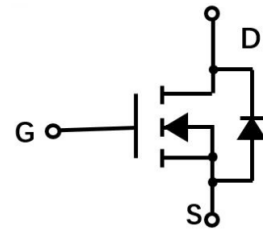
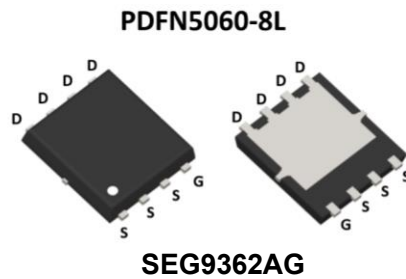
Features

- 100V, 40A
- $R_{DS(ON)} = 16m\Omega$ (Max.) @ $V_{GS} = 10V, I_D = 20A$
- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- 100% UIS tested , 100% ΔV_{DS} Tested
- RoHS and Halogen-Free Compliant

Application

- High Frequency Switching
- Synchronous Rectification

Package



Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current ^{note5}	$T_C = 25^\circ C$	40	A
I_D	Continuous Drain Current ^{note5}	$T_C = 100^\circ C$	27	A
I_{DM}	Pulsed Drain Current ^{note3}		160	A
P_D	Power Dissipation ^{note2}	$T_C = 25^\circ C$	50	W
I_{AS}	Avalanche Current ^{note3,6}		6	A
E_{AS}	Single Pulse Avalanche Energy ^{note3,6}		32	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2.1	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ^{note1,4}		55	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$

Electrical Characteristics $T_C=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.8	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 20A$	-	14.3	16	m Ω
		$V_{GS} = 4.5V, I_D = 10A$	-	18.8	22.5	m Ω
R_g	Gate Resistance	$V_{DS} = V_{GS}=0V, f = 1.0MHz$	-	1.44	-	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	-	1130	-	pF
C_{oss}	Output Capacitance		-	496	-	pF
C_{rss}	Reverse Transfer Capacitance		-	60	-	pF
Switching Characteristics						
Q_g	Total Gate Charge	$V_{DS} = 50V, I_D = 40A,$ $V_{GS} = 10V$	-	30	-	nC
Q_{gs}	Gate-Source Charge		-	6	-	
Q_{gd}	Gate-Drain("Miller") Charge		-	8.2	-	
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 50V, I_D = 40A,$ $R_G = 3.3\Omega, V_{GS}=10V$	-	46	-	ns
t_r	Turn-On Rise Time		-	55	-	
$t_{d(off)}$	Turn-Off Delay Time		-	249	-	
t_f	Turn-Off Fall Time		-	105	-	
Diode Characteristics						
I_S	Continuous Source Current		-	-	40	A
V_{SD}	Diode Forward Voltage	$I_S=20A, V_{GS} = 0V$	-	0.88	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD}=20A,$	-	36.5	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_{SD}/dt=100A/\mu s$	-	36	-	nC

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with $T_A = 25^{\circ}C$ and the maximum allowed junction temperature of $150^{\circ}C$. The value in any given application depends on the user's specific board design.
2. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}C$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
3. Single pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}C$.
4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
5. The maximum current rating is package limited.
6. The EAS data shows Max. rating. The test condition is $V_{DS}=50V, V_{GS}=10V, L=0.5mH$

Typical Performance Characteristics

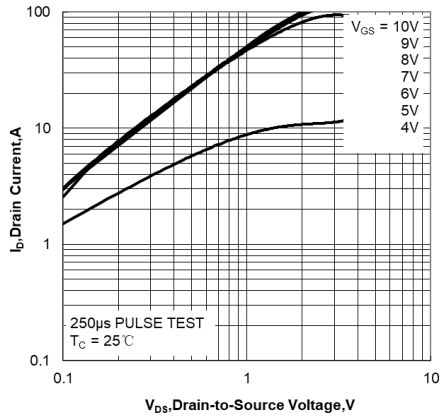


Figure 1. Output Characteristics

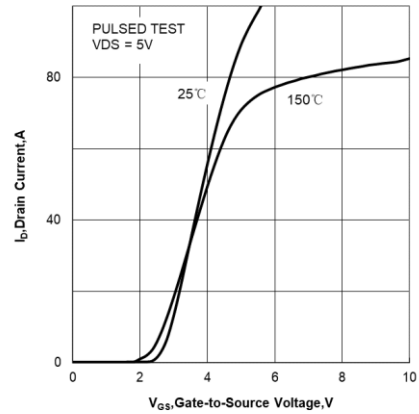


Figure 2. Transfer Characteristics

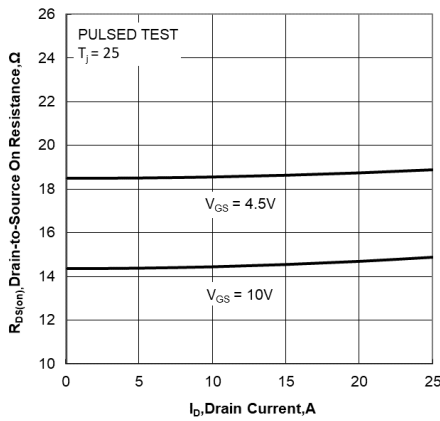


Figure 3. Drain-to-Source On Resistance vs Drain Current

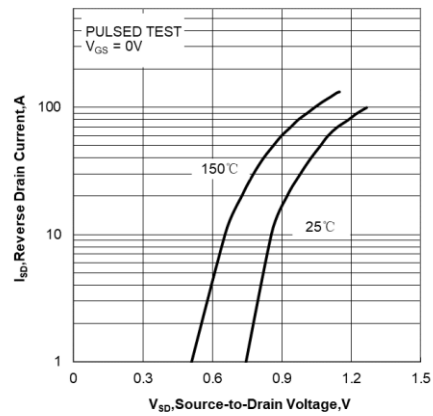


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

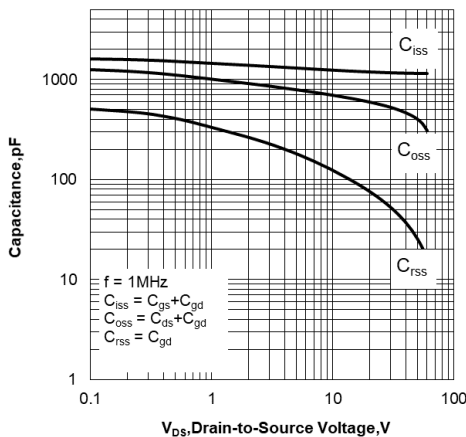


Figure 5. Capacitance Characteristics

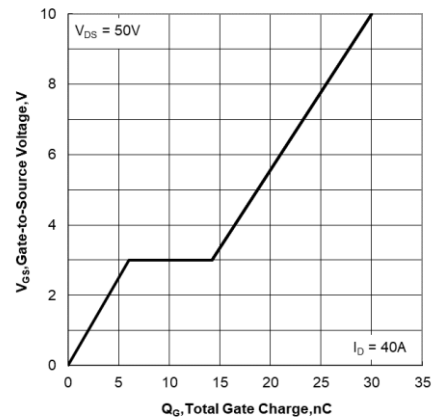


Figure 6. Gate Charge Characteristics

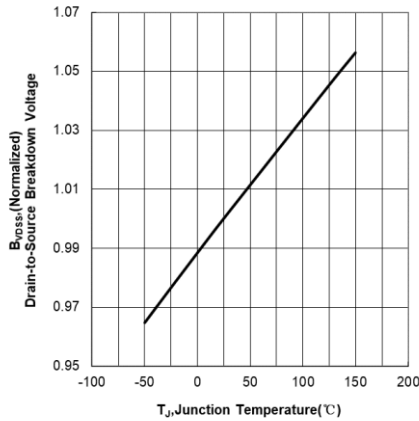


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

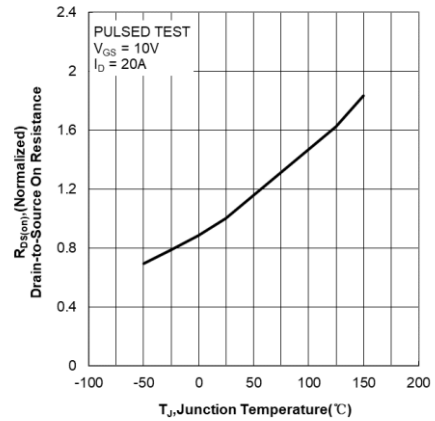


Figure 8. Normalized On Resistance vs Junction Temperature

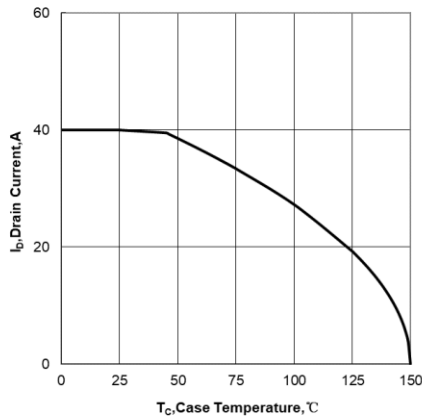


Figure 9. Maximum Continuous Drain Current vs Case Temperature

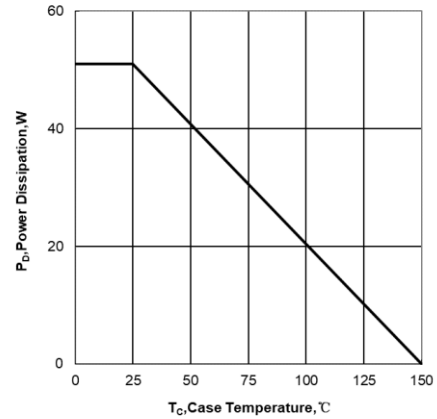


Figure 10. Maximum Power Dissipation vs Case Temperature

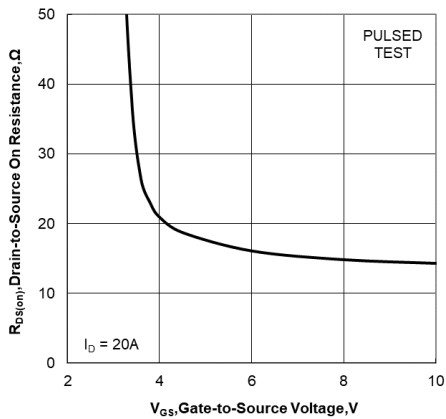


Figure 11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

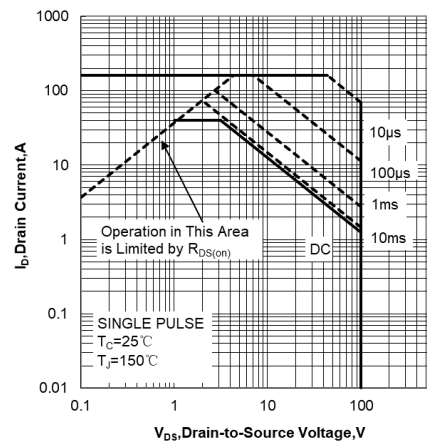


Figure 12. Maximum Safe Operating Area

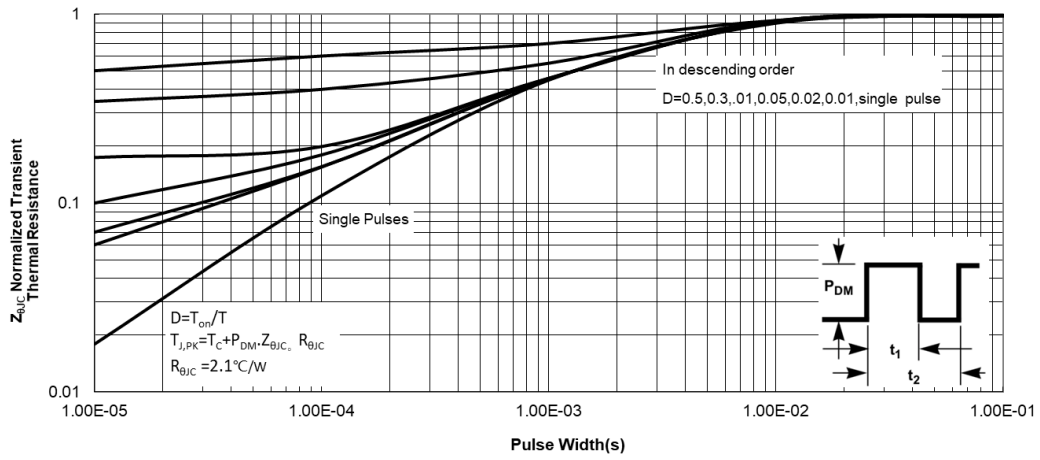
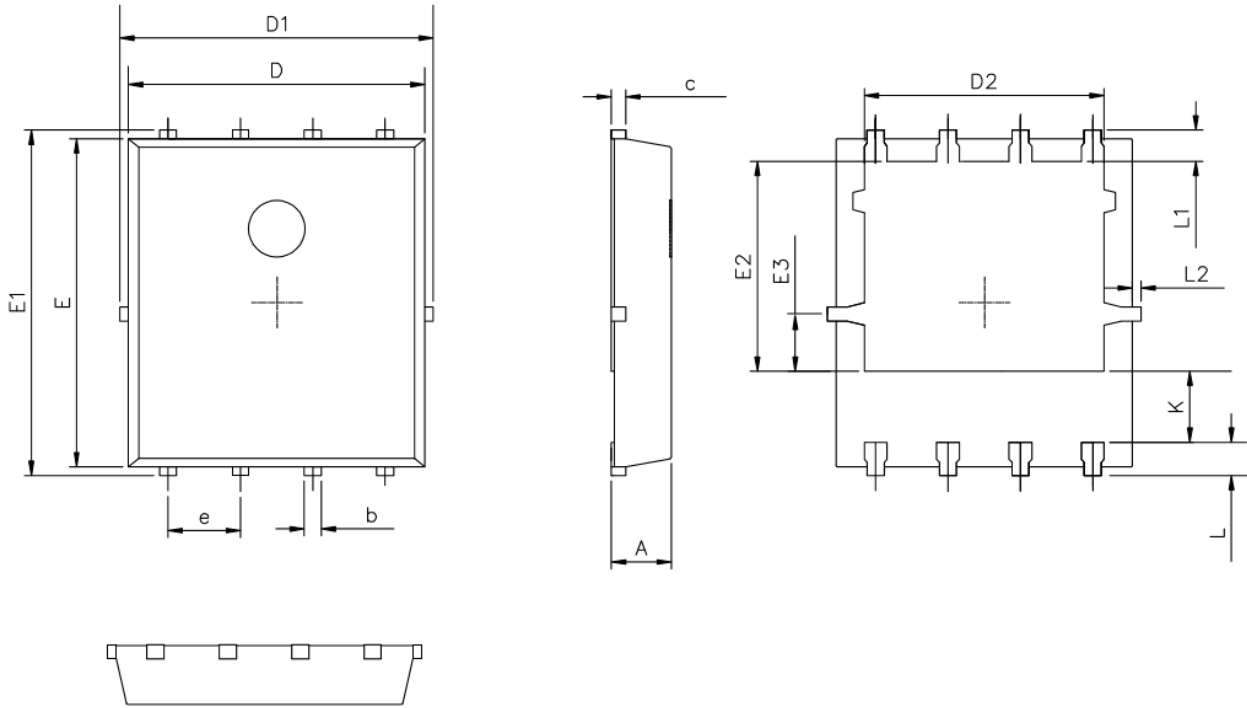
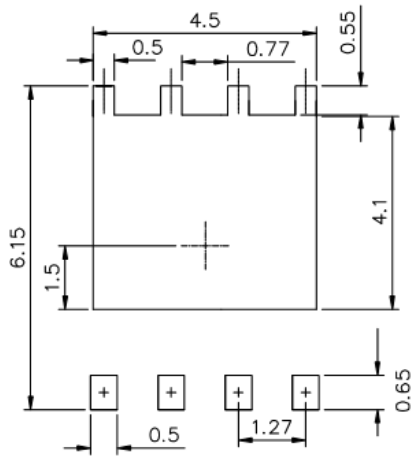


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

PDFN5060-8L Package Mechanical Data



RECOMMENDED LAND PATTERN



UNIT:mm

	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.25	0.35	0.50
c	0.10	0.20	0.30
D	4.80	5.00	5.30
D1	4.90	5.10	5.50
D2	3.92	4.02	4.20
E	5.65	5.75	5.85
E1	5.90	6.05	6.20
E2	3.325	3.525	3.775
E3	0.80	0.90	1.00
e		1.27	
L	0.40	0.55	0.70
L1		0.65	
L2	0.00		0.15
K	1.00	1.30	1.50

SEG9362AG Product Description

Silicon N-Channel MOSFET



NOTE:

1. We strongly recommend customers check carefully on the trademark when buying our product, if there is any question, please don't be hesitate to contact us.
2. Please do not exceed the absolute maximum ratings of the device when circuit designing.
3. Winsemi Microelectronics Co., Ltd reserved the right to make changes in this specification sheet and is subject to change without prior notice.

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