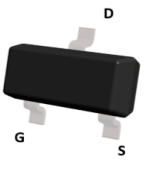
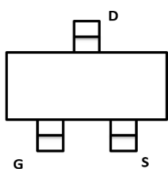
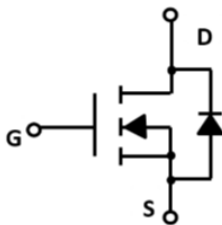


<p>Features</p> <ul style="list-style-type: none"> • 100V, 3A • $R_{DS(ON)} = 140m\Omega$ (Max.) @ $V_{GS} = 10V, I_D = 3A$ • High Power and Current Handling Capability • Lead Free Product is Acquired • Surface Mount Package 	<p>Application</p> <ul style="list-style-type: none"> • PWM Application • Load Switch • Power Management
<p>Package</p> <div style="display: flex; justify-content: space-around; align-items: center;">    </div> <p style="text-align: center;">SOT-23-3L SFZ3N10AT</p>	

Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise specified

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	3	A
I_{DM}	Pulsed Drain Current ^{note1}	12	A
P_D	Maximum Power Dissipation	17	W
E_{AS}	Single pulsed avalanche energy ^{note5}	1.2	mJ
R_{thC}	Thermal Resistance, From Junction To Case	7.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ^{note2}	62.5	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$

*Drain current limited by maximum junction temperature

Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	110	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
On Characteristics ^{note3}						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.95	3.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance ^{note2}	$V_{GS} = 10V, I_D = 3A$	-	115	140	m Ω
Dynamic Characteristics ^{note4}						
C_{iss}	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1.0MHz$	-	206	-	pF
C_{oss}	Output Capacitance		-	28.9	-	pF
C_{rss}	Reverse Transfer Capacitance		-	1.4	-	pF
Q_g	Total Gate Charge	$V_{DS} = 50V, I_D = 3A,$ $V_{GS} = 10V$	-	4.3	-	nC
Q_{gs}	Gate-Source Charge		-	1.5	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	1.1	-	nC
Switching Characteristics ^{note4}						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50V, I_{DS}=3A$ $R_G = 2\Omega, V_{GEN} = 10V$	-	14.7	-	ns
t_r	Turn-On Rise Time		-	3.5	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	20.9	-	ns
t_f	Turn-Off Fall Time		-	2.7	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current ^{note2}		-	-	3	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	12	A
V_{SD}	Drain to Source Diode Forward Voltage ^{note3}	$V_{GS} = 0V, I_S = 3A$	-	-	1.3	V
t_{rr}	Body Diode Reverse Recovery Time	$V_{GS} = 0V, I_F = 3A,$ $di/dt = 100A/\mu s$	-	32.1	-	ns
Q_{rr}	Body Diode Reverse Recovery Time Charge		-	39.4	-	nC
I_{rrm}	Peak Reverse Recovery Current		-	2.1	-	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. $V_{DD}=50$ V, $R_G=50$ Ω , $L=0.3$ mH, starting $T_j=25$ $^{\circ}\text{C}$

Typical Performance Characteristics

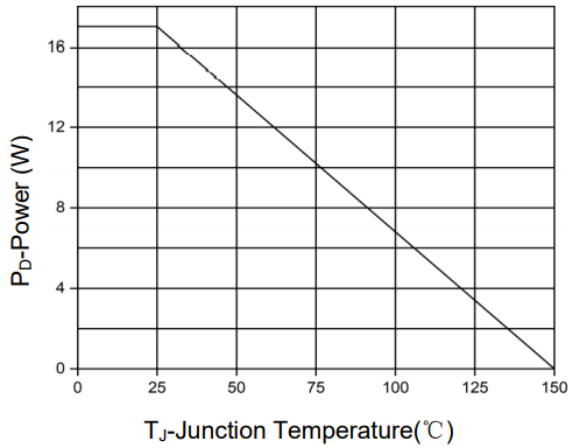


Figure 1. Power Dissipation

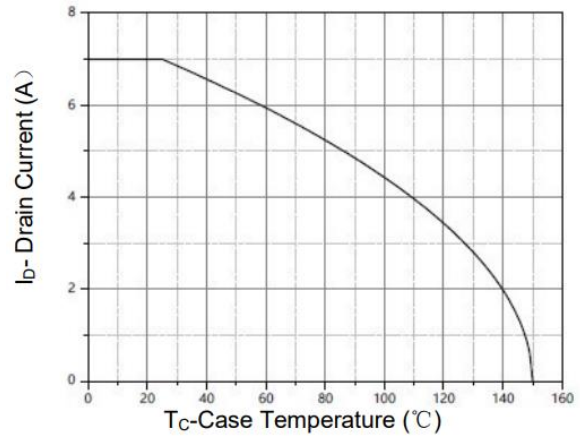


Figure 2. Drain Current

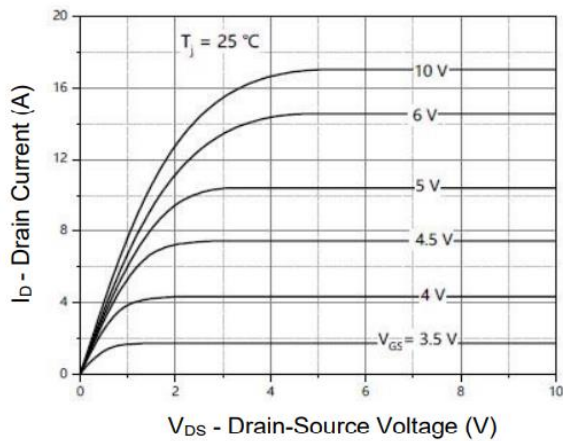


Figure 3. Output characteristics

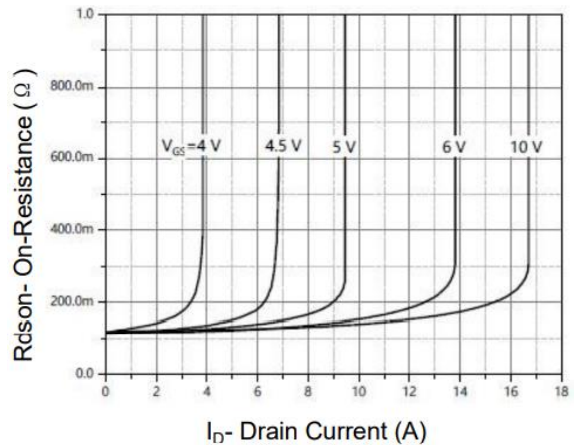


Figure 4. Drain-Source On-state resistance

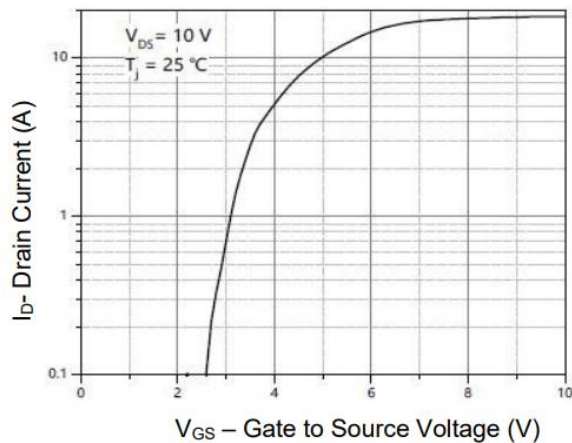


Figure 5. Transfer Characteristics

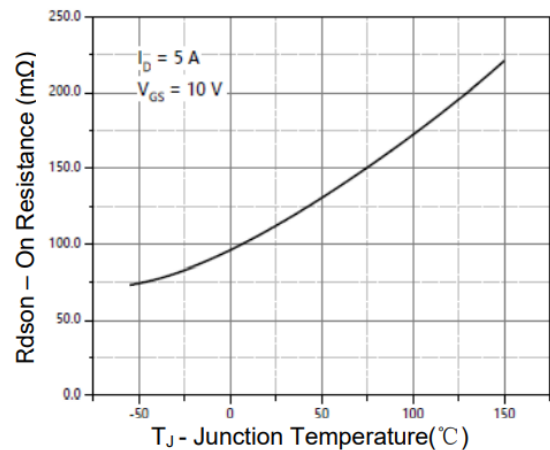


Figure 6. Drain-Source On-State Resistance

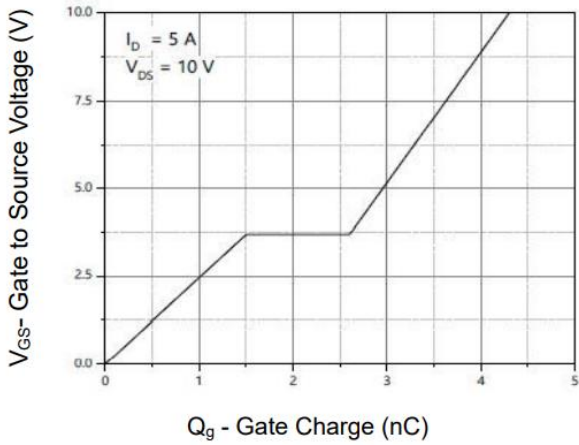


Figure 7. Gate Charge

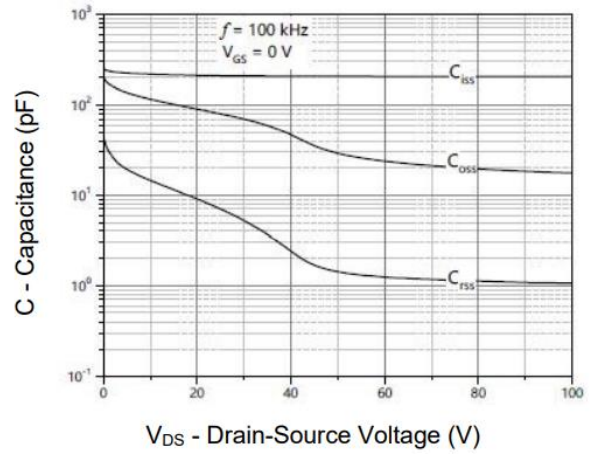


Figure 8. Capacitance vs Vds

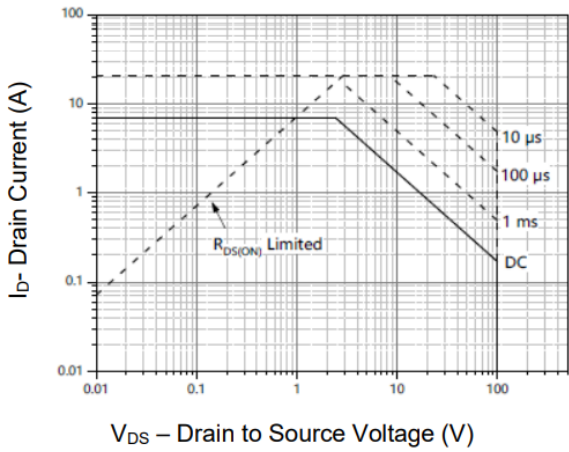


Figure 9. Safe Operation Area

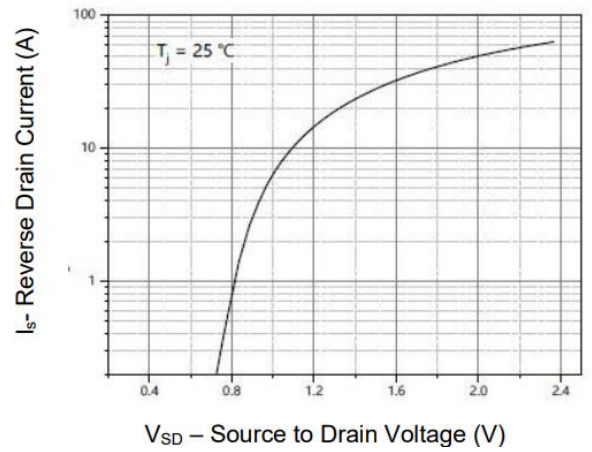


Figure 10. Source- Drain Diode Forward

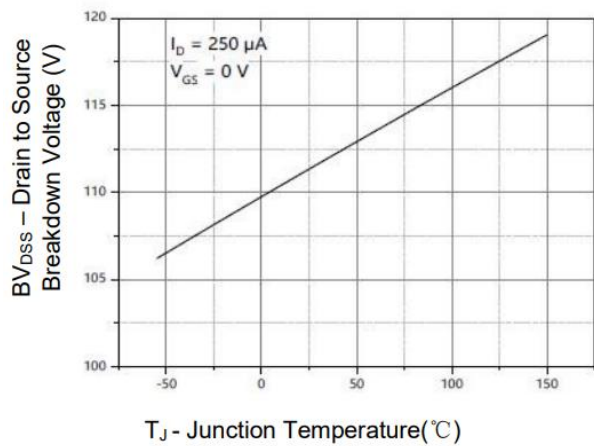


Figure 11. Drain-source breakdown voltage

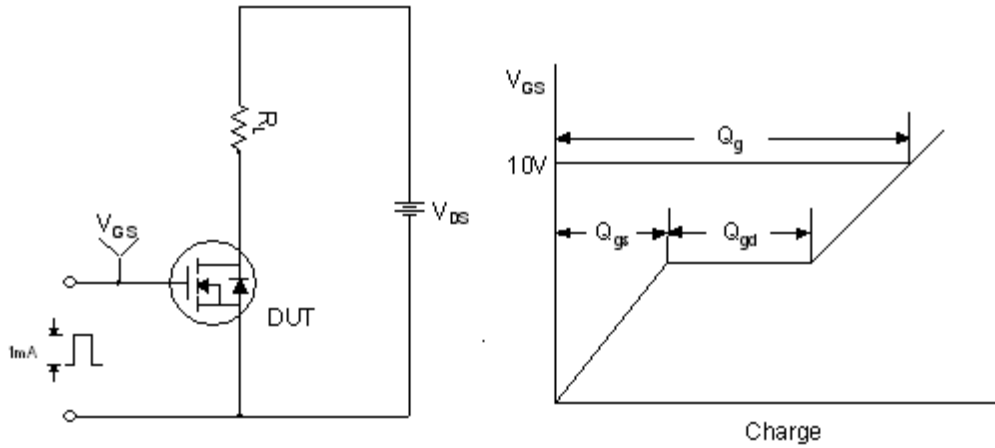


Figure 12. Gate Charge Test Circuit & Waveform

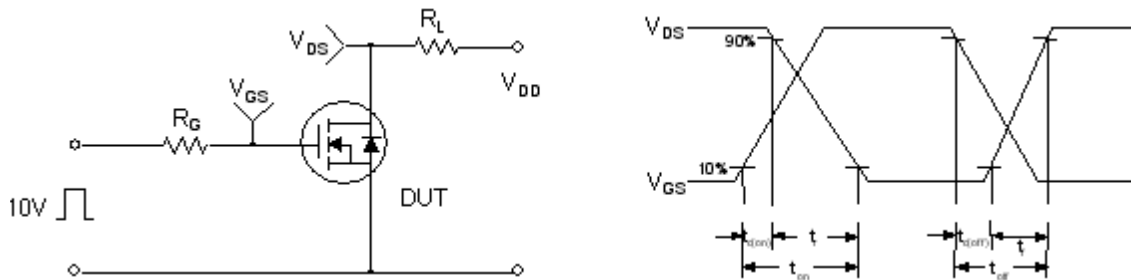


Figure 13. Resistive Switching Test Circuit & Waveforms

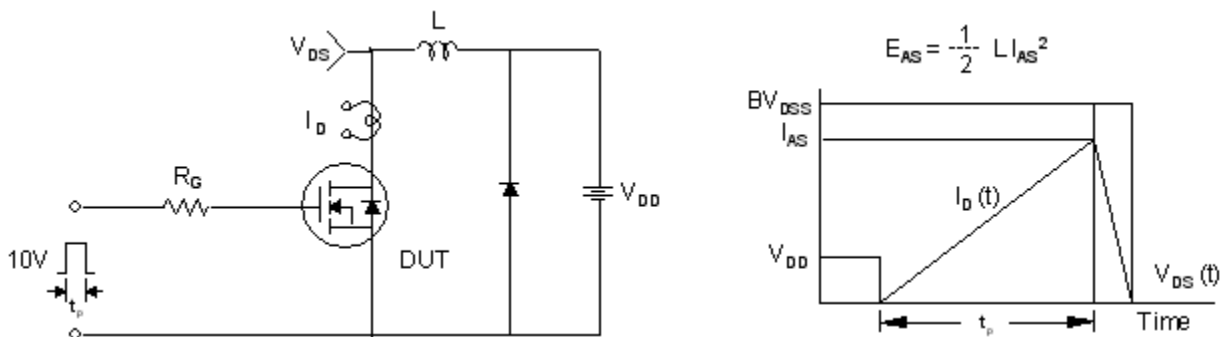


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

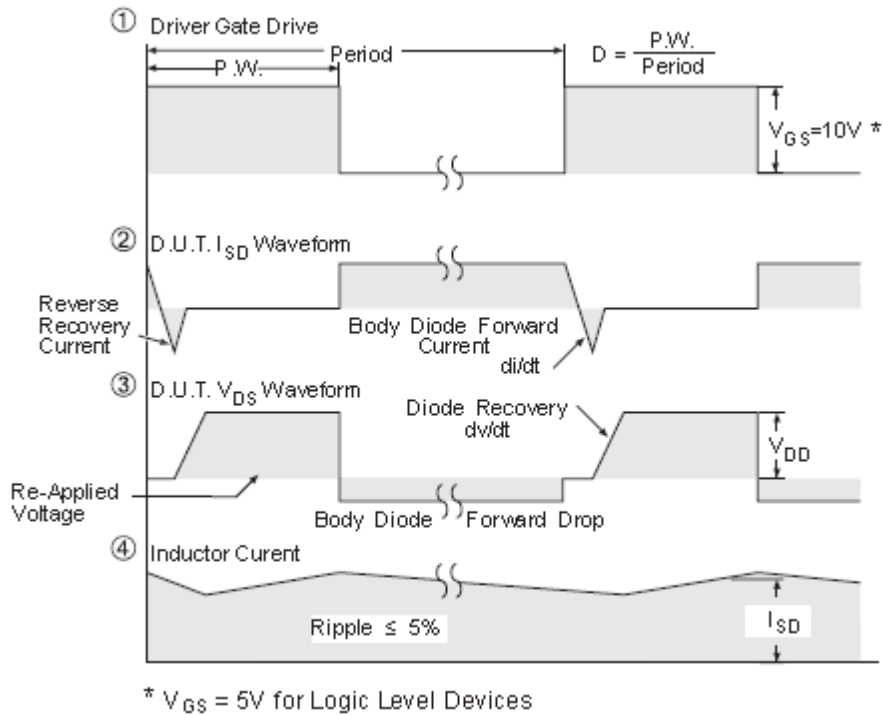
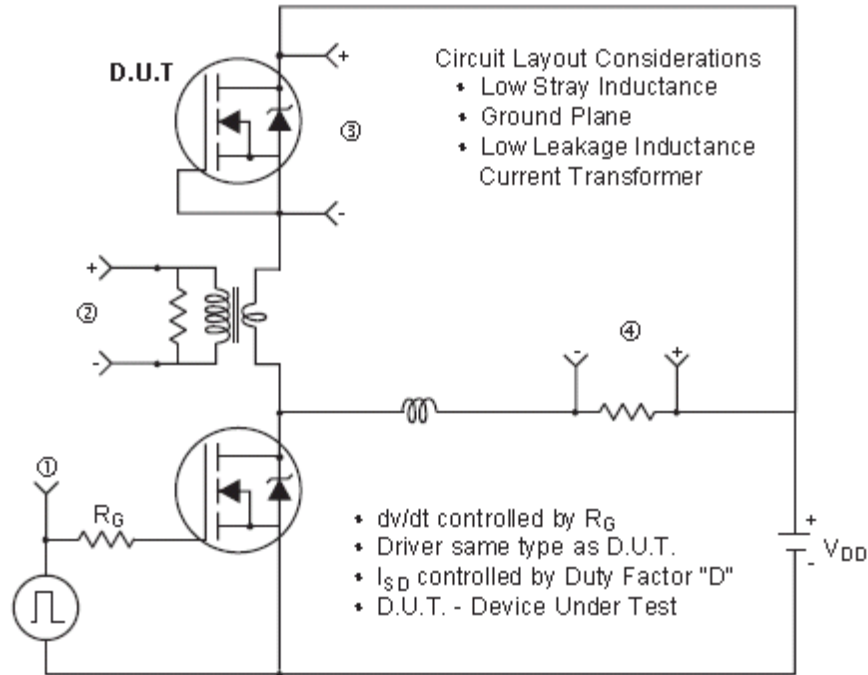
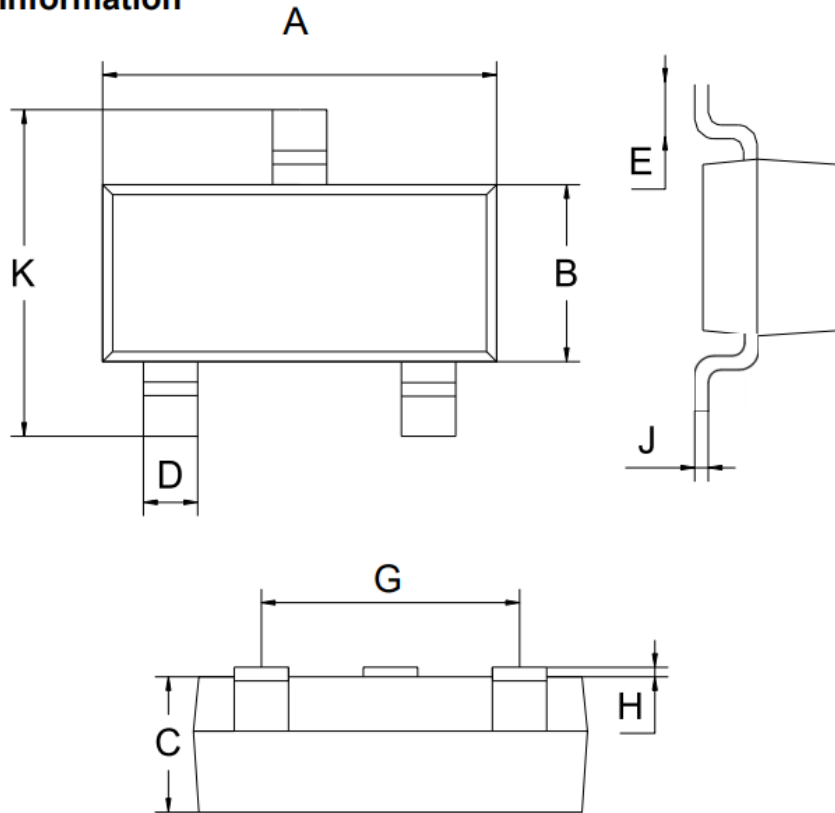


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

SOT-23-3L Package Information



SOT-23-3L			
Dim	MIN	NOM	MAX
A	2.80	2.90	3.00
B	1.50	1.60	1.70
C	1.00	1.10	1.20
D	0.30	0.40	0.50
E	0.25	0.40	0.55
G	1.90		
H	0.00	-	0.10
J	0.047	0.127	0.207
K	2.60	2.80	3.00
All Dimensions in mm			

SFZ3N10AT Product Description

Silicon N-Channel MOSFET



NOTE:

1. We strongly recommend customers check carefully on the trademark when buying our product, if there is any question, please don't be hesitate to contact us.
2. Please do not exceed the absolute maximum ratings of the device when circuit designing.
3. Winsemi Microelectronics Co., Ltd reserved the right to make changes in this specification sheet and is subject to change without prior notice.

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