

## 8 keys Touch Pad Detector IC

### Outline

- The TTP239-COBN TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 8 touch pads with two kinds of serial output interface.

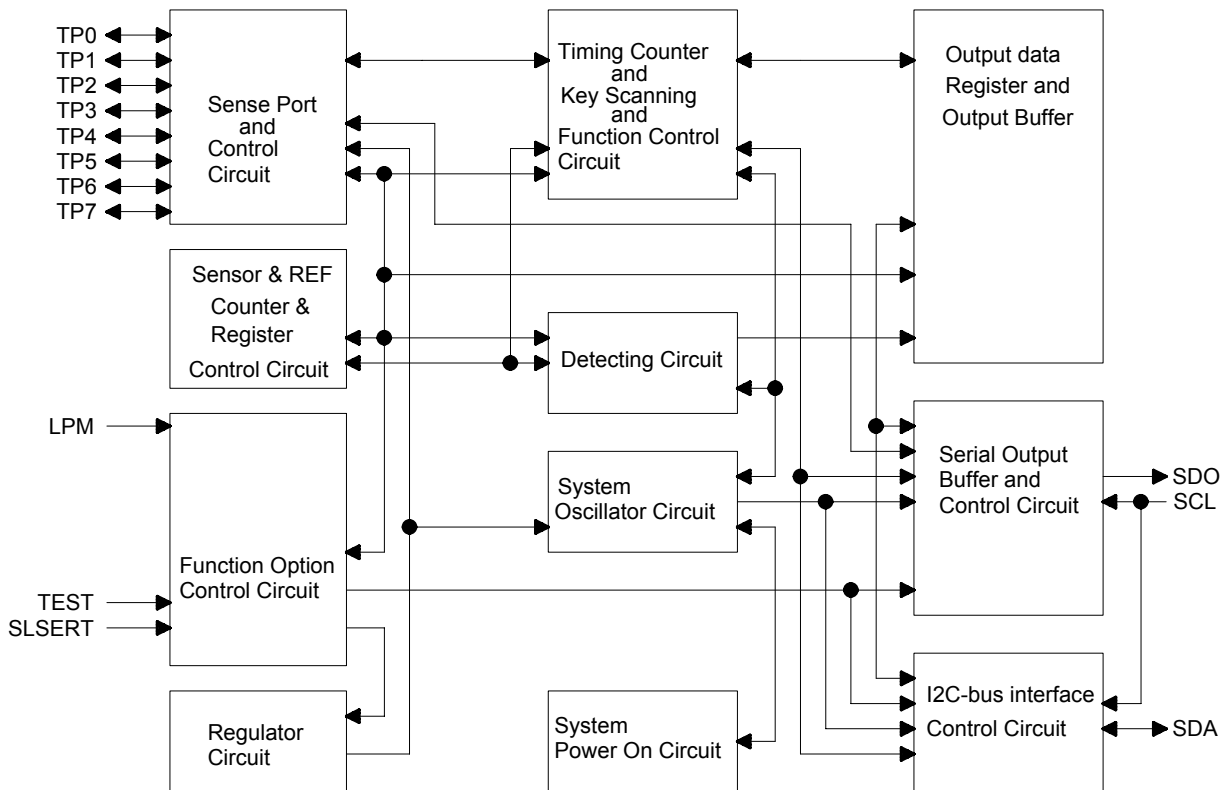
### Characteristic

- Operating voltage 2.4V ~ 5.5V
- Built-in regulator for touch sensor
- Built-in low voltage reset(LVR) function
- Operating current, @VDD=3V no load  
At low power mode typical 5.0uA, At fast mode typical 30uA
- @VDD=3V operating voltage :  
The response time about 160mS at low power mode, 60mS at fast mode
- Sensitivity can adjust by the capacitance ( 1~50pF ) outside for each touch pad
- Provides Fast mode and Low Power mode selection by pad option (LPM pin)
- Provides two kinds of serial output interface  
Include 2-wires and I<sup>2</sup>C-bus slave serial interface that can be selected by pad option (SLSERT pin)
- Have the maximum on time about 16sec
- Provides Single-key functions
- 2-wires serial interface active low
- After power-on have about 0.5sec stable-time, during the time do not touch the key pad, and the function is disabled
- Auto calibration for life  
The re-calibration period is about 1 sec within 8 sec after power-on. When key has been touched within 8 sec or key has not been touched more than 8 sec after power-on, then the re-calibration period change to 4 sec

### Applications

- Wide consumer products
- Button key replacement

## Block diagram



**Pin Description**

Pin NO	Pin Name	Type	Pad Description
1	TP3	I/O	Touch pad input pin
2	TP2	I/O	Touch pad input pin
3	TP1	I/O	Touch pad input pin
4	TP0	I/O	Touch pad input pin
5	LPM	I-PH	Low power/fast mode option 1(Default)=>Low power mode; 0=>Fast mode
6	TEST	I-PL	Only for test
7	VDD	P	Positive power supply
8	SDA	I/OD	Data pin for the I <sup>2</sup> C-bus serial data interface
9	SDO	O	Data pin for the 2-wires serial output, active Low
10	SCL	I	Serial clock input pin for serial type At 2-wires serial type active Low
11	VSS	P	Negative power supply, ground
12	SLSSERT	I-PH	The option pin for serial output type selection, Default:1
13	TP7	I/O	Touch pad input pin
14	TP6	I/O	Touch pad input pin
15	TP5	I/O	Touch pad input pin
16	TP4	I/O	Touch pad input pin

**Pin Type**

- I CMOS input only
- O CMOS push-pull output
- I/O CMOS I/O
- P Power/Ground
- I-PH CMOS input and pull-high resistor
- I-PL CMOS input and pull-low resistor
- OD Open drain output

## Electrical Characteristics

- Absolute maximum ratings**

Parameter	Symbol	Conditions	Rating	Unit
Operating Temperature	T <sub>OP</sub>	—	-40~+85	°C
Storage Temperature	T <sub>STG</sub>	—	-50~+125	°C
Supply Voltage	VDD	Ta=25°C	VSS-0.3~VSS+5.5	V
Input Voltage	V <sub>IN</sub>	Ta=25°C	VSS-0.3~VDD+0.3	V
Human Body Mode	ESD	—	5	KV

Note : VSS symbolizes for system ground

- DC / AC characteristics : ( Test condition at room temperature = 25 °C )**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	Internal regulator enable	2.4		5.5	V
Internal Regulator			2.2	2.3	2.4	V
Operating Current	I <sub>OPL</sub>	VDD=3V, At low power mode		5.0		uA
	I <sub>OFF</sub>	VDD=3V, At fast mode		30.0		uA
Input Ports	V <sub>IL</sub>	Input Low Voltage	0		0.2	VDD
Input Ports	V <sub>IH</sub>	Input High Voltage	0.8		1.0	VDD
Output Port Sink Current	I <sub>OL</sub>	VDD=3V, V <sub>OL</sub> =0.6V		8		mA
Output Port Source Current	I <sub>OH</sub>	VDD=3V, V <sub>OH</sub> =2.4V		-4		mA
Input Pin Pull-high Resistor	R <sub>PH</sub>	VDD=3V		30K		ohm
Input Pin Pull-low Resistor	R <sub>PL</sub>	VDD=3V		30K		ohm
Output Response Time	T <sub>R</sub>	VDD=3V、 At fast mode		60		mS
		VDD=3V、 At low power mode		160		

## Function Description

### I . Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP239-COBN offers some methods for adjusting the sensitivity outside

1. by the electrode size

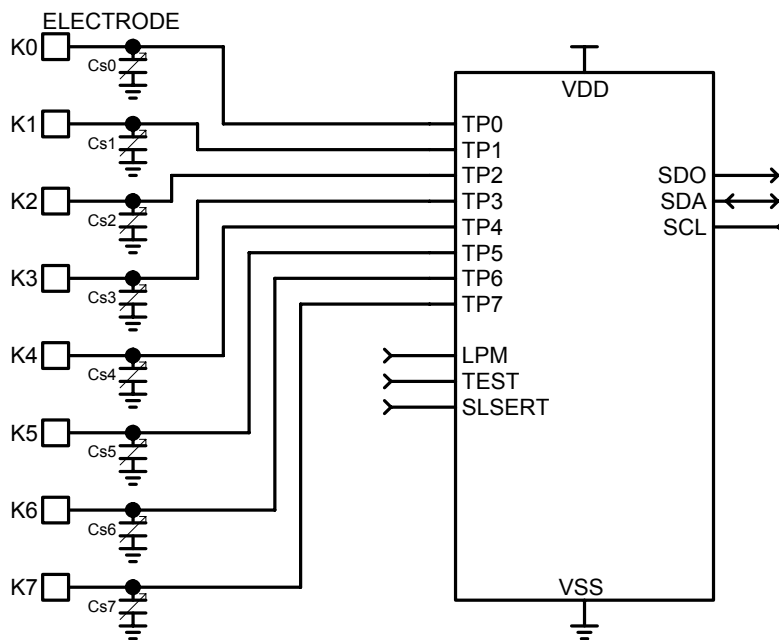
Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope

2. by the panel thickness

Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value

3. by the value of Cs0~Cs7 ( please see the below figure )

Under other conditions are fixed. Add the capacitors Cs0~Cs7 can fine tune the sensitivity for single key, that lets all key's sensitivity identical. When do not use any capacitor to VSS, the sensitivity is most sensitive. When adding the values of Cs0~Cs7 will reduce sensitivity in the useful range (  $1 \leq Cs0 \sim Cs7 \leq 50pF$  )



## II. Maximum key on duration time

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP239-COBN sets a timer to monitor the detection. The timer is the maximum on duration time about 16sec. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection

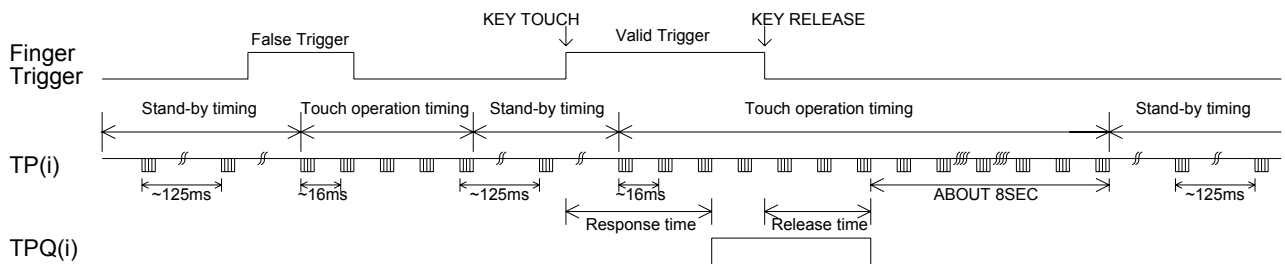
## III. Fast and Low power mode select ( By LPM pin option )

The TTP239-COBN has Fast mode and Low Power mode to be selected. It depends on the state of LPM pin. When the LPM pin is connected to VSS, the TTP239-COBN runs in Fast mode. When the LPM pin is opened or connected to VDD, the TTP239-COBN runs in Low Power mode.

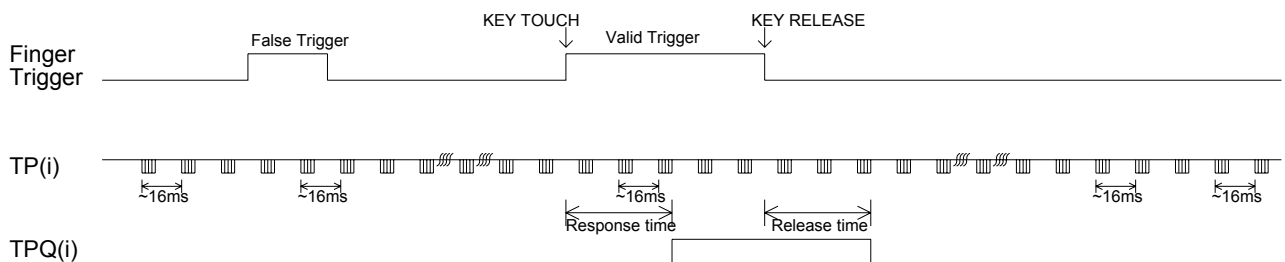
In the Fast mode response time is faster, but the current consumption will be increased. In the Low Power mode it will be saving power, but will be slowing response time for first touch. When it awaked in fast mode, the response time is the same the fast mode. In this mode when detecting key touch, it will switch to Fast mode. Until the key touch is released and will keep a time about 8sec. Then it returns to Low Power mode.

The states and timing of two modes please see below figure.

### Low Power Mode timing diagram:



### Fast Mode timing diagram:



LPM	Option features	Remark
1	Low Power mode	Default
0	Fast mode	

## IV. Serial output interface

SLSERT	Option features	Remark
1	2-wires serial type	Default
0	I <sup>2</sup> C-bus serial type	

7-1 The 2-wires serial output interface mode can be selected by the SLSERT pin that it has to be floated or connected to VDD. At the mode the SDO pin is data output pin, the SCL is clock input pin, both active low.

The 2-wires serial mode supports always polling data for other device on the system. Or other device can wait that TTP239-COBN outputs the data valid (DV) signal by the SDO pin, and it can give the clock signal to TTP239-COBN SCL pin and get the keys data from SDO pin. The TTP239-COBN 2-wires serial interface supports a timeout mechanism for SCL pin. If the SCL pin has no signal edge change over 2ms, the 2-wires serial interface will reset itself and return to stand-by state.

2-wires serial interface mode timing please see below.  
The D0~D7 correspond to data of the TP0~7.

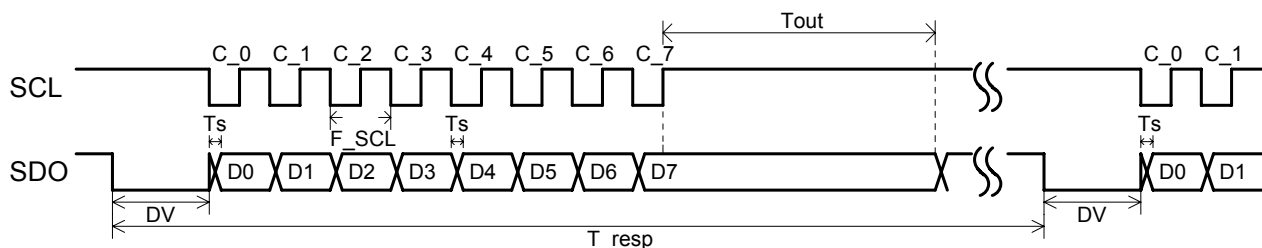


Figure 7-1-1 : The timing for active-low

The parameters for figure 7-1-1 :

Parameter	Min.	Typ.	Max.	Unit
DV(Time out)	-	2	-	ms
Ts	200	-	-	ns
Tout	-	2	-	ms
T_resp	-	16	-	ms
F_SCL	1K	-	512K	Hz

Note :

- (1) When any data of the TP0~TP7 change, the SDO pin output DV signal, the time out of DV signal is about 2msec. But other device can not wait that the DV signal time is over, after it detect the DV signal, and then can give the clock signal to the TTP239-COBN by the SCL pin at the duration of DV signal. When the TTP239-COBN detect the first clock edge changing, and the DV signal is over, and the SDO pin change to output the data of TP0~TP7.
- (2) The parameter Ts is data set-up time, it means that the data change time for SDO pin.

7-2 For I2C-bus slave interface mode selection, the SLSERT pin has to be connected to VSS. At the mode the SDA pin is a serial data pin, the SCL is a serial clock input pin. The SDA and SCL pins must be pulled-high with an external resistor. And the 4-bits identify code for the TTP239-COBN is " (1010) ". The device address is defined 101. The TTP239-COBN 8-bits slave device address includes 4-bits identifier, 3-bits option address and R/W bit (see the Table 7-2-1). The TTP239-COBN IC uses the I<sup>2</sup>C-bus slave interface data transmission protocol to output the data of the touch pads (TP0~TP7 pins), so the TTP239-COBN only accepts the read operation that R/W bit is " 1 ". If it is " 0 ", the TTP239-COBN will not respond the write operation. Otherwise, the I<sup>2</sup>C-bus slave interface of TTP239-COBN conforms to the communication protocols. It supports the fast mode that the maximum SCL clock frequency is 400KHz. The I<sup>2</sup>C-bus slave interface supports the following communication protocols:

Bus not busy : The SDA and the SCL lines remain High level when the bus is not active.

Start condition : Start condition is SDA 1 to 0 transition when SCL=1.(see figure 7-2-2)

Stop condition : Stop condition is SDA 0 to 1 transition when SCL=1.(see figure 7-2-2)

Data valid : Following a start condition, the data on the SDA line must be stable during the High period of SCL. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.(see figure 7-2-2)

ACK (Acknowledge) : An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the ninth clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data. But the slave does not send an ACK if it does not successfully received the eight bits of data. In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the ninth clock period. If an ACK is detected, the slave will continue to transmit next data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

Slave Address : The identify code for the TTP239-COBN is " (1010) ". The device address is 101.

Read/Write : The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is " 1 ", a read operation is executed. If it is " 0 ", a write operation is executed. But the TTP239-COBN only accepts read operation. The sequence of read data operation please see figure 7-2-1.

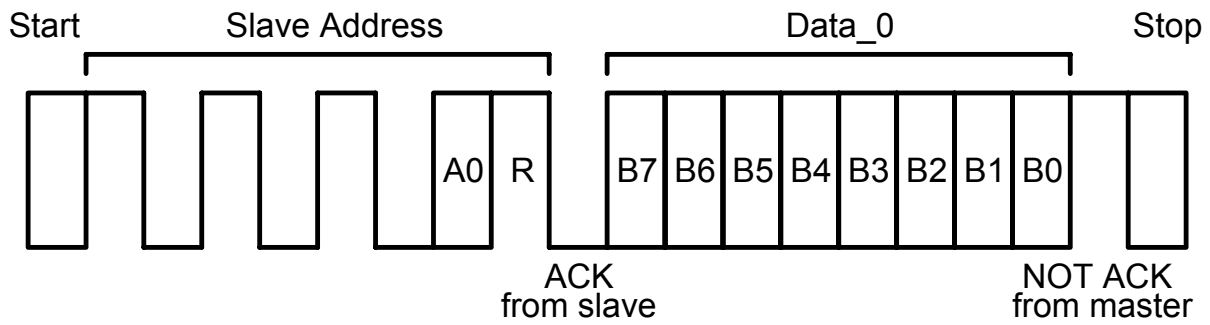
Table 7-2-1. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	B7	B6	B5	B4	B3	B2	B1	B0
TTP239-COBN	1	0	1	0	1	0	1	R

Note :

The SDA and SCL pins have Diode protective circuit. So when use two pins of TTP239-COBN in the I2C-bus interface system. Do not propose to use the different voltage with the other devices in the I2C-bus interface system. That avoids to occurring the leakage current in the system.





Note : Data\_0 : B7~B0 are TP0~TP7 on/off status. 0 is key off, 1 is key on.

Figure 7-2-1. Read Operation Sequence

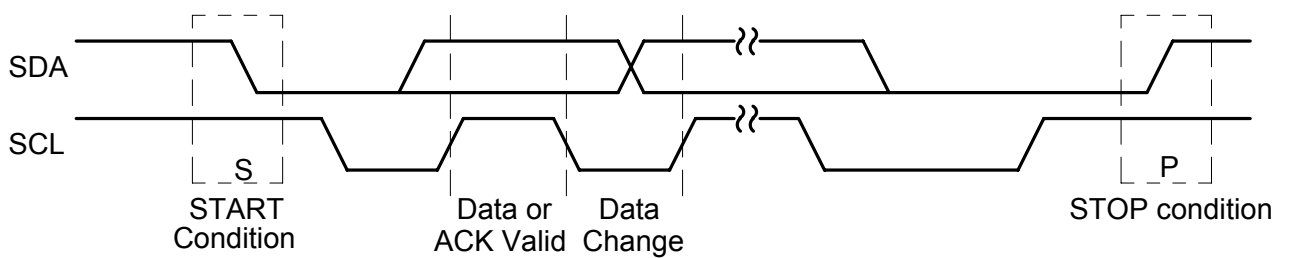


Figure 7-2-2. Data Transmission Sequence

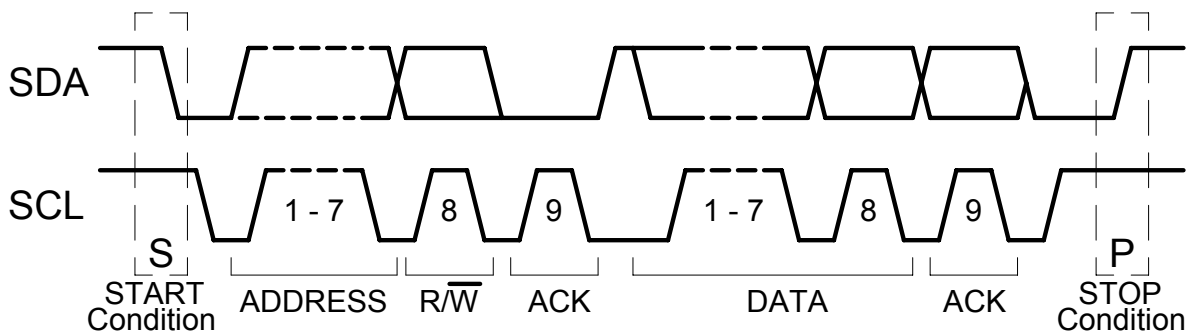


Figure 7-2-3. A complete data transfer

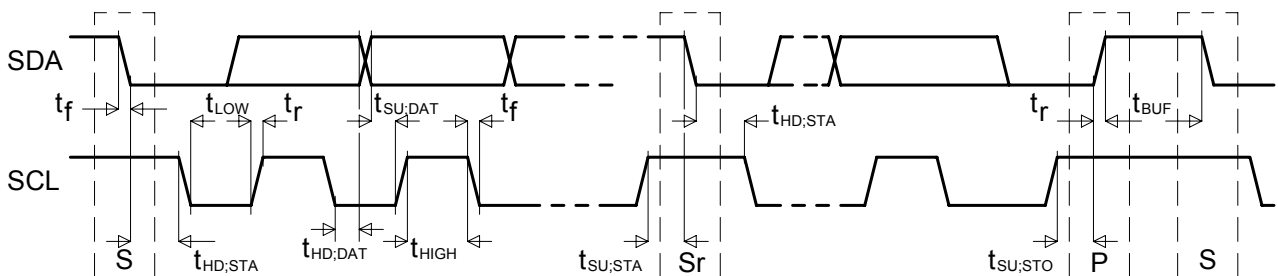
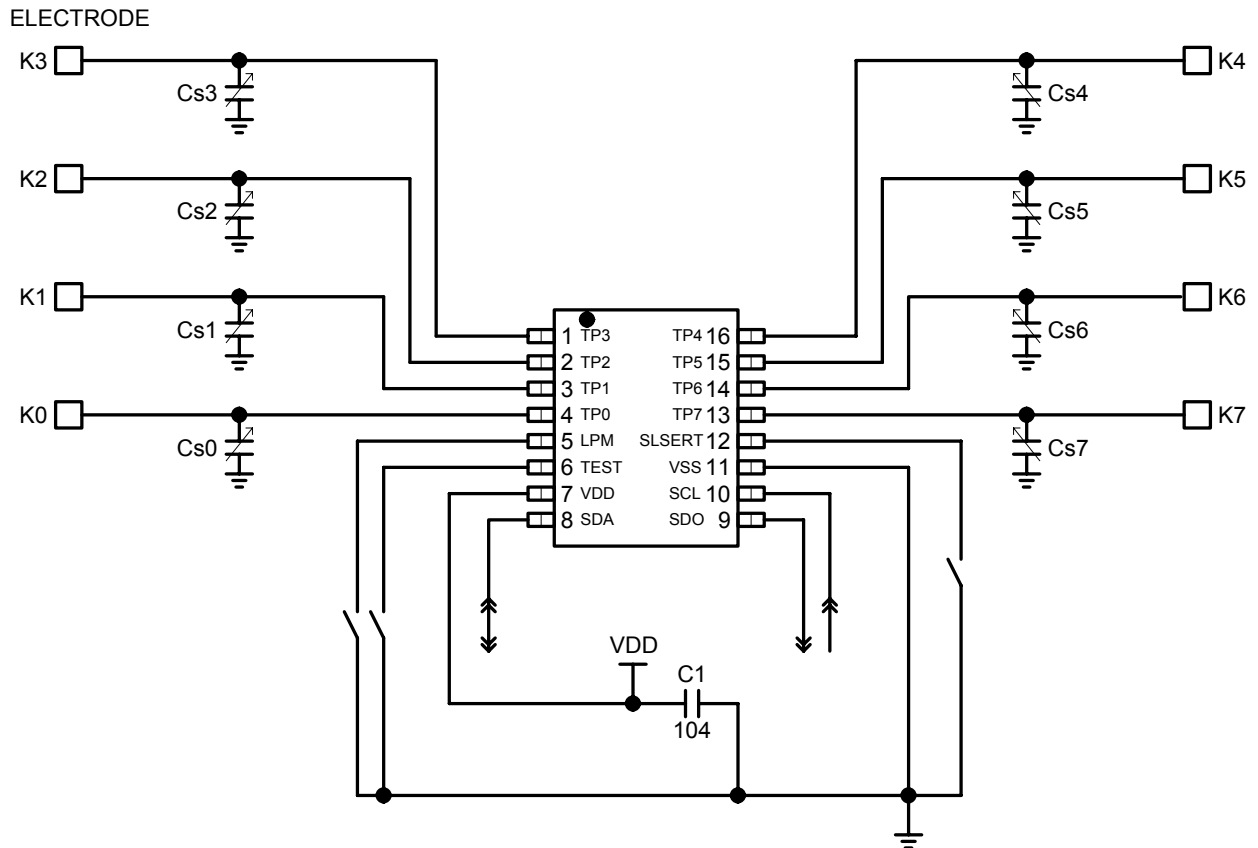


Figure 7-2-4. Definition of timing for F/S-mode devices on the I<sup>2</sup>C-bus

Table 7-2-2. Characteristics of the SDA and SCL bus lines for F/S-mode I<sup>2</sup>C-bus devices

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f <sub>SCL</sub>		100		400	KHz
LOW period of the SCL clock	t <sub>LOW</sub>	4.7		1.3		us
HIGH period of the SCL clock	t <sub>HIGH</sub>	4.0		0.6		us
Hold time (repeated) START condition	t <sub>HD;STA</sub>	4.0		0.6		us
Set-up time for a repeated START condition	t <sub>SU;STA</sub>	4.7		0.6		us
Data hold time	t <sub>HD;DAT</sub>	0		0		us
Data set-up time	t <sub>SU;DAT</sub>	250		100		ns
Rise time of both SDA and SCL signals	t <sub>r</sub>		1000		300	ns
Fall time of both SDA and SCL signals	t <sub>f</sub>		300		300	ns
Set-up time for STOP condition	t <sub>SU;STO</sub>	4.0		0.6		us
Bus free time between a STOP and START condition	t <sub>BUF</sub>	4.7		1.3		us
Capacitive load for each bus line	C <sub>b</sub>		400		400	pF

## Application circuit

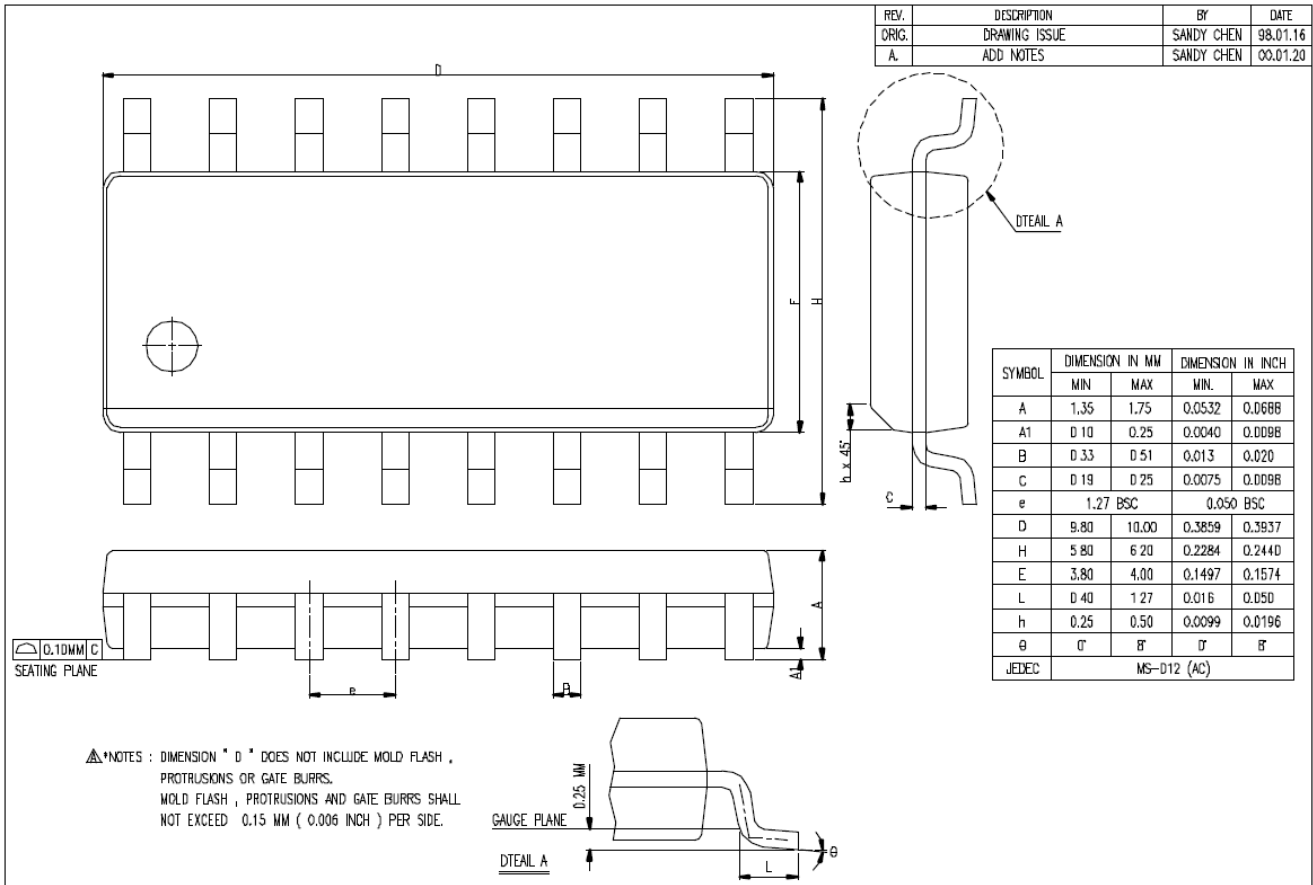


P.S. :

1. On PCB, the length of lines from touch pad to IC pin shorter is better. And the lines do not parallel and cross with other lines.
2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP239-COBN).
5. The capacitance Cs0~Cs7 can be used to adjust the sensitivity. The value of Cs0~Cs7 use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range of Cs0~Cs7 value are 1~50pF.
6. The sensitivity adjustment capacitors (Cs0~Cs7) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.
7. The SCL pin is input only, and it can not float.

## Package outline

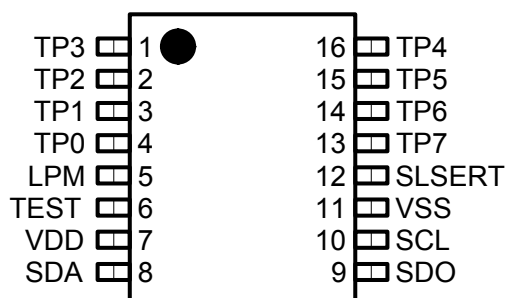
Package Type: SOP-16



## Package configuration

TTP239-COBN

Package Type SOP-16



## Ordering Information

### TTP239-COBN

Package Type	Chip Type	Wafer Type
TTP239-COBN	No support	No support

**REVISION HISTORY**

1. 2016/9/1  
- Initial version : V1.0