TTU983　8 Bits TV game system

Features：

System :

1. CPU : 6502
2. Internal Working Ram : 2K Bytes
3. Internal Video Ram : 2K Bytes
4. DMA
5. One bus mode : 8 bits data bus or 16 bits data bus
6. Bank decoder for expandable memory up to 2M Bytes
7. TV signal output (NTSC, PAL-B, PAL-M, PAL-N)

Peripheral Application :

Bulit-in joystick1
Joystick 2, Light gun

Graphic Processor

1. Resolution : 256 X240 pixel
2. 4 color mode for each font
3. 64 sprites in one frame
4. 25 Color pallette

Sound Generator

1. 3 rhythm channels
2. 1 noise channel
3. 1 PCM voice channel

General Description：

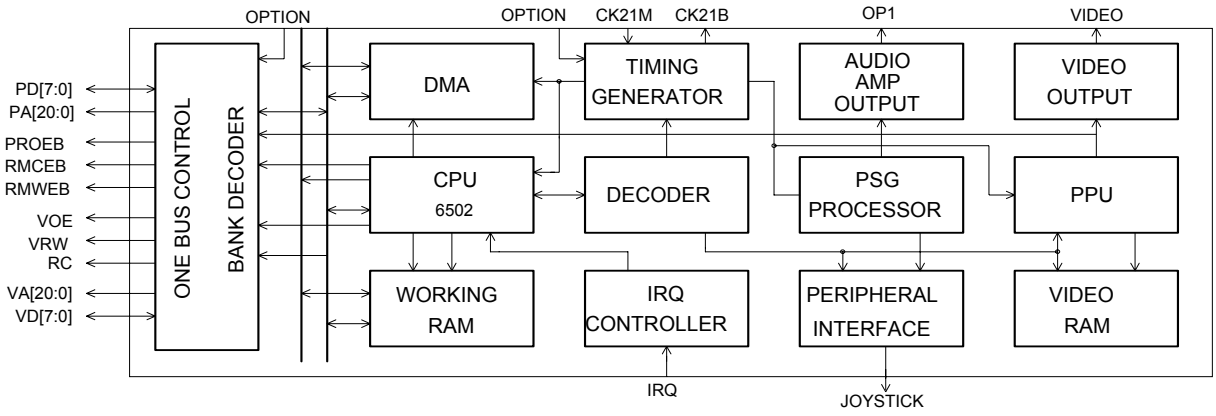
TTU983 is a single chip microprocessor for use in TV game. It is composed of CPU(6502), PPU(picture processor unit), PSG(programmable sound generator), 2K Bytes working RAM, 2K Bytes video RAM, DMA unit, and other control circuit.

Video : TTU983 apply to display variable animated cartoon. In background picture, it supply 2-page size in the screen; In sprite picture, it also supply 64 sprites per frame. Besides, the X and Y coordinate positions is programmable to display the actual area

AUDIO : TTU983 apply to multi-mix sound output. It with 5 channels programmable sound generator, include 3 rhythm channels, 1 noise channel, and 1 PCM voice channel.

TTU983 can combine program and video bus into one bus mode. Thus it needs only one memory IC as the program memory and video memory. Under one bus mode, programmer specifies the program and video bank individually in the same external memory and then TTU983 will combine the two independent buses into one bus. External memory can be extended to 4M bytes through the function decoder of TTU983.

Block Diagram：



Pad / Pin Description：

PAD Name	I/O	DESCRIPTION
PA[0:14]	O	Address bus A0-A14 of CPU
PA[15:20]		On one bus mode or internal two bus mode, ROM or flash Address bus A15 – A20.
PD[0:7]	I/O	Data bus bit 0-7 of CPU .
RMCEB	O	On external one bus mode or internal two bus mode, $6000-7FFF chip enable signal (Low chip enable). On external two bus mode, CPU clock 1.8Mhz (CK18).
RMWEB	O	On one bus mode or internal two bus mode, $6000-7FFF write enable signal (Low write enable). On external two bus mode, CPU read/write signal (RWB).
PROEB	O	On external one bus mode or two bus mode, ROM or flash chip enable signal (Low chip enable).
VA[0:12]	O	On two bus mode, Address bus A0-A12 of PPU.
VA13	O	On internal two bus mode, Address A13 of PPU On internal one bus mode, ROM or flash chip enable signal (Low chip enable),
VA14	O	On internal two bus mode, Address A14 of PPU On internal one bus mode, $6000-7FFF chip enable signal (Low chip enable).
VA[15:17]	O	On internal two bus mode, Address bus A15-A17 of PPU.
VA18	I/O	On internal two bus mode, Address A18 of PPU. On external two bus mode, Internal Video Ram address A10.
VA19	I/O	On internal two bus mode, Address A19 of PPU. On external two bus mode, CPU interrupt input signal (IRQB) On one bus 8 bit mode, ROM or flash Address A22

VA20	O	On internal two bus mode, Address A20 of PPU On one bus mode, ROM or flash Address A21.
VD[0:7]	I/O	On two bus mode, Data bus bit 0-7of PPU. On one bus 16 bit mode, Data bus bit 8-15
VRW	O	Read/Write control signal of PPU memory
VOE	O	PPU memory read enable signal (Low read enable)
RC	O	PPU memory chip enable signal(Low chip enable)
VSS	P	VSS power pin
VDD	P	VDD power pin
PORN,F50R6	I	TV system select pin : (pull-high) “**11**“ : PAL-B , “**10**“ : PAL-M, “**01**“ : PAL-N , “**00**“ : NTSC
OPT_EXTB	I	Internal or external mode select pin : (pull-high) “**1**“ : internal mode, “**0**“ : external mode.
OPT_XONE,	I	One bus mode select pin :(pull-high) “**1**“ : One bus mode, “**0**“ : Two bus mode
OPT_XBYTE	I	8 bits or 16 bit data bus select pin for one bus mode : “**1**“ : 8 bits data bus, “**0**“: 16 bits data bus A0 will decide low byte PD[7:0] data or high byte VD[7:0] data for 8 bits data bus
TEST2	I	For function test2 (pull-high)
TEST1	I	For function test1 (pull-high)
CK21B	O	System clock output , to crystal oscillator
CK21M	I	System clock input , to crystal oscillator
VIDEO	O	Video signal output
OP1	O	Audio signal output
RESTB	I	System reset input , “**0**” = Reset ; “**1**” : Normal (pull-high)
TESTB	I	Test mode control pin, ‘**0**” :Test mode, “**1**” : Normal (pull-high)
LEFT, RIGHT, UP DOWN, A, B START, SEL		Built-in jostick1 press key (pull-high)
H32,H16,H8	O	32Hz, 16Hz, 8Hz frequency output for turbo key
Q0	O	Q0 signal for joystick2
CUP47	O	CUP47 signal for joystick2
TEST_Q1	O	Output1 for test function
D047	I	D047 signal for joystick2
TEST_Q2	O	Output2 for test function
TEST_Q3	O	Output3 for test function
TEST_Q4	O	Output4 for test function
D347	I	D347 signal for joystick2
D447	I	D447 signal for joystick2
TEST_Q5	O	Output5 for test function
TEST_Q6	O	Output6 for test function

TTU983 bank decoder (C3 programable) :

1. The write command PROT $5000,The action use A12,A13,A14,A15,RWB to control.
   Each write command function as below :

(1). The 1'st write command : D0-D7 control START ADDRESS VA10 - VA17 of CHR-ROM.
CHR ADDRESS cooresponding WRITE DATA as below :

ADDRESS	VA17	VA16	VA15	VA14	VA13	VA12	VA11	VA10
INPUT DATA	D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	W1Q7	W1Q6	W1Q5	W1Q4	W1Q3	W1Q2	W1Q1	W1Q0

(2). The 2'nd write command : D0-D7 control START ADDRESS PA13 - PA20 of PRG-ROM.
PRG ADDRESS cooresponding WRITE DATA as below :

ADDRESS	PA20	PA19	PA18	PA17	PA16	PA15	PA14	PA13
INPUT DATA	D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	W2Q7	W2Q6	W2Q5	W2Q4	W2Q3	W2Q2	W2Q1	W2Q0

(3). The 3'rd write command : D0-D3 control GAME SIZE and START ADDRESS of CHR-ROM.
: D4-D7 control START ADDRESS HIGH-BIT VA18-VA21 of CHR-ROM.
CHR GAME SIZE and START ADDRESS cooresponding WRITE DATA as below :
(A).CHR GAME SIZE cooresponding WRITE DATA :

INPUT DATA				CHR 之 ADDRESS								
D3	D2	D1	D0	VA17	VA16	VA15	VA14	VA13	VA12	VA11	VA10	GAME SIZE
0	X	X	X	W1Q7	W1Q6	W1Q5	W1Q4	W1Q3	W1Q2	W1Q1	W1Q0	8K
1	0	0	0	W1Q7	W1Q6	W1Q5	W1Q4	W1Q3	W1Q2	W1Q1	C3CA10	16K
1	0	0	1	W1Q7	W1Q6	W1Q5	W1Q4	W1Q3	W1Q2	C3CA11	C3CA10	32K
1	0	1	0	W1Q7	W1Q6	W1Q5	W1Q4	W1Q3	C3CA12	C3CA11	C3CA10	64K
1	0	1	1	W1Q7	W1Q6	W1Q5	W1Q4	C3CA13	C3CA12	C3CA11	C3CA10	128K
1	1	0	0	W1Q7	W1Q6	W1Q5	C3CA14	C3CA13	C3CA12	C3CA11	C3CA10	256K
1	1	0	1	W1Q7	W1Q6	C3CA15	C3CA14	C3CA13	C3CA12	C3CA11	C3CA10	512K
1	1	1	0	W1Q7	C3CA16	C3CA15	C3CA14	C3CA13	C3CA12	C3CA11	C3CA10	1M
1	1	1	1	C3CA17	C3CA16	C3CA15	C3CA14	C3CA13	C3CA12	C3CA11	C3CA10	2M

(B). CHR HIGH-BIT START ADDRESS cooresponding WRITE DATA :

ADDRESS	VA21	VA20	VA19	VA18
INPUT DATA	D7	D6	D5	D4
OUTPUT	W3Q7	W3Q6	W3Q5	W3Q4

(4).The 4'th write command : D0-D5 control GAME SIZE and START ADDRESS of PRG-ROM.

(A) PRG GAME SIZE cooresponding WRITE DATA :

INPUT DATA						PRG 之 ADDRESS						
D5	D4	D3	D2	D1	D0	PA18	PA17	PA16	PA15	PA14	PA13	GAME SIZE
1	1	1	1	1	1	W2Q5	W2Q4	W2Q3	W2Q2	W2Q1	W2Q0	64K
1	1	1	1	1	0	W2Q5	W2Q4	W2Q3	W2Q2	W2Q1	C3PA13	128K
1	1	1	1	0	0	W2Q5	W2Q4	W2Q3	W2Q2	C3PA14	C3PA13	256K
1	1	1	0	0	0	W2Q5	W2Q4	W2Q3	C3PA15	C3PA14	C3PA13	512K
1	1	0	0	0	0	W2Q5	W2Q4	C3PA16	C3PA15	C3PA14	C3PA13	1M
1	0	0	0	0	0	W2Q5	C3PA17	C3PA16	C3PA15	C3PA14	C3PA13	2M
0	0	0	0	0	0	C3PA18	C3PA17	C3PA16	C3PA15	C3PA14	C3PA13	4M

PRG HIGH-BIT START ADDRESS cooresponding WRITE DATA :

ADDRESS		PA21
INPUT DATA	D7	D6
OUTPUT	LOCK	W4Q6

(B) The 4'th write command, if D7 be write "1", then the Address cooresponding value be just set and lock in the preceding 4 times write command.
Unless power-on again or press reset key, the write command is invalid

2. POWER-ON , internal REGISTER be INITAL " 0 " .
3. PORT 6000 - 7FFF be retain for external program RAM use

TTU983 One bus and Two bus pin mapping :

There are Two bus mode and One bus mode for TTU983 function.
One bus mode have 16 bits(D15-D0) data bus and 8 bits(D7-D0) data bus.

1.Two bus mode :

PRG-ROM address A0-A20 : PA0-PA20
PRG-ROM data D7-D0 : PD7-PD0
CHR-ROM address A0-A20 : VA0-VA20
CHR-ROM data D7-D0 : VD7-VD0

2.One bus mode for 16 bits data bus : can use TONTEK transfer program

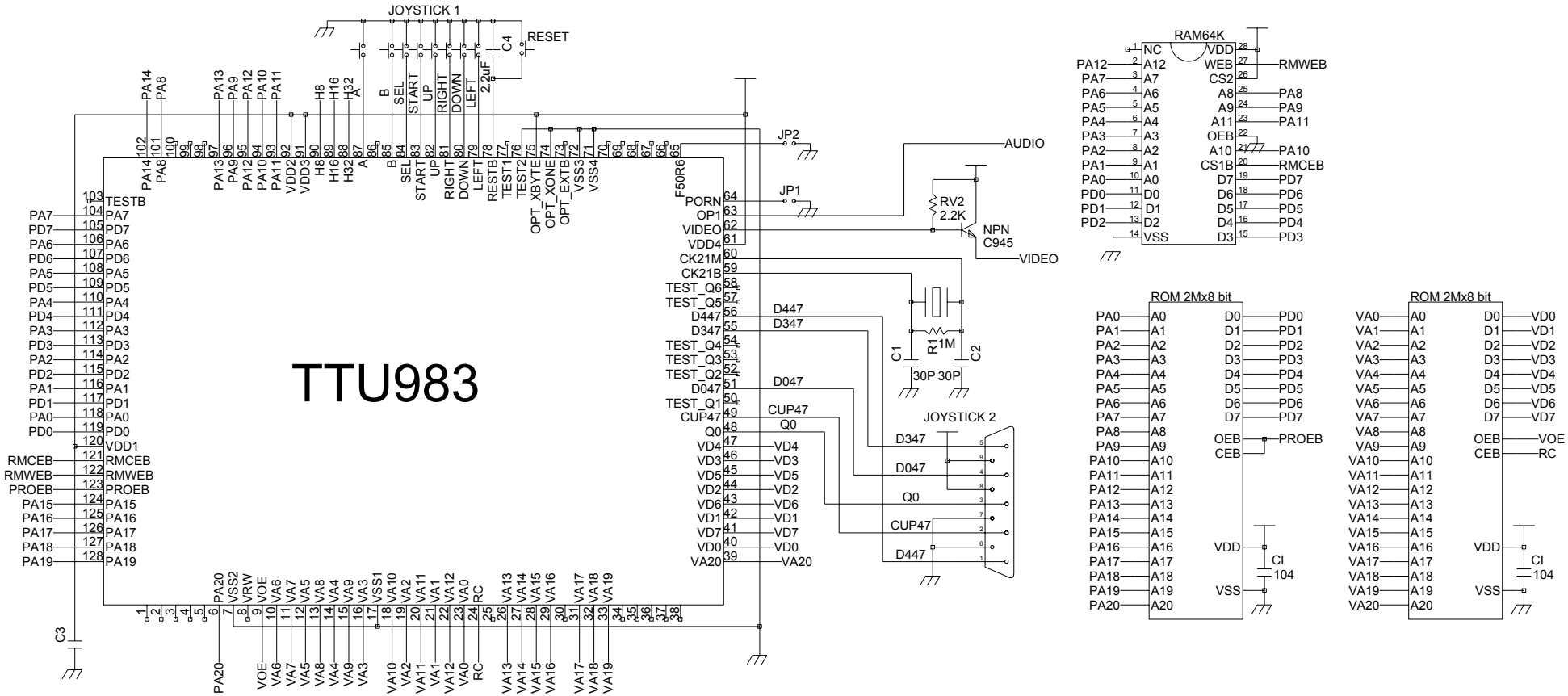
ROM address A0-A21 : PA0-PA21
ROM data D7-D0 : PD7-PD0
D15-D8 : VD7-VD0
(D7-D0 save PRG-ROM data, D15-D8 save CHR-ROM data)

Use one bus mode for 16 bits application , TONTEK offer transfer program, the transfer program can combine 2bus data(2 file) into 1bus data(1 file)

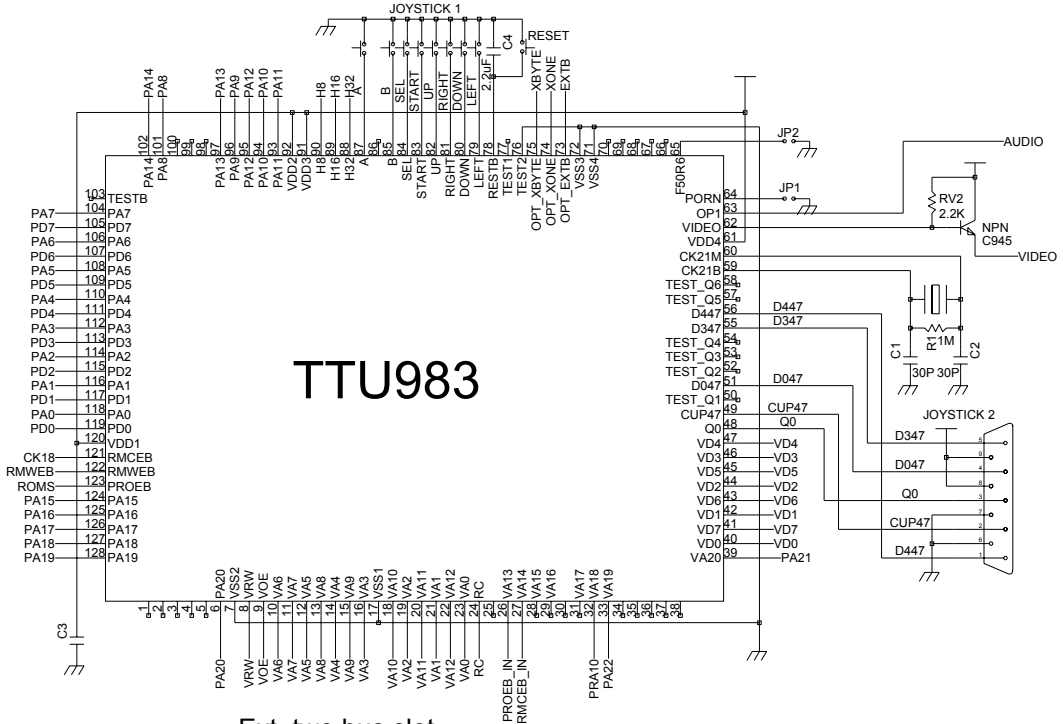
3.One bus mode for 8 bits data bus :

ROM address A0-A21 : PA1-PA22
ROM data D7-D0 : PD7-PD0

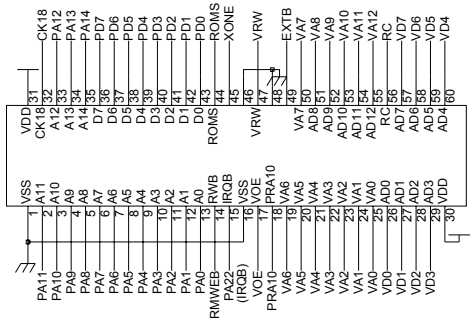
TTU983 internal two bus mode application

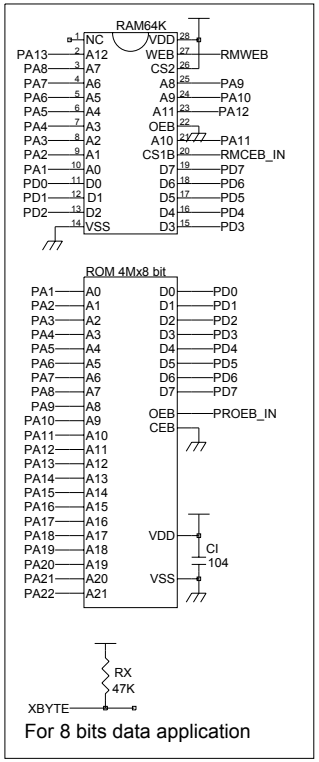


TTU983 internal one bus mode with external two bus slot application

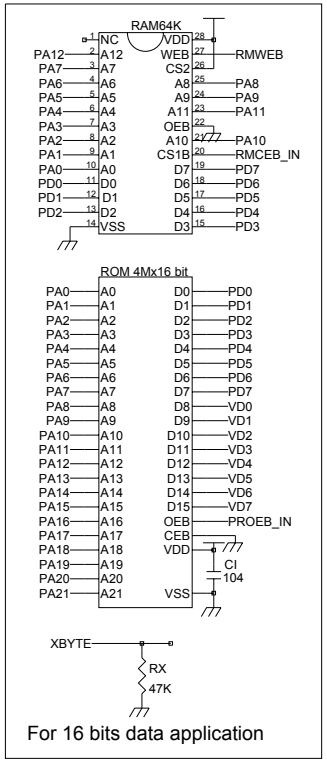


Ext two bus slot





For 8 bits data application

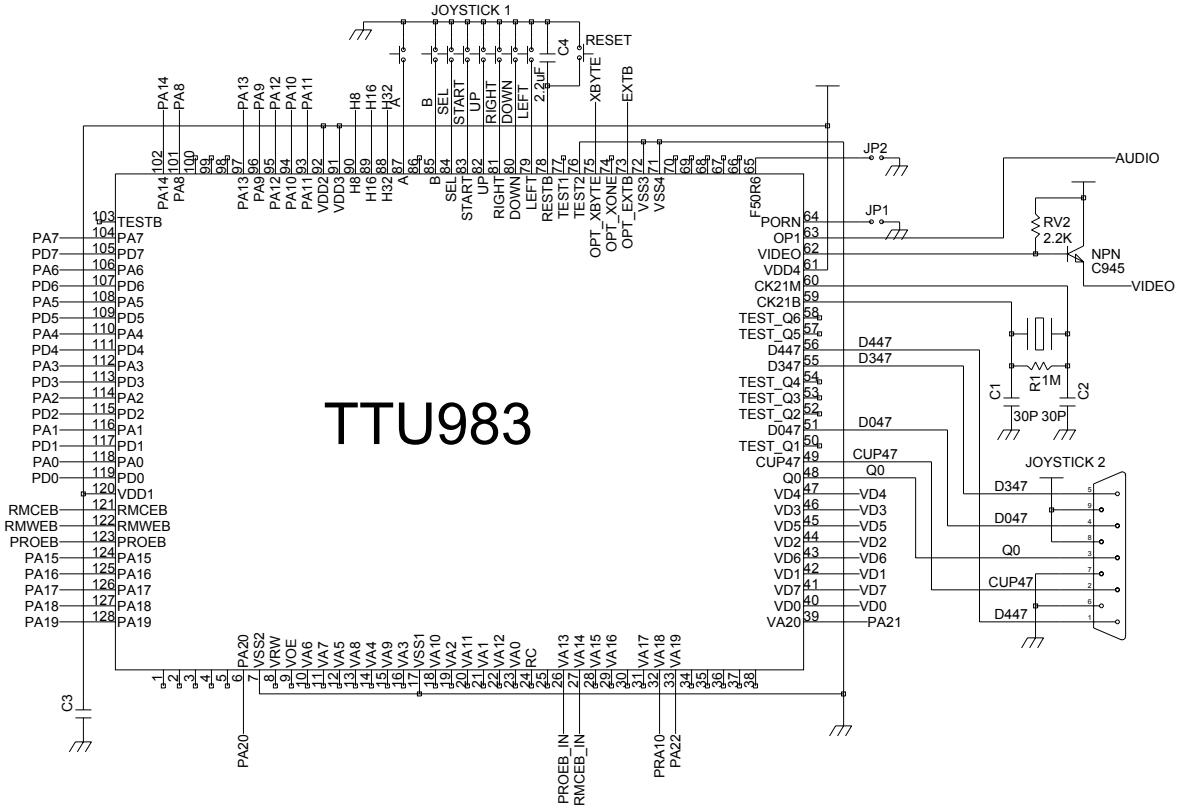


For 16 bits data application

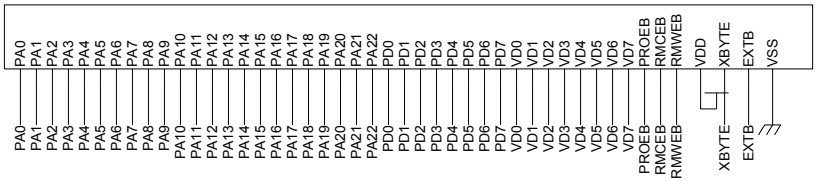
Note : Use one bus for 16 bits data application, can use TONTEK transfer program
The transfer program can combine 2bus data (2 file) into 1bus data(1 file)

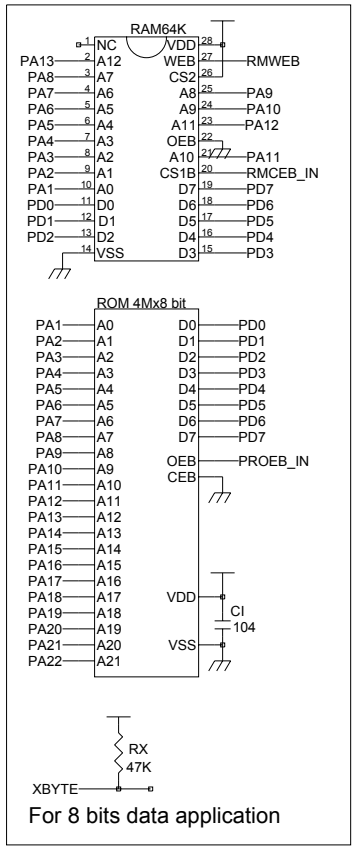
Reference Only
Version ： 2.1
Date：2007/08/02

TTU983 internal one bus mode with external one bus slot application

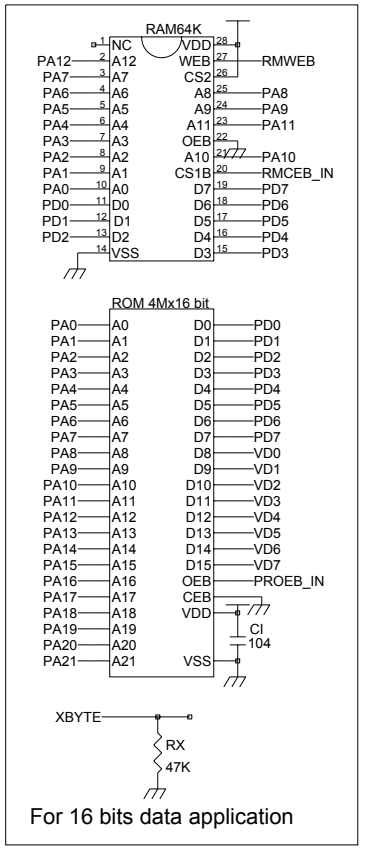


Ext one bus slot





For 8 bits data application

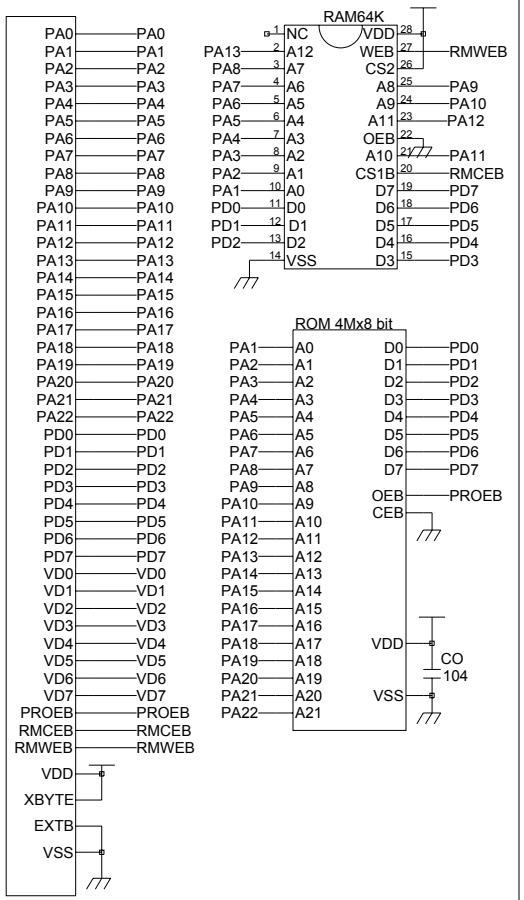


For 16 bits data application

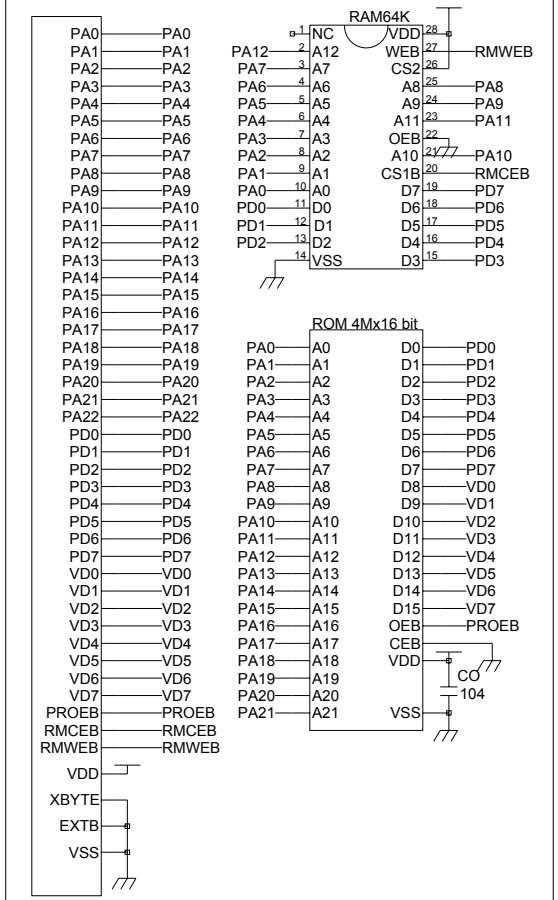
Note : Use one bus for 16 bits data application, can use TONTEK transfer program
The transfer program can combine 2bus data (2 file) into 1bus data(1 file)

TTU983 external one bus mode application

TTU983 external one bus mode
for 8 bits data application

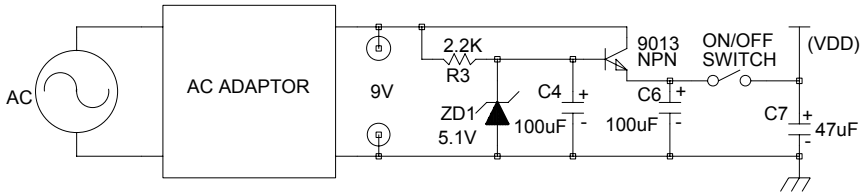


TTU983 external one bus mode
for 16 bits data application

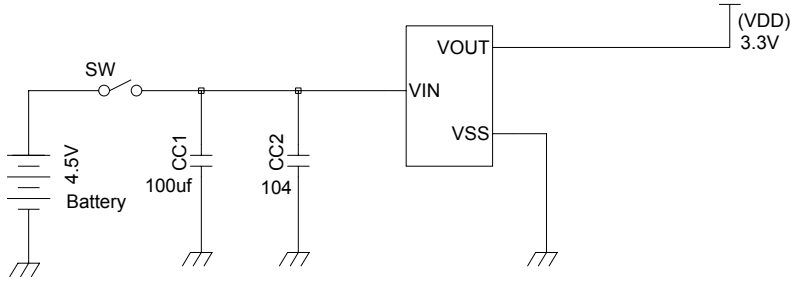


Note : Use one bus for 16 bits data application, can use TONTEK transfer program
The transfer program can combine 2bus data (2 file) into 1bus data(1 file)

VDD application : for AC power source

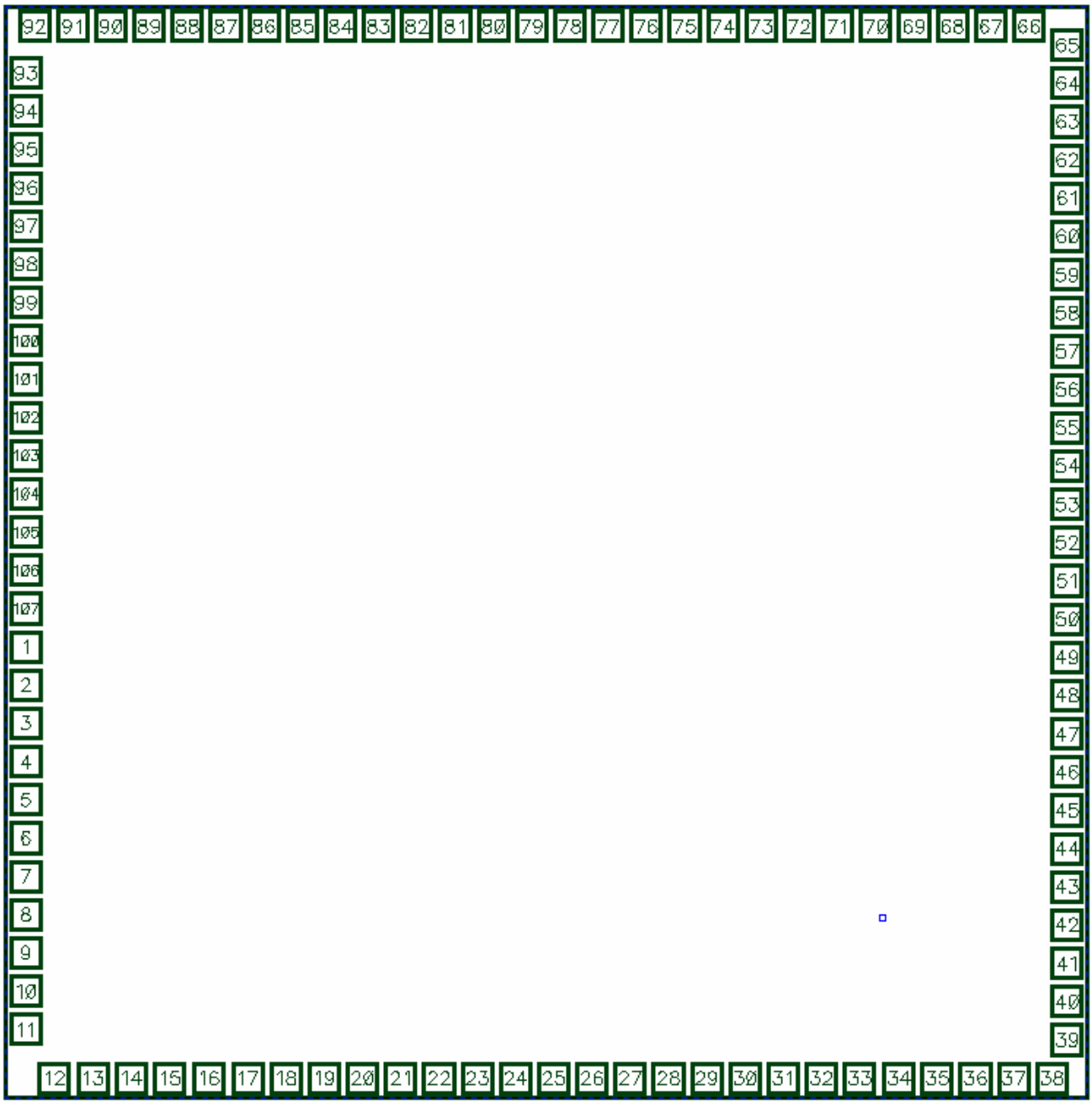


VDD application : for Battery power source



TV system application

T V. SYSTEM	CRYSTAL (MHZ)	JP1(PORN)	JP2(F50R6)
PAL B	26.601712	OPEN	OPEN
NTSC	21.477270	SHORT	SHORT
PAL M	21.453669	OPEN	SHORT
PAL N	21.492337	SHORT	OPEN


92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66
65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39
38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12
11 10 9 8 7 6 5 4 3 2 1 107 106 105 104 103 102 101 100 99 98 97 96 95 94 93

TTU983 Chip size: 3410um X 3440um

NO	NAME	X=	Y=
1	VA1	-1593.000	-288.950
2	VA12	-1593.000	-405.950
3	VA0	-1593.000	-522.950
4	RC	-1593.000	-639.950
5	VA13	-1593.000	-756.950
6	VA14	-1593.000	-873.950
7	VA15	-1593.000	-990.950
8	VA16	-1593.000	-1107.950
9	VA17	-1593.000	-1224.950
10	VA18	-1593.000	-1341.950
11	VA19	-1593.000	-1458.950
12	VA20	-1505.000	-1608.000
13	VD0	-1388.000	-1608.000
14	VD7	-1271.000	-1608.000
15	VD1	-1151.650	-1608.000
16	VD6	-1033.050	-1608.000
17	VD2	-913.750	-1608.000
18	VD5	-796.750	-1608.000
19	VD3	-679.750	-1608.000
20	VD4	-562.750	-1608.000
21	Q0	-445.750	-1608.000
22	CUP47	-328.750	-1608.000
23	TEST_Q1	-211.750	-1608.000
24	D047	-94.750	-1608.000
25	TEST_Q2	22.250	-1608.000
26	TEST_Q3	139.250	-1608.000
27	TEST_Q4	256.250	-1608.000
28	D347	373.250	-1608.000
29	D447	490.250	-1608.000
30	TEST_Q5	607.250	-1608.000
31	TEST_Q6	724.250	-1608.000
32	CK21B	841.250	-1608.000
33	CK21M	958.250	-1608.000
34	VDD:	1078.500	-1608.000
35	VIDEO	1195.500	-1608.000
36	OP1	1312.500	-1608.000
37	PORN	1429.500	-1608.000
38	F50R6	1546.500	-1608.000
39	VSS:	1593.000	-1491.000
40	VSS:	1593.000	-1374.000

41	OPT_EXTB	1593.000	-1257.000
42	OPT_XONE	1593.000	-1140.000
43	OPT_XBYTE	1593.000	-1023.000
44	TEST2	1593.000	-906.000
45	TEST1	1593.000	-789.000
46	RESTB	1593.000	-672.000
47	LEFT	1593.000	-555.000
48	DOWN	1593.000	-438.000
49	RIGHT	1593.000	-321.000
50	UP	1593.000	-204.000
51	START	1593.000	-87.000
52	SEL	1593.000	30.000
53	B	1593.000	147.000
54	A	1593.000	264.000
55	H32	1593.000	381.000
56	H16	1593.000	498.000
57	H8	1593.000	615.000
58	VDD:	1593.000	732.000
59	VDD:	1593.000	849.000
60	PA11	1593.000	966.000
61	PA10	1593.000	1083.000
62	PA12	1593.000	1200.000
63	PA9	1593.000	1317.000
64	PA13	1593.000	1434.000
65	PA8	1593.000	1551.000
66	PA14	1476.000	1608.000
67	TESTB	1359.000	1608.000
68	PA7	1241.450	1608.000
69	PD7	1124.450	1608.000
70	PA6	1007.450	1608.000
71	PD6	890.450	1608.000
72	PA5	773.450	1608.000
73	PD5	656.450	1608.000
74	PA4	539.450	1608.000
75	PD4	422.450	1608.000
76	PA3	305.450	1608.000
77	PD3	188.450	1608.000
78	PA2	71.450	1608.000
79	PD2	-45.550	1608.000
80	PA1	-162.550	1608.000
81	PD1	-279.550	1608.000
82	PA0	-396.550	1608.000
83	PD0	-513.550	1608.000
84	VDD:	-630.550	1608.000
85	RMCEB	-747.550	1608.000
86	RMWEB	-864.550	1608.000

87	PROEB	-981.550	1608.000
88	PA15	-1098.550	1608.000
89	PA16	-1215.550	1608.000
90	PA17	-1332.550	1608.000
91	PA18	-1449.550	1608.000
92	PA19	-1566.550	1608.000
93	PA20	-1593.000	1466.050
94	VSS:	-1593.000	1349.050
95	VRW	-1593.000	1232.050
96	VOE	-1593.000	1115.050
97	VA6	-1593.000	998.050
98	VA7	-1593.000	881.050
99	VA5	-1593.000	764.050
100	VA8	-1593.000	647.050
101	VA4	-1593.000	530.050
102	VA9	-1593.000	413.050
103	VA3	-1593.000	296.050
104	VSS:	-1593.000	179.050
105	VA10	-1593.000	62.050
106	VA2	-1593.000	-54.950
107	VA11	-1593.000	-171.950

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.ORDER INFORMATION

a. **Package form : TTU983**
b. **Chip form : TCU983**