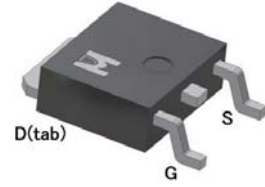
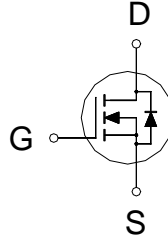


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	100V
$R_{DS(on)}$ (MAX.)	50m $\Omega$
$I_D$	25A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	25	A
	$T_C = 100\text{ }^\circ\text{C}$		17	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	100	
Avalanche Current		$I_{AS}$	25	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 25\text{A}, R_G = 25\Omega$	$E_{AS}$	31.25	mJ
Repetitive Avalanche Energy <sup>2</sup>	$L = 0.05\text{mH}$	$E_{AR}$	15.6	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	41	W
	$T_C = 100\text{ }^\circ\text{C}$		16	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.0	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

ELECTRICAL CHARACTERISTICS ( $T_c = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	2.8	4.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 25V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	25			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 25A$		43	50	$m\Omega$
		$V_{GS} = 7V, I_D = 15A$		50	60	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 25A$		28		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		2140		$pF$
Output Capacitance	$C_{oss}$			143		
Reverse Transfer Capacitance	$C_{rss}$			102		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.0		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 50V, V_{GS} = 10V,$ $I_D = 25A$		35		$nC$
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			10.5		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			9.5		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 50V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		20		$nS$
Rise Time <sup>1,2</sup>	$t_r$			15		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			50		
Fall Time <sup>1,2</sup>	$t_f$			15		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				25	A
Pulsed Current <sup>3</sup>	$I_{SM}$				100	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = 25A, di_F/dt = 100A / \mu S$		60		nS
Reverse Recovery Charge	$Q_{rr}$			120		nC

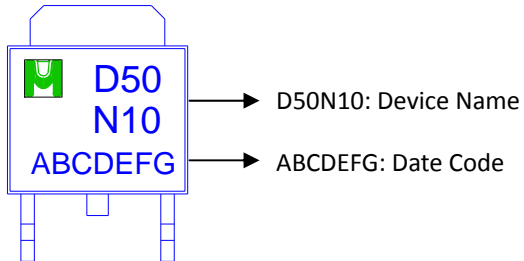
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

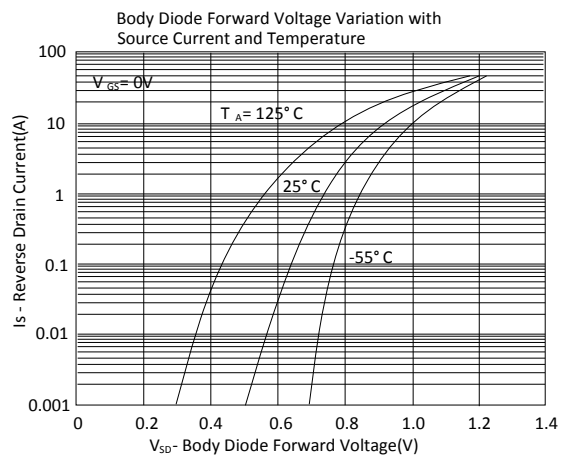
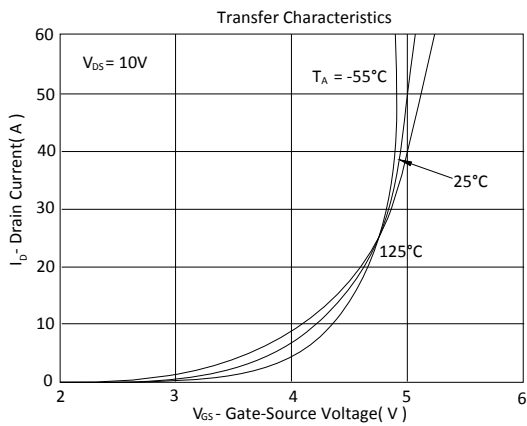
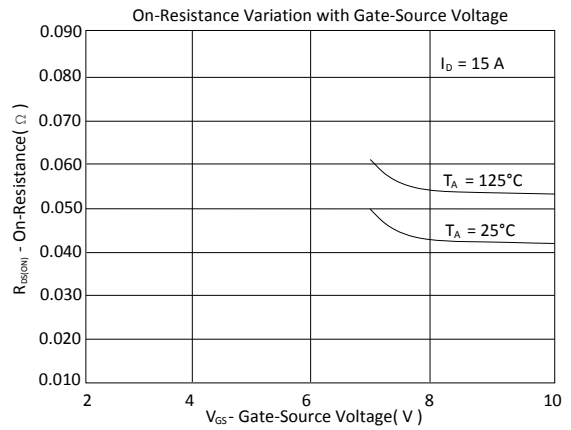
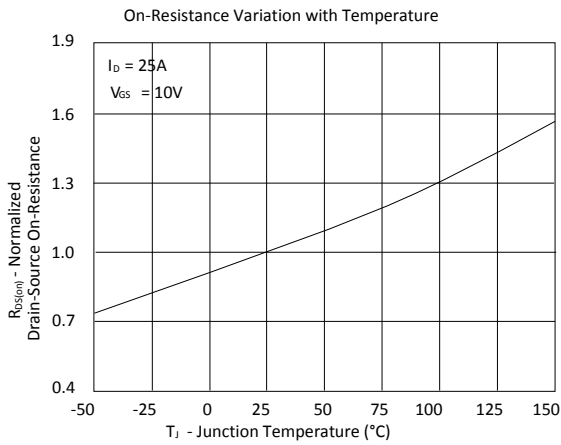
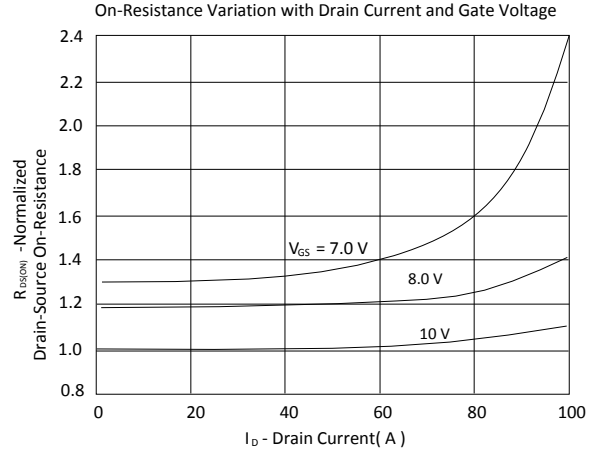
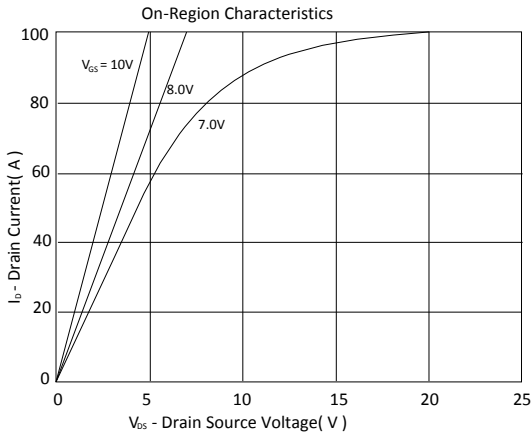
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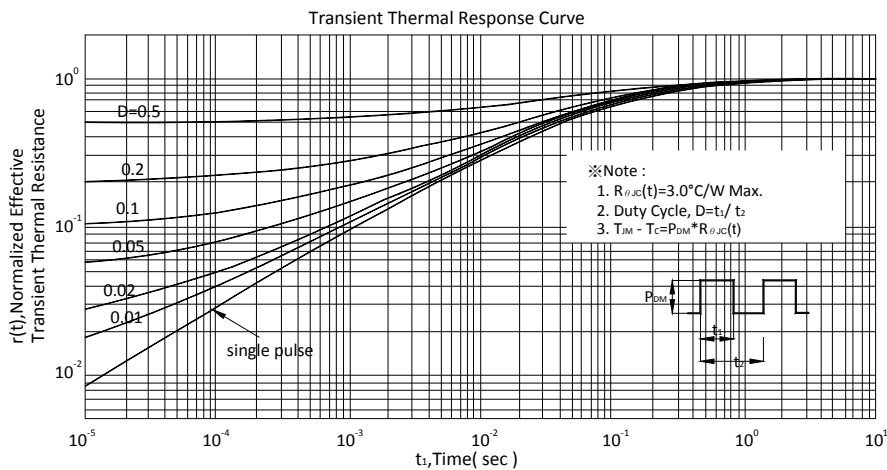
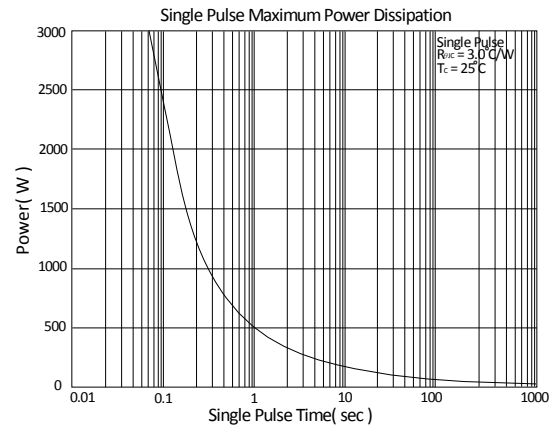
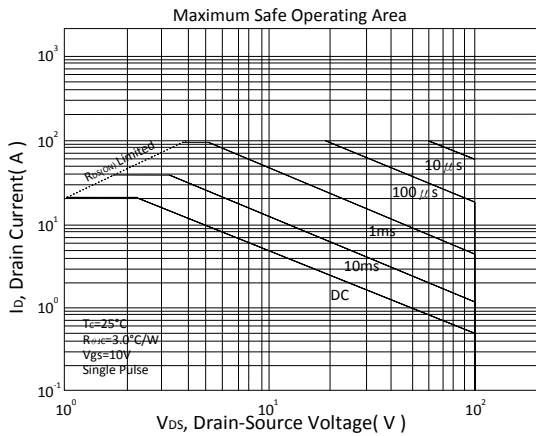
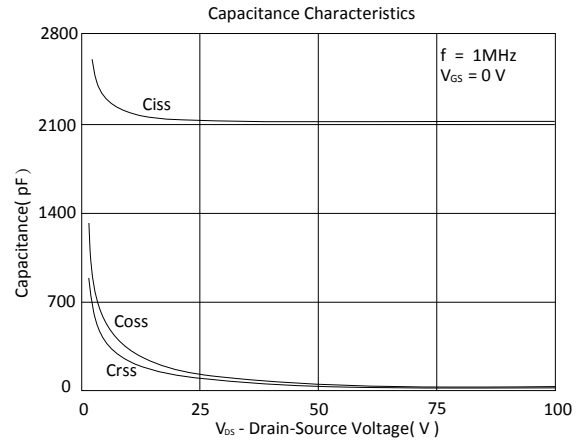
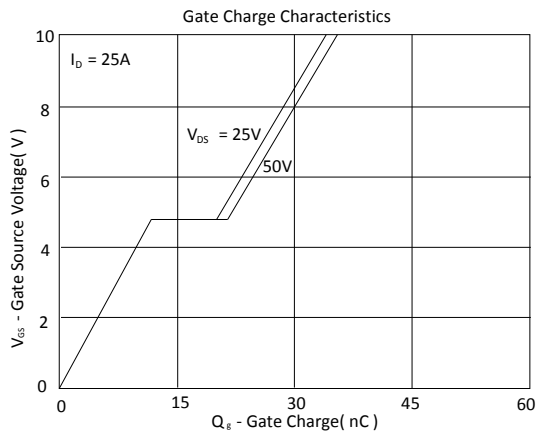
Device Name: EMD50N10A for DPAK (TO-252)





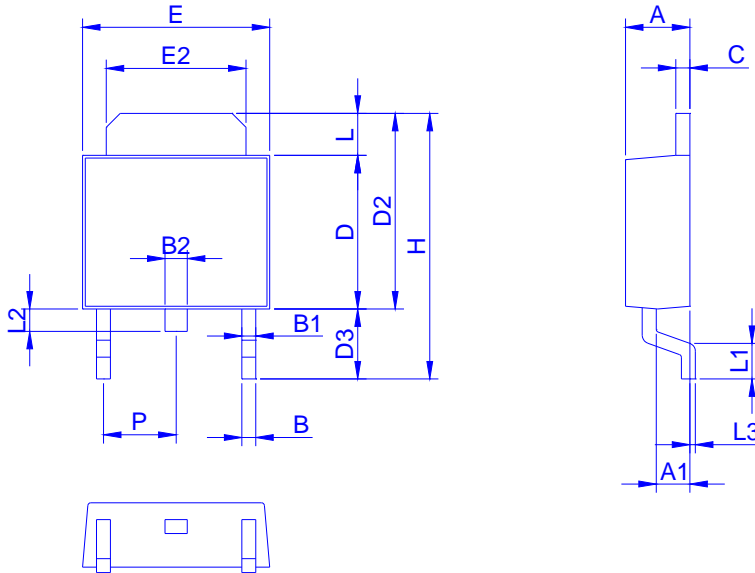
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

