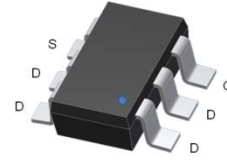
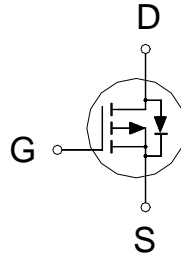


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	-20V
$R_{DS(on) (MAX.)}$	60m $\Omega$
$I_D$	-4.5A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	-4.5	A
	$T_A = 70\text{ }^\circ\text{C}$		-3.2	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-18	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	1.25	W
	$T_A = 70\text{ }^\circ\text{C}$		0.8	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		100	$^\circ\text{C}/\text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$



ELECTRICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.3	-0.75	-1.2	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16V, V_{GS} = 0V$			-1	$\mu A$
		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-4.5			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -3.5A$		50	60	$m\Omega$
		$V_{GS} = -2.5V, I_D = -2.5A$		75	96	
		$V_{GS} = -1.8V, I_D = -1.0A$		150	250	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -3.5A$		10		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		382		$pF$
Output Capacitance	$C_{oss}$			70		
Reverse Transfer Capacitance	$C_{rss}$			60		
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3.5A$		7.2		$nC$
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			1.2		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			2.3		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$		17		$nS$
Rise Time <sup>1,2</sup>	$t_r$			32		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			37		
Fall Time <sup>1,2</sup>	$t_f$			32		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				-4.5	A
Pulsed Current <sup>3</sup>	$I_{SM}$				-18	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			-1.2	V

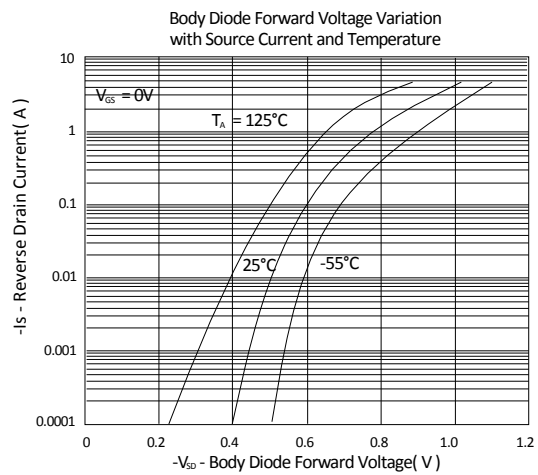
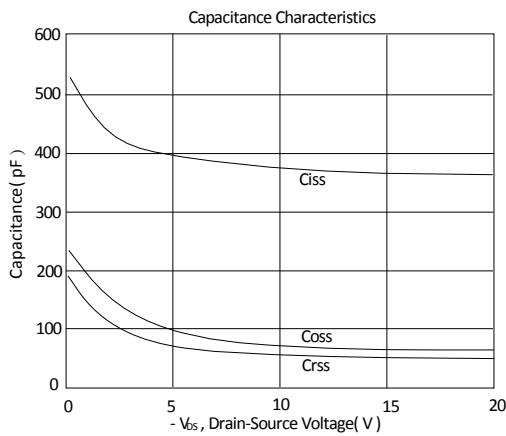
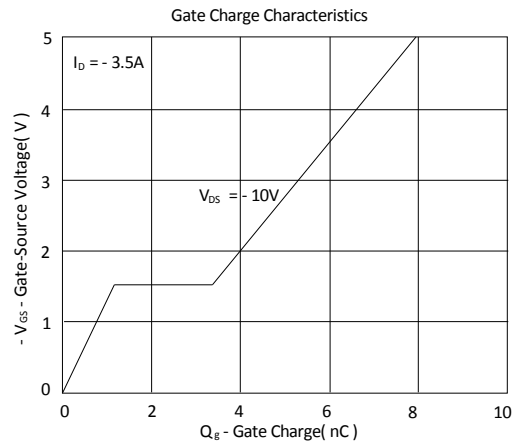
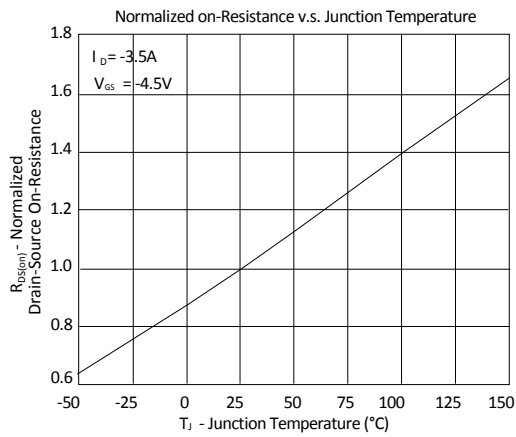
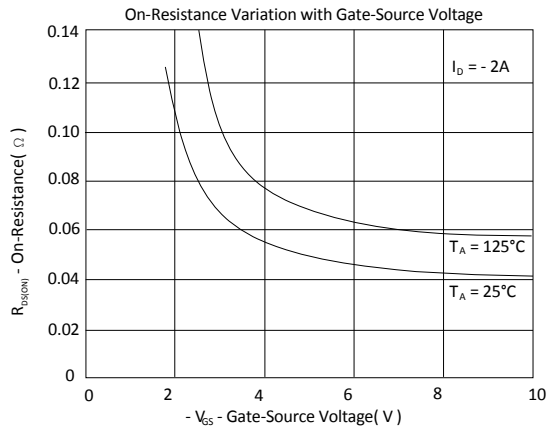
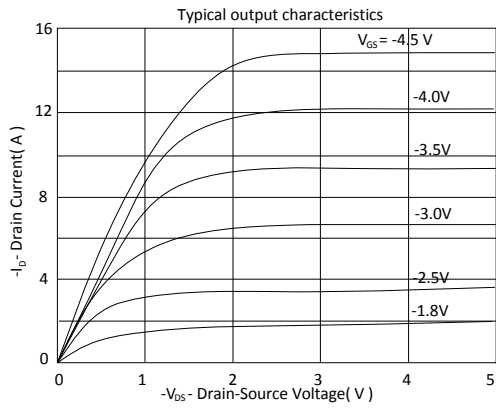
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\ \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

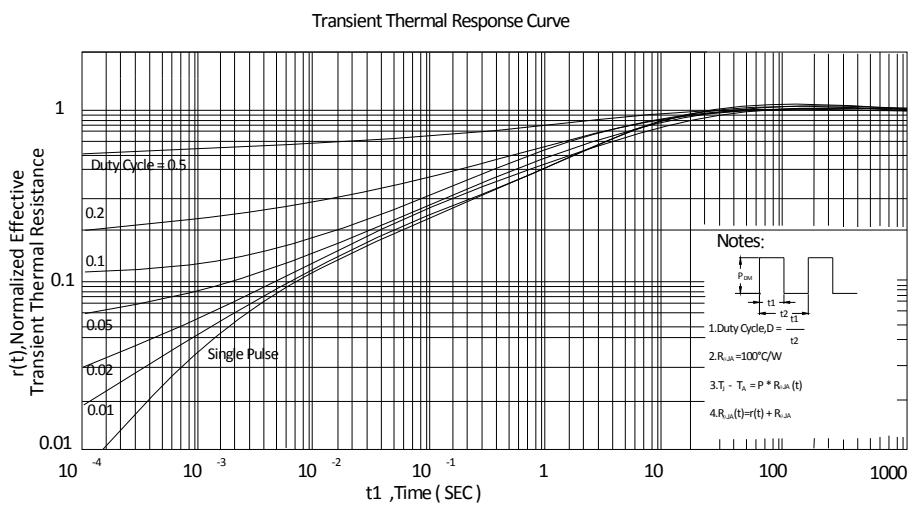
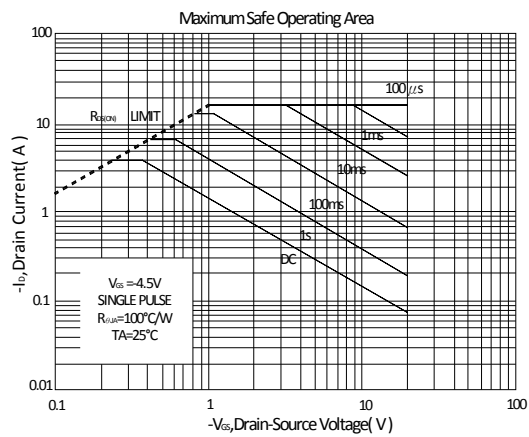
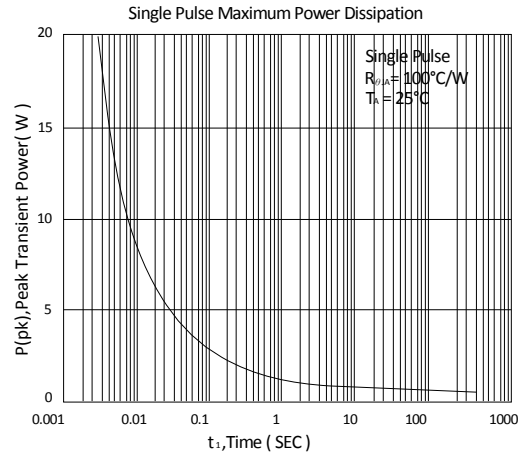
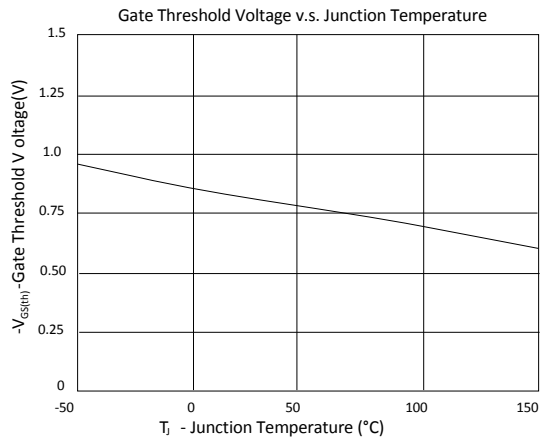
<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.



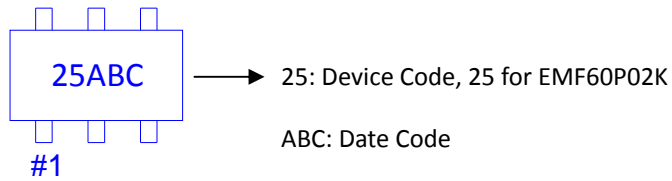
TYPICAL CHARACTERISTICS



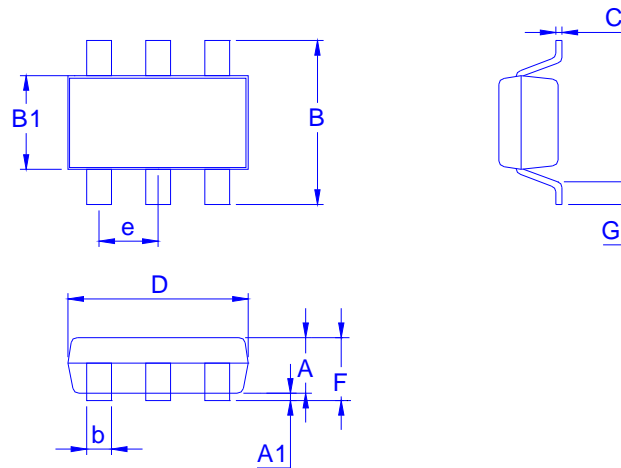


### Ordering & Marking Information:

Device Name: EMF60P02K for TSOP-6



### Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.70	0	2.50	1.50	0.30	0.08	2.70		0.75	0.30
Typ.			2.80	1.60	0.40		2.90	0.95		
Max.	1.00	0.10	3.10	1.70	0.50	0.20	3.10		1.10	0.60

### Footprint

