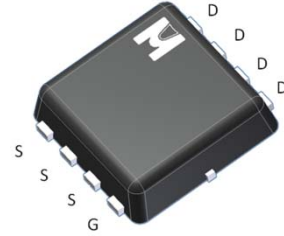
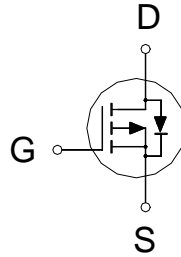


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-40V
$R_{DS(on)}$ (MAX.)	12.6m Ω
I_D	-22A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-22	A
	$T_C = 100\text{ }^\circ\text{C}$		-14	
Pulsed Drain Current ¹		I_{DM}	-88	
Avalanche Current		I_{AS}	-18	
Avalanche Energy	$L = 0.1\text{mH}$, $I_D = -18\text{A}$, $R_G = 25\text{ }\Omega$	E_{AS}	16.2	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	8.1	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	2.5	W
	$T_A = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		T_{j} , T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.8	-3.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -30V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-22			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -12A$		11.3	12.6	m Ω
		$V_{GS} = -5V, I_D = -9A$		18	23	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -12A$		28		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -20V, f = 1MHz$		3452		pF
Output Capacitance	C_{oss}			336		
Reverse Transfer Capacitance	C_{rss}			293		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		4.0		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -10V, V_{GS} = -10V,$ $I_D = -12A$		50		nC
Gate-Source Charge ^{1,2}	Q_{gs}			8		
Gate-Drain Charge ^{1,2}	Q_{gd}			11		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		15		nS
Rise Time ^{1,2}	t_r			28		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			32		
Fall Time ^{1,2}	t_f			26		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				-5	A
Pulsed Current ³	I_{SM}				-20	
Forward Voltage ¹	V_{SD}	$I_F = I_S A, V_{GS} = 0V$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		40		nS
Reverse Recovery Charge	Q_{rr}			30		nC

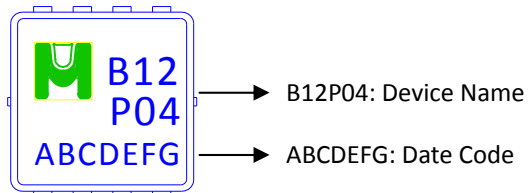
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

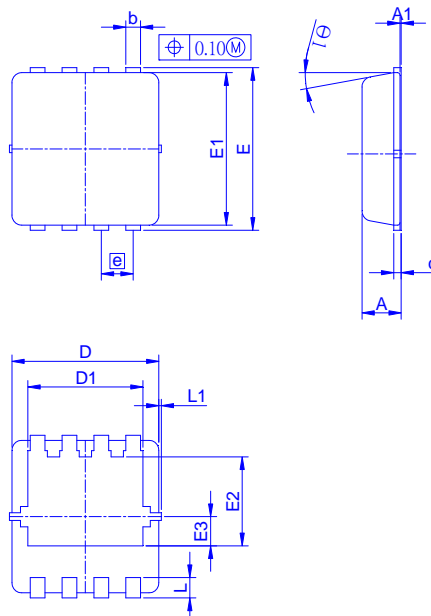
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB12P04V for EDFN 3 x 3



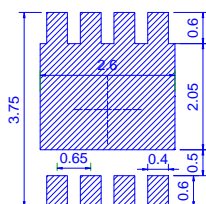
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads



TYPICAL CHARACTERISTICS

