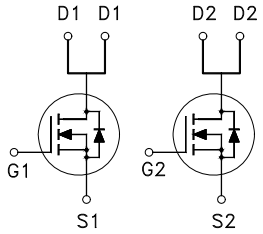
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	250V
$R_{DSON\ (MAX.)}$	1.7Ω
I_D	0.5A



Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	0.5	A
	T_A = 100 °C		0.3	
Pulsed Drain Current[1]		I_{DM}	2	
Power Dissipation	T_A = 25 °C	P_D	2	W
	T_A = 70 °C		1.3	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]62.5°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	250			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200V, V_{GS} = 0V			1	μA
		V_{DS} = 200V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	0.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 0.25A		1.35	1.7	mΩ
		V_{GS} = 5V, I_D = 0.15A		1.5	2.0	
Forward Transconductance[1]	g_{fs}	V_{DS} = 50V, I_D = 0.25A		2.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		680		pF
Output Capacitance	C_{oss}			15		
Reverse Transfer Capacitance	C_{rss}			13		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 200V, V_{GS} = 10V, I_D = 0.25A		17.8		nC
Gate-Source Charge[1,2]	Q_{gs}			2.2		
Gate-Drain Charge[1,2]	Q_{gd}			4.4		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 125V, I_D = 0.1A, V_{GS} = 10V, R_G = 6Ω		10		nS
Rise Time[1,2]	t_r			40		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			12		
Fall Time[1,2]	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				0.5	A
Pulsed Current[3]	I_{SM}				2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V

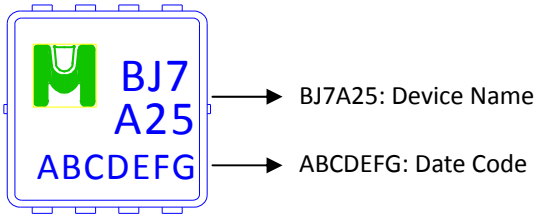
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

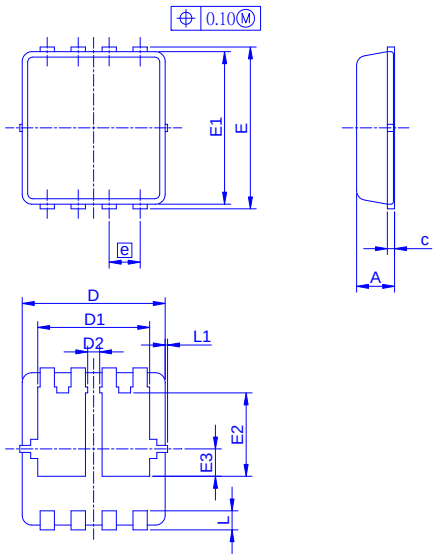
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBJ7A25V for EDFN 3 x 3



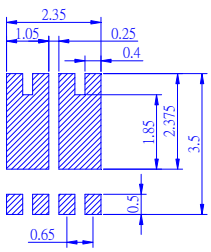
Outline Drawing



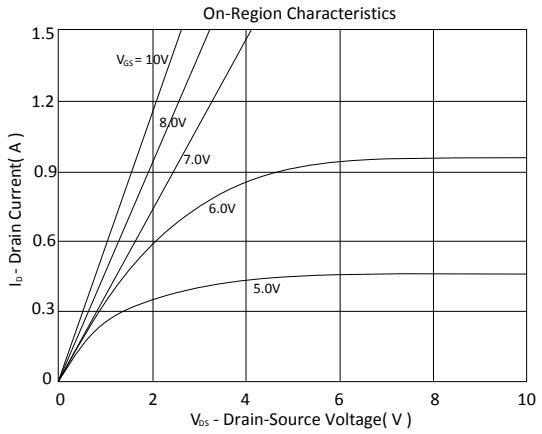
Dimension in mm

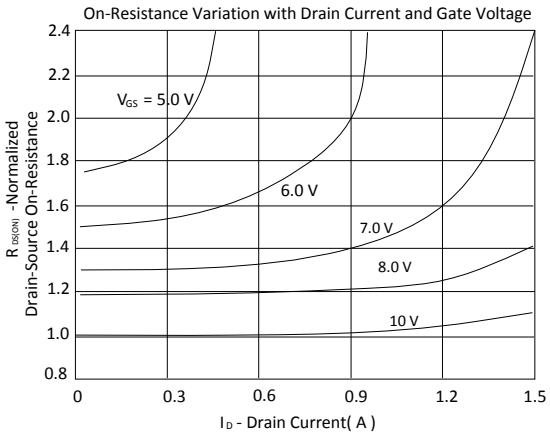
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

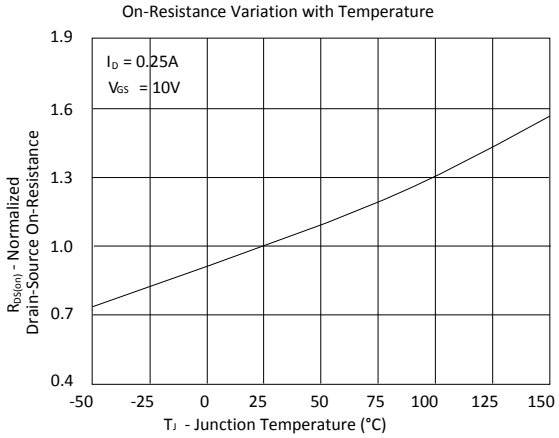
Recommended minimum pads

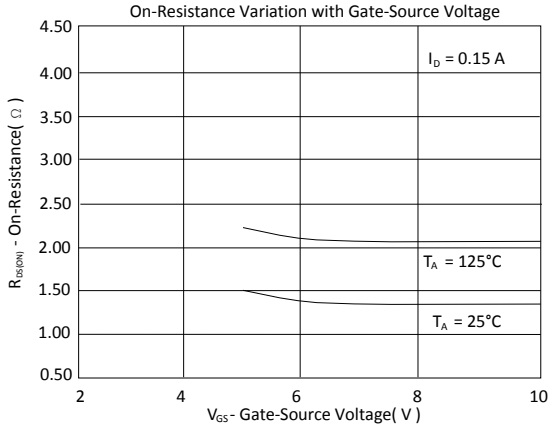


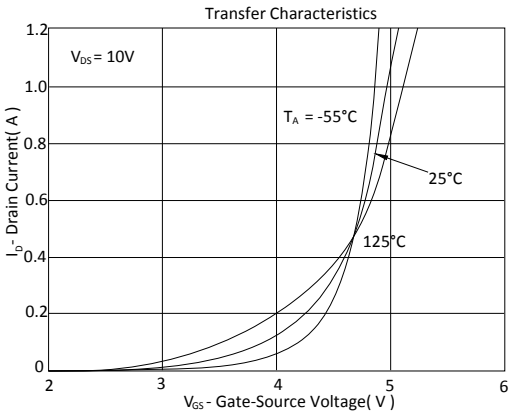
TYPICAL CHARACTERISTICS

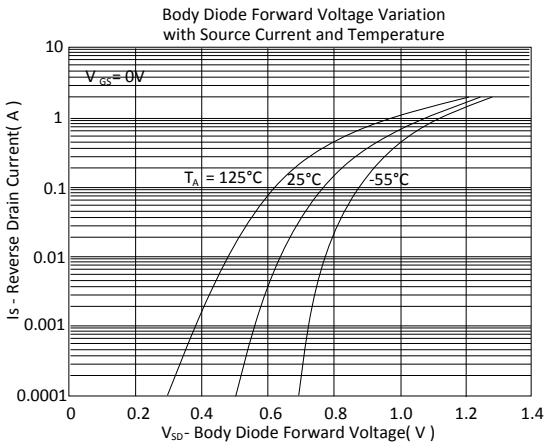


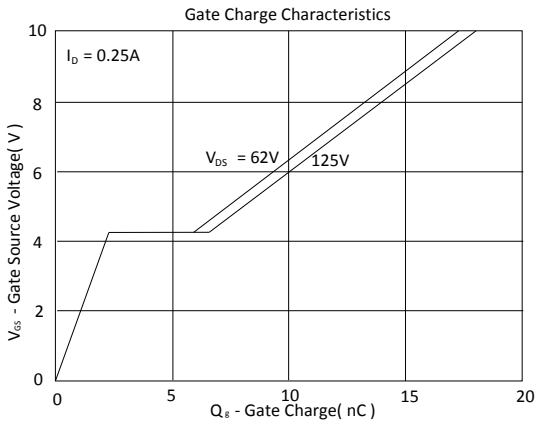


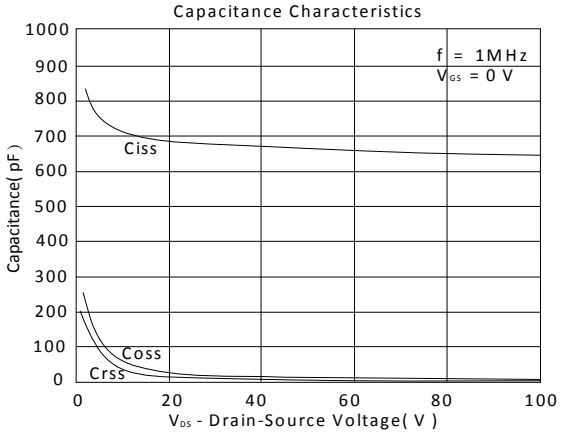


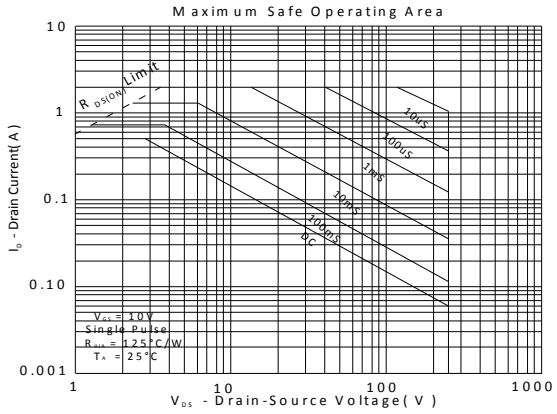


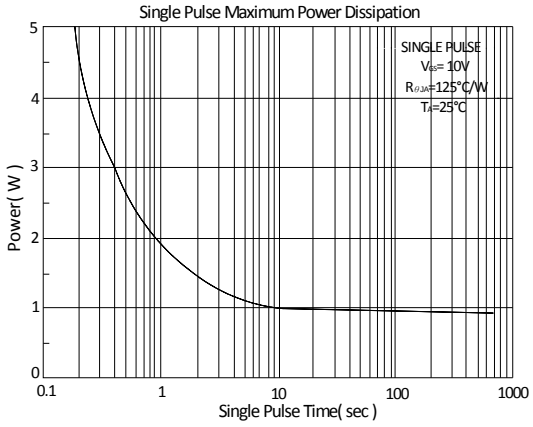


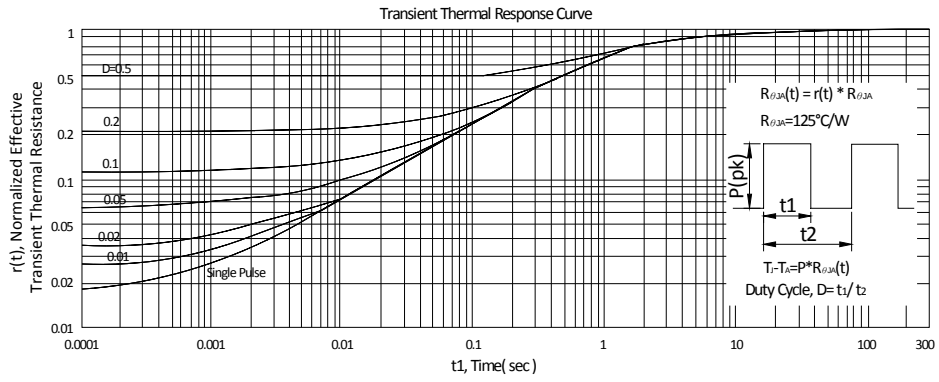



Gate Charge Characteristics
I_D = 0.25A
V_{DS} = 62V
125V
V_{GS} - Gate Source Voltage(V)
Q_g - Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS} - Drain-Source Voltage(V)


Maximum Safe Operating Area
$R_{DS(ON)}$ Limit
10μs
100μs
1ms
10ms
100ms
1s
10s
DC
V_{GS} = 10V
Single Pulse
$R_{\theta JA}$ = 125°C/W
T_A = 25°C
I_D - Drain Current(A)
V_{DS} - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
SINGLE PULSE
V_{GS}= 10V
$R_{\theta JA}$=125°C/W
T_A=25°C
Power(W)
Single Pulse Time(sec)


Transient Thermal Response Curve
D=0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
$R_{\theta JA}$=125°C/W
P(pk)
t1
t2
$T_J - T_A = P * R_{\theta JA}(t)$
Duty Cycle, D= t_1/ t_2
r(t), Normalized Effective Transient Thermal Resistance
t1, Time(sec)