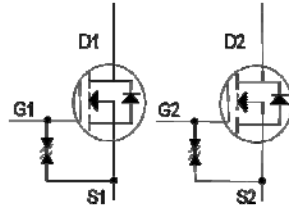


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DS(on)}$ (MAX.)	14m Ω
I_D	7A



Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	7	A
	$T_A = 70^\circ\text{C}$		4.5	
Pulsed Drain Current ¹		I_{DM}	28	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.27	W
	$T_A = 70^\circ\text{C}$		1.45	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		7.5	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		55	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³55 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.4	0.75	1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 4.5V$	7			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 7A$		12.3	14	m Ω
		$V_{GS} = 2.5V, I_D = 4A$		15	20	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 7A$		8		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$		1192		pF
Output Capacitance	C_{oss}			203		
Reverse Transfer Capacitance	C_{rss}			174		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.8		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 4A$		14.2		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$		15		nS
Rise Time ^{1,2}	t_r			18		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			35		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				2	A
Pulsed Current ³	I_{SM}				8	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

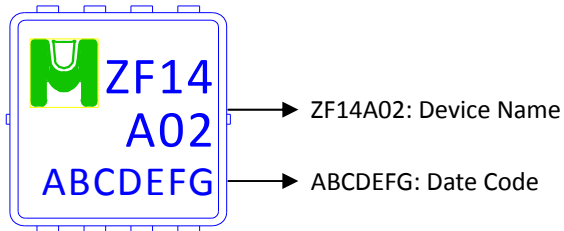
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

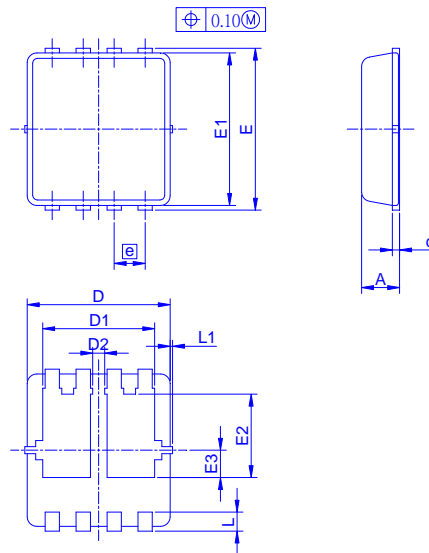
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZF14A02V for EDFN 3 x 3



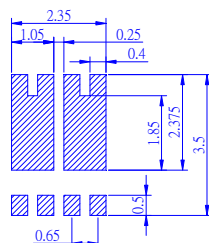
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	θ1
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

Recommended minimum pads





TYPICAL CHARACTERISTICS

