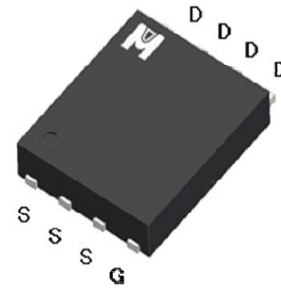


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DS(on)} (MAX.)	11.5mΩ
I _D	25A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	25	A
	T _C = 100 °C		20	
Pulsed Drain Current ¹		I _{DM}	100	
Avalanche Current		I _{AS}	30	
Avalanche Energy	L = 0.1mH, I _D =30A, R _G =25Ω	E _{AS}	45	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	22.5	
Power Dissipation	T _C = 25 °C	P _D	35	W
	T _C = 100 °C		14	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=15A, Rated V_{DS}=25V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		3.5	°C / W
Junction-to-Ambient ³	R _{θJA}		62	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62°C / W when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	25			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 15A$		9.7	11.5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$		17	23	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 15A$		15		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		762		pF
Output Capacitance	C_{oss}			150		
Reverse Transfer Capacitance	C_{rss}			130		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.0		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 15A$		15.2		nC
	$Q_g(V_{GS}=4.5V)$			10		
Gate-Source Charge ^{1,2}	Q_{gs}			2.1		
Gate-Drain Charge ^{1,2}	Q_{gd}			6.5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		8	
Rise Time ^{1,2}	t_r			6		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			18		
Fall Time ^{1,2}	t_f			3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				25	A
Pulsed Current ³	I_{SM}				100	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		18		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			100		A
Reverse Recovery Charge	Q_{rr}			10		nC

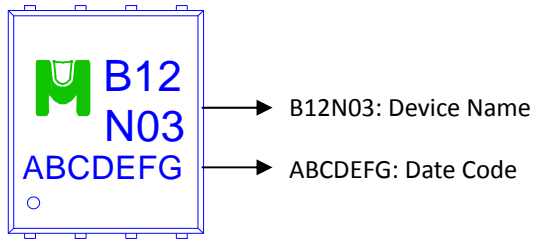
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

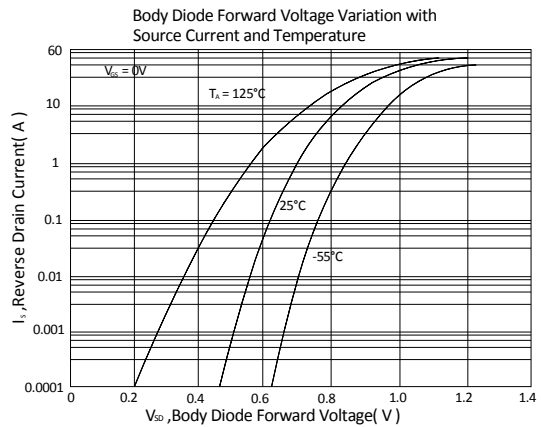
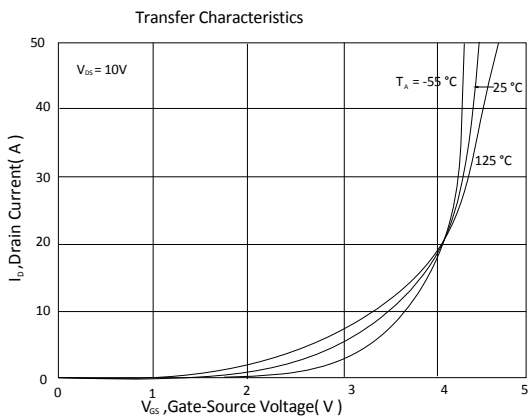
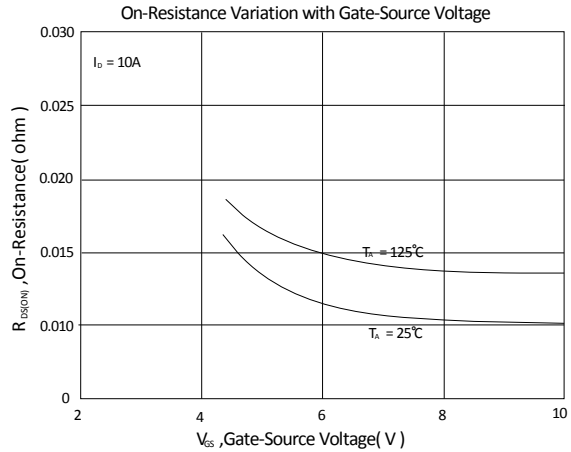
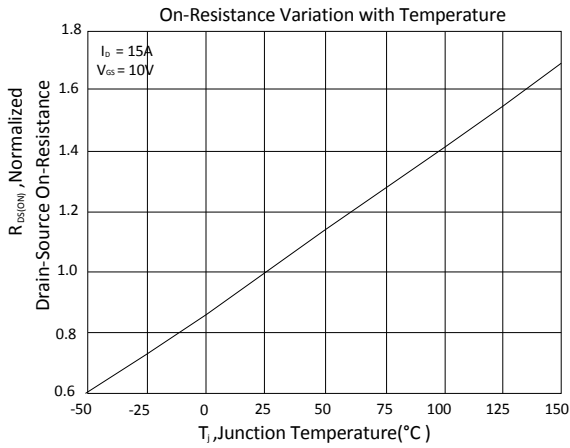
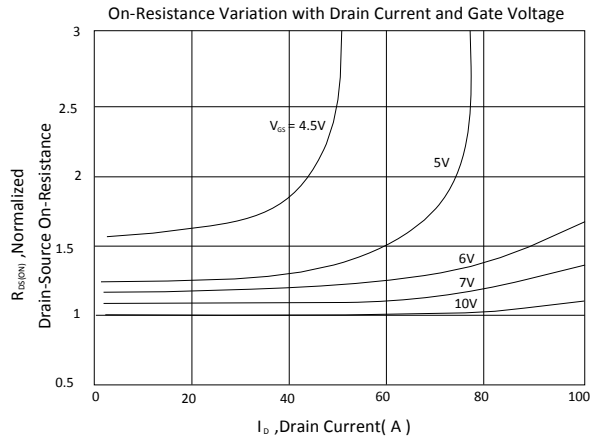
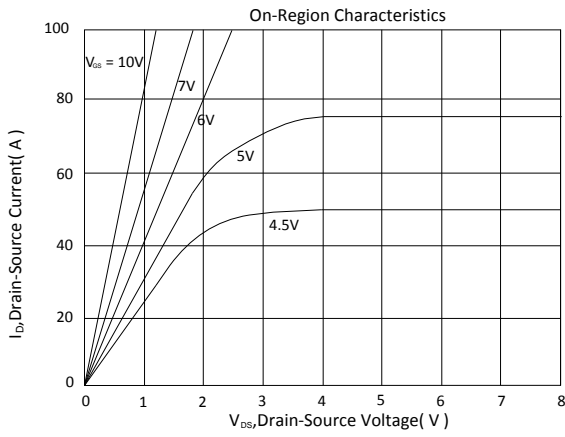
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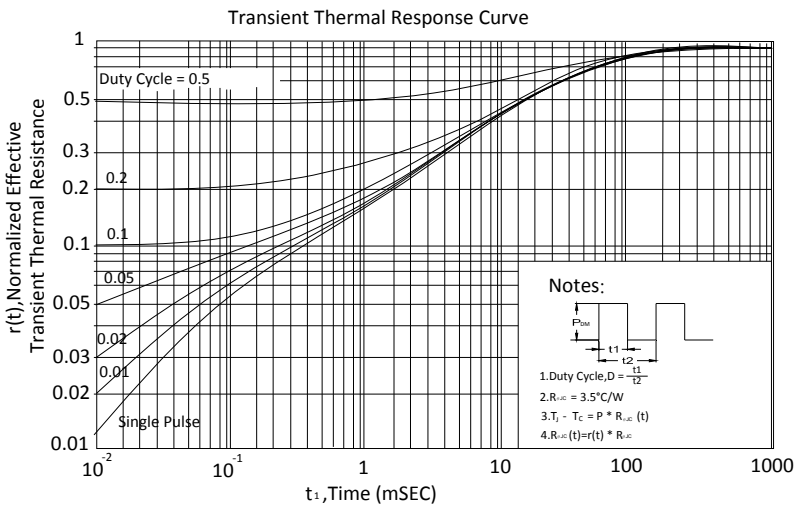
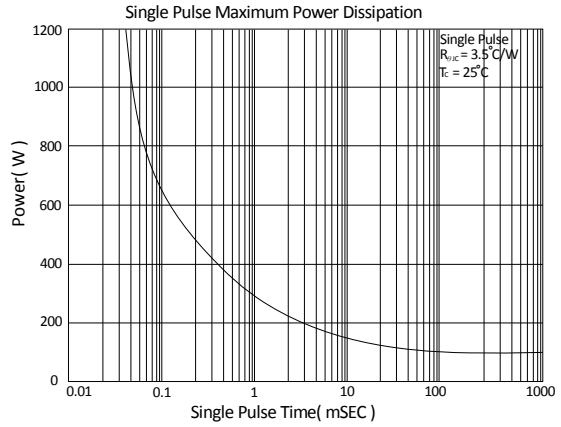
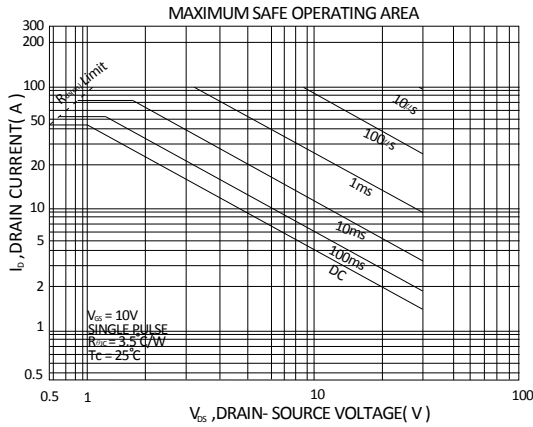
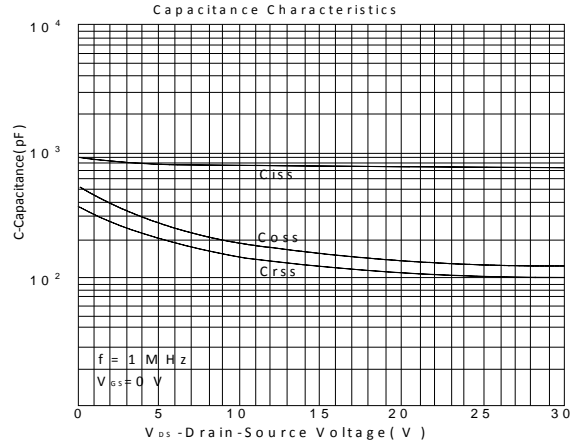
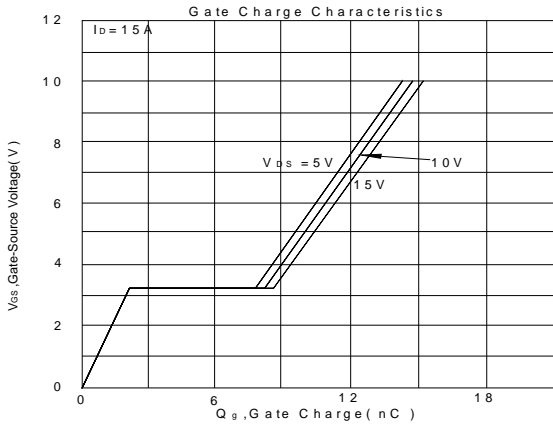
Device Name: EMB12N03H for EDFN 5 x 6





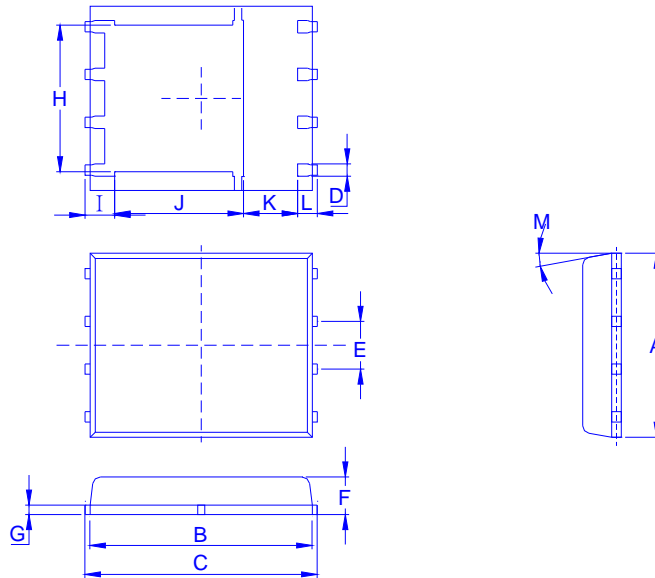
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

