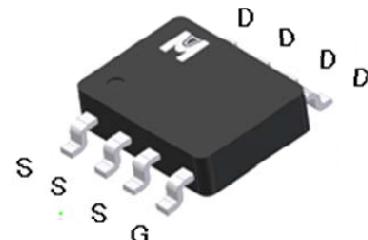


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DSON} (MAX.)	5mΩ
I _D	20A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	20	A
	T _A = 100 °C		13	
Pulsed Drain Current ¹		I _{DM}	80	
Avalanche Current		I _{AS}	20	
Avalanche Energy	L = 0.1mH, ID=20A, RG=25Ω	E _{AS}	20	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	10	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	25	50	°C / W
Junction-to-Ambient ³	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	20			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 20A$		3.9	5	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 15A$		7.1	9	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$		28		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1\text{MHz}$		2935		pF
Output Capacitance	C_{oss}			217		
Reverse Transfer Capacitance	C_{rss}			142		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		1.3		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V, I_D = 20A$		52		nC
	$Q_g(V_{GS}=4.5V)$			32		
Gate-Source Charge ^{1,2}	Q_{gs}			5.7		
Gate-Drain Charge ^{1,2}	Q_{gd}			7.2		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		25		ns
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			70		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{GS} = 0V$			10	A
Pulsed Current ³	I_{SM}				40	
Forward Voltage ¹	V_{SD}				1.2	
Reverse Recovery Time	t_{rr}			35		
Peak Reverse Recovery Current	$I_{RM(\text{REC})}$			50		
Reverse Recovery Charge	Q_{rr}			15		

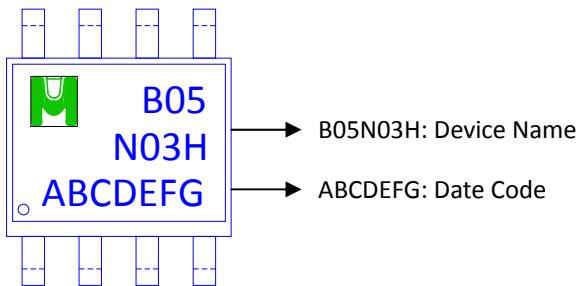
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

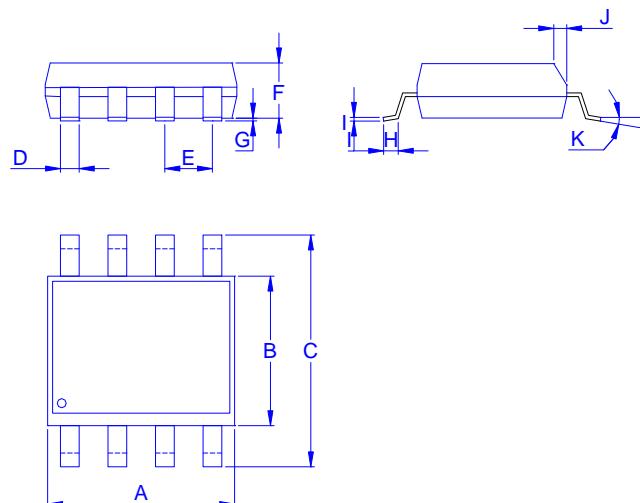
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB05N03GH for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

