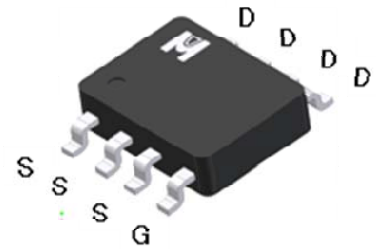
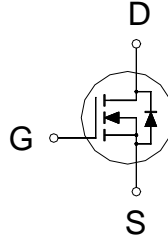


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	100V
$R_{DS(on)}$ (MAX.)	150m $\Omega$
$I_D$	4A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	4	A
	$T_A = 100\text{ }^\circ\text{C}$		2.8	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	16	
Avalanche Current		$I_{AS}$	4	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 4\text{A}, R_G = 25\Omega$	$E_{AS}$	0.8	mJ
Repetitive Avalanche Energy <sup>2</sup>	$L = 0.05\text{mH}$	$E_{AR}$	0.4	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.5	W
	$T_A = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>50 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	4			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2A$		125	150	m $\Omega$
		$V_{GS} = 5V, I_D = 1.5A$		168	225	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 2A$		8		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$		1030		pF
Output Capacitance	$C_{oss}$			50		
Reverse Transfer Capacitance	$C_{rss}$			42		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.2		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 80V, V_{GS} = 10V,$ $I_D = 2A$		23		nC
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			2.3		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			6.1		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 50V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		12		nS
Rise Time <sup>1,2</sup>	$t_r$			20		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			25		
Fall Time <sup>1,2</sup>	$t_f$			25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				2.3	A
Pulsed Current <sup>3</sup>	$I_{SM}$				9.2	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = I_S, di_F/dt = 100A / \mu S$		35		nS
Reverse Recovery Charge	$Q_{rr}$			65		nC

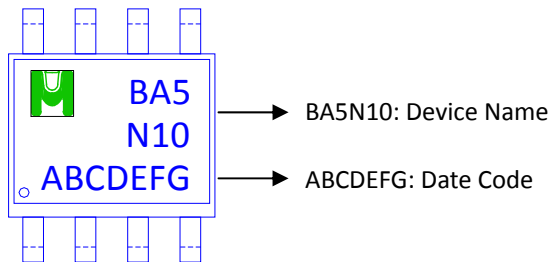
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

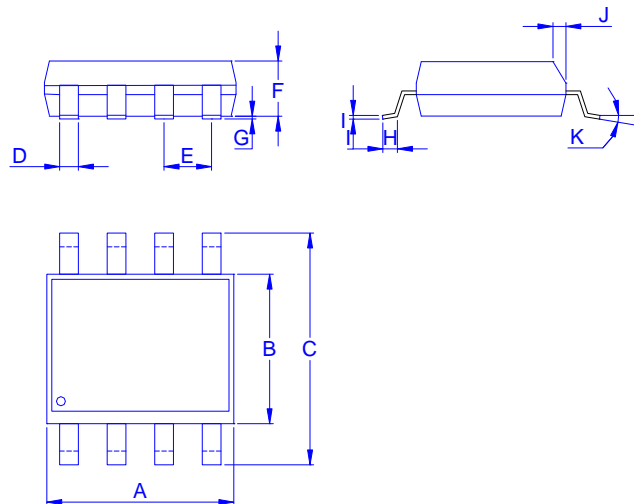
<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMBA5N10G for SOP-8



### Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



TYPICAL CHARACTERISTICS

