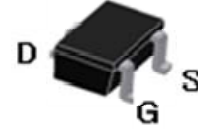
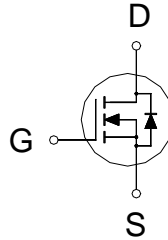


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	100V
$R_{DS(on)}$ (MAX.)	220m $\Omega$
$I_D$	1.4A



UIS 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	1.4	A
	$T_A = 100\text{ }^\circ\text{C}$		0.85	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	5.6	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	1.25	W
	$T_A = 100\text{ }^\circ\text{C}$		0.8	
Operating Junction & Storage Temperature Range		$T_j, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to- Ambient	$R_{\theta JA}$		100	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$



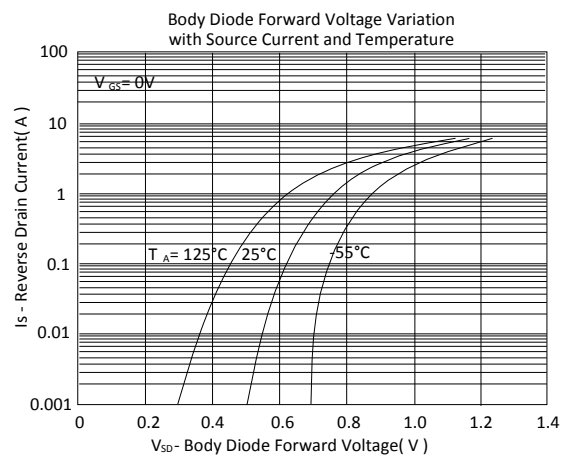
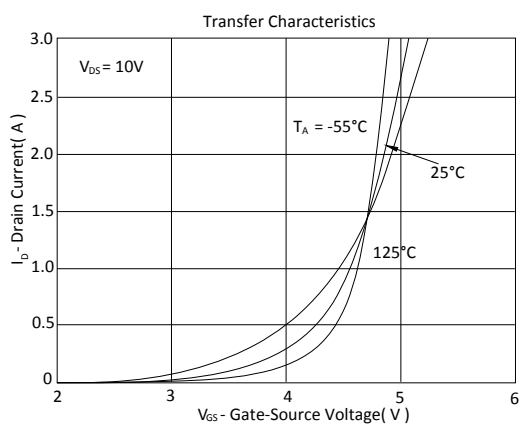
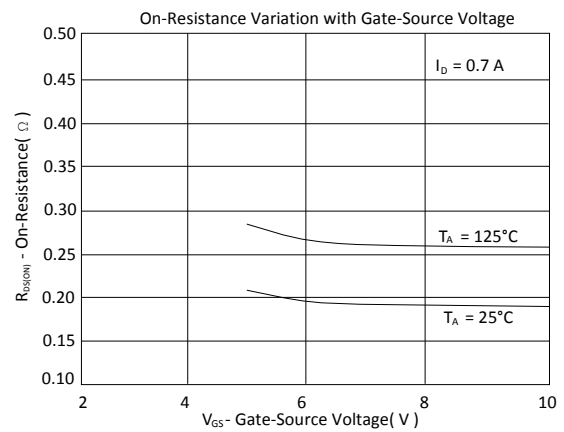
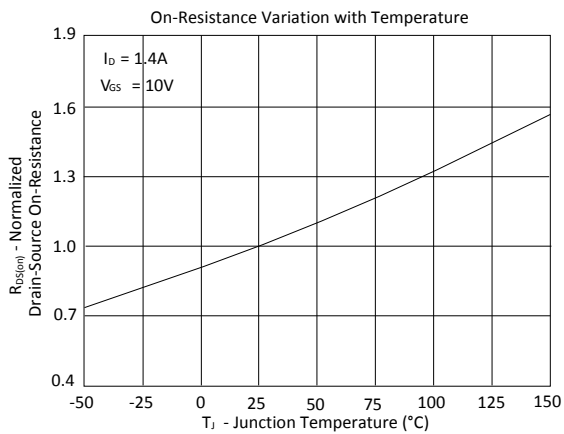
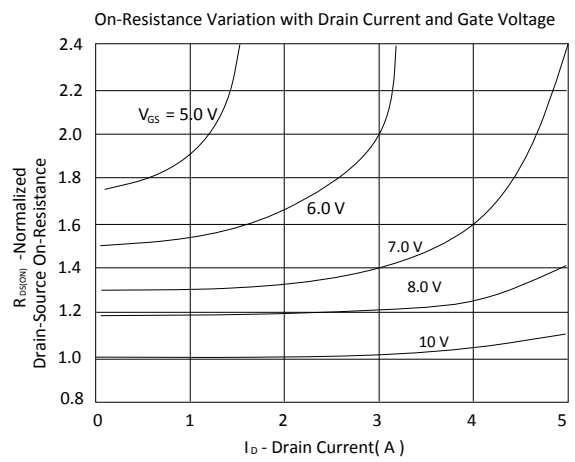
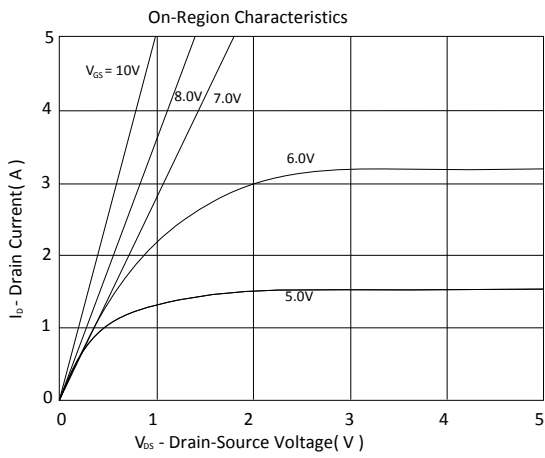
ELECTRICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

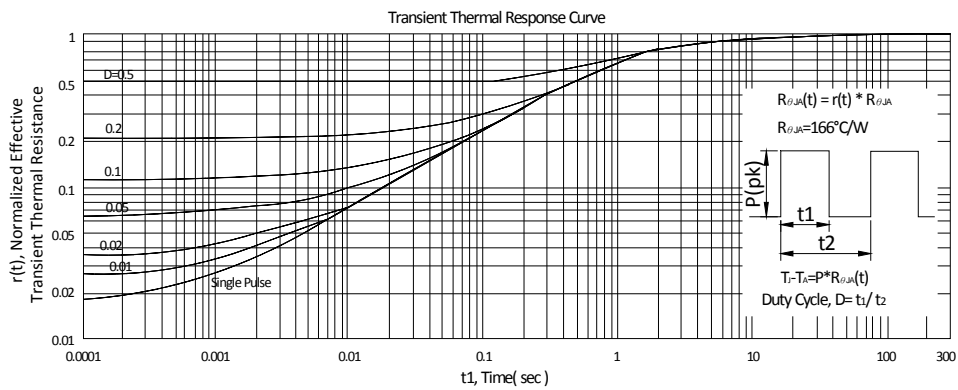
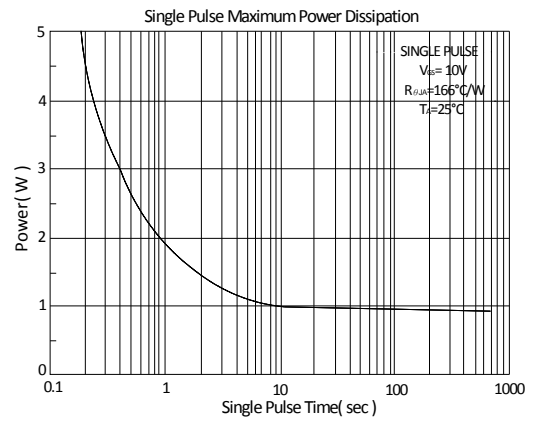
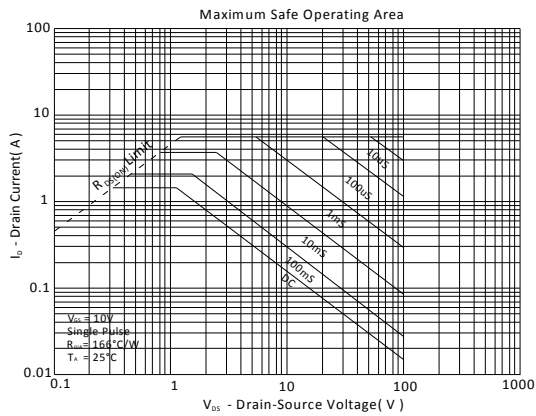
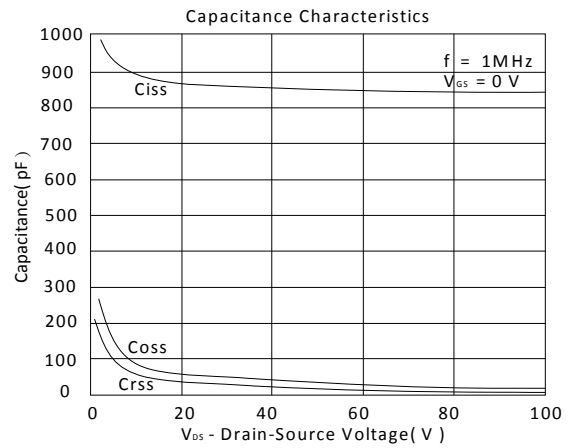
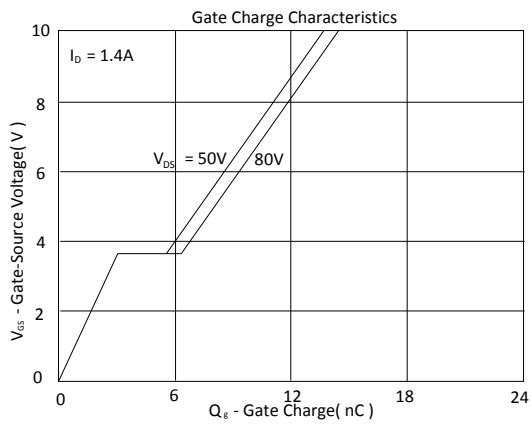
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	1.4			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 1.4A$		185	220	$m\Omega$
		$V_{GS} = 5V, I_D = 0.5A$		205	250	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 1.4A$		4		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$		858		$pF$
Output Capacitance	$C_{oss}$			38		
Reverse Transfer Capacitance	$C_{rss}$			27		
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 1.4A$		14.3		nC
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			2.9		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			3.4		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		20		nS
Rise Time <sup>1,2</sup>	$t_r$			30		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			36		
Fall Time <sup>1,2</sup>	$t_f$			30		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				1.4	A
Pulsed Current <sup>3</sup>	$I_{SM}$				5.6	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	$t_{rr}$			50		nS
Reverse Recovery Charge	$Q_{rr}$			90		nC

<sup>1</sup>Pulse test : Pulse Width  $\leq 300\ \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

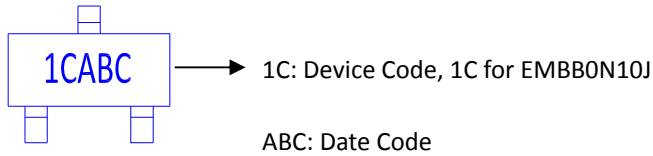




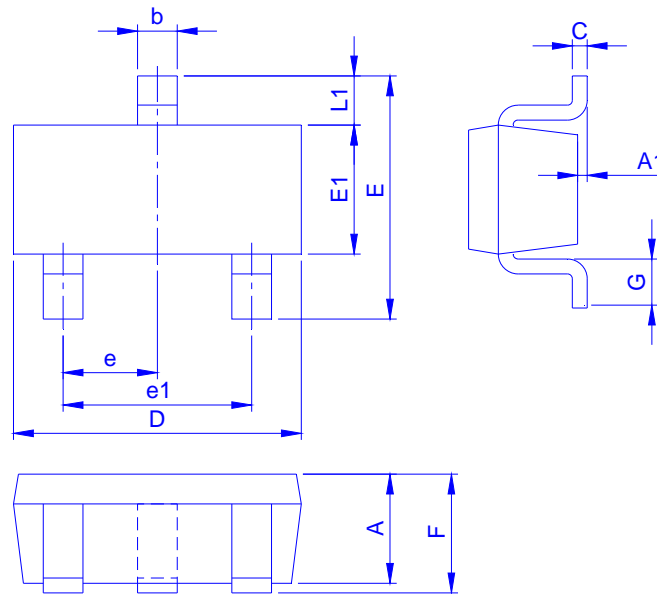


Ordering & Marking Information:

Device Name: EMBB0N10J for SOT-23



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.7	0		0.35	0.1	2.8	2.6	1.5	0.9		0.8	0.3	0.55
Typ.						2.9	2.8	1.6	0.95	1.9			
Max.	1.12	0.1		0.5	0.2	3	3	1.7	1		1.2	0.6	0.65

Footprint

