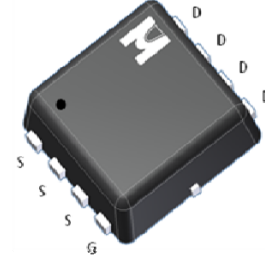
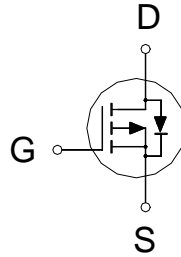


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	-40V
R <sub>DS(on)</sub> (MAX.)	39mΩ
I <sub>D</sub>	-12A



UIS, R<sub>g</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-12	A
	T <sub>A</sub> = 100 °C		-8	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	-48	
Avalanche Current		I <sub>AS</sub>	-10	
Avalanche Energy	L = 0.1mH, I <sub>D</sub> = -10A, R <sub>G</sub> = 25Ω	E <sub>AS</sub>	5	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	2.5	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5	W
	T <sub>A</sub> = 100 °C		1	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		6	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>50°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_C = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-2.3	-3.2	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -32V, V_{GS} = 0V$			-1	$\mu A$
		$V_{DS} = -30V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-12			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -8A$		34	39	m $\Omega$
		$V_{GS} = -7V, I_D = -6A$		50	70	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -8A$		11		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -20V, f = 1MHz$		1076		pF
Output Capacitance	$C_{oss}$			125		
Reverse Transfer Capacitance	$C_{rss}$			96		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		5.8		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = -10V, V_{GS} = -10V,$ $I_D = -8A$		16.5		nC
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			3.2		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			3.8		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		7		nS
Rise Time <sup>1,2</sup>	$t_r$			10		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			20		
Fall Time <sup>1,2</sup>	$t_f$			12		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				-2.3	A
Pulsed Current <sup>3</sup>	$I_{SM}$				-9.2	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S A, V_{GS} = 0V$			-1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = I_S, di_F/dt = 100A / \mu S$		15		nS
Reverse Recovery Charge	$Q_{rr}$			8		nC

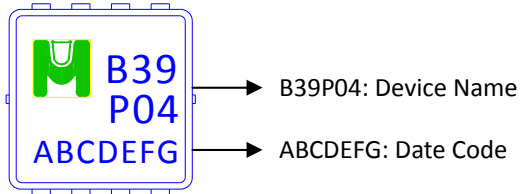
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

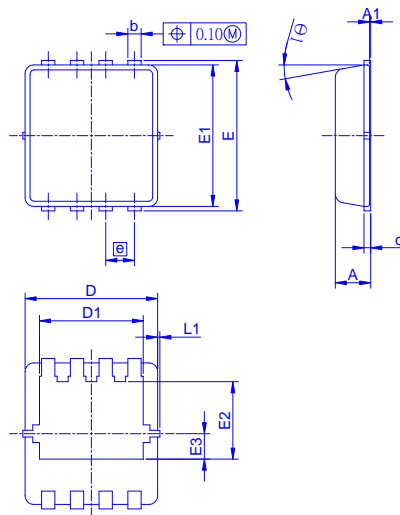
<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMB39P04V for EDFN 3 x 3



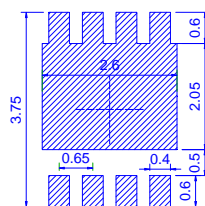
### Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	Θ1
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

### Recommended minimum pads





TYPICAL CHARACTERISTICS

