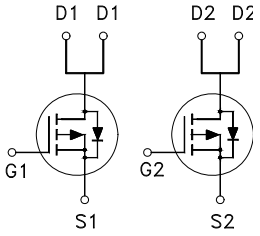
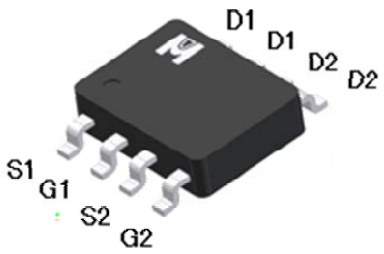
Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-100V
$R_{DSON\ (MAX.)}$	250mΩ
I_D	-2.5A





Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	-2.5	A
	T_A = 100 °C		-1.8	
Pulsed Drain Current[1]		I_{DM}	-10	
Power Dissipation	T_A = 25 °C	P_D	2	W
	T_A = 100 °C		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-2.0	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80V, V_{GS} = 0V			-1	μA
		V_{DS} = -70V, V_{GS} = 0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-2.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -1.5A		210	250	mΩ
		V_{GS} = -5V, I_D = -1A		280	375	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -1.5A		7		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -20V, f = 1MHz		2018		pF
Output Capacitance	C_{oss}			82		
Reverse Transfer Capacitance	C_{rss}			61		
Total Gate Charge[1,2]	Q_g	V_{DS} = -80V, V_{GS} = -10V, I_D = -1.5A		31		nC
Gate-Source Charge[1,2]	Q_{gs}			6.3		
Gate-Drain Charge[1,2]	Q_{gd}			4.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -50V, I_D = -1A, V_{GS} = -10V, R_{GS} = 6Ω		12		nS
Rise Time[1,2]	t_r			55		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			40		
Fall Time[1,2]	t_f			40		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_A = 25 °C)						
Continuous Current	I_S				-2.5	A
Pulsed Current[3]	I_{SM}				-10	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.3	V

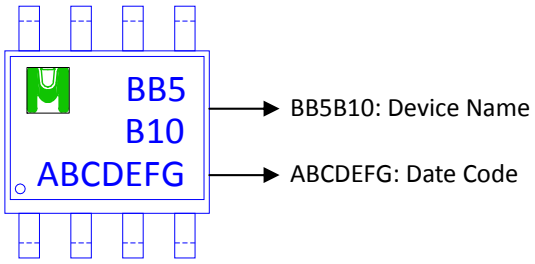
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

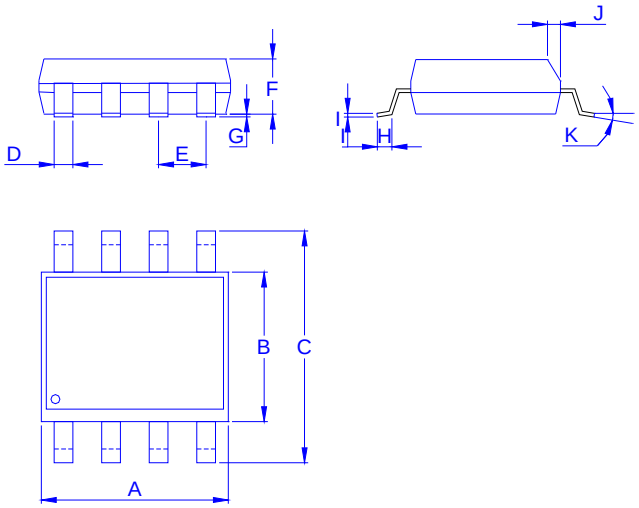
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBB5B10G for SOP-8



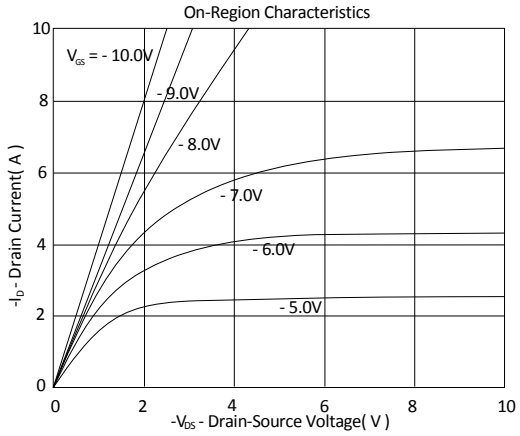
Outline Drawing

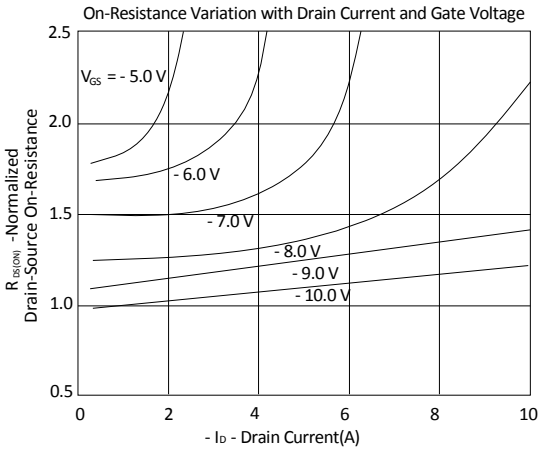


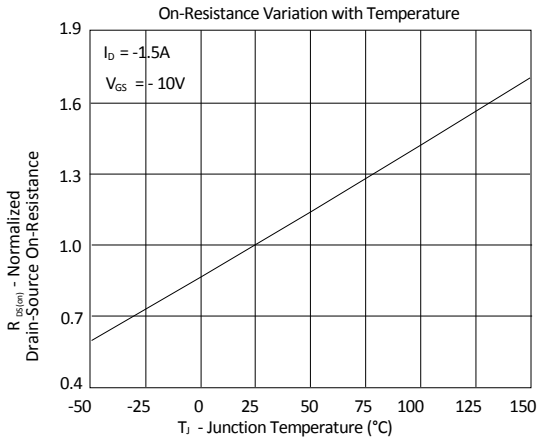
Dimension in mm

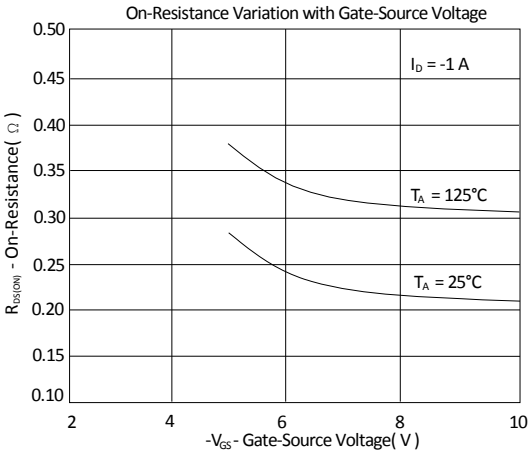
Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

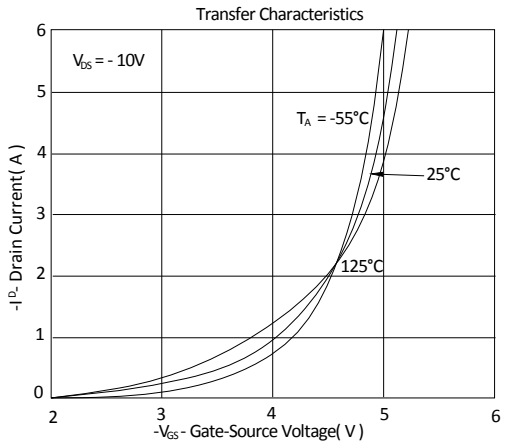
TYPICAL CHARACTERISTICS

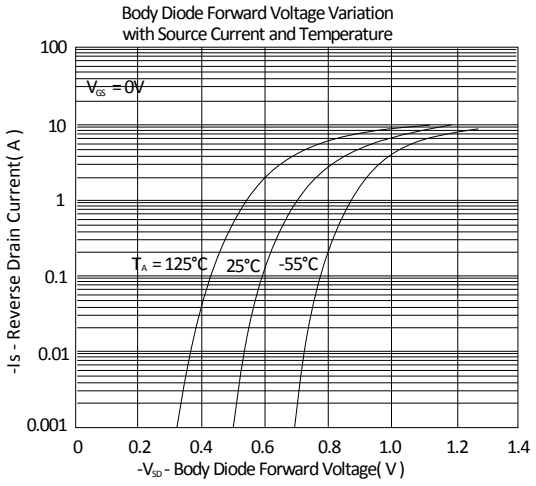




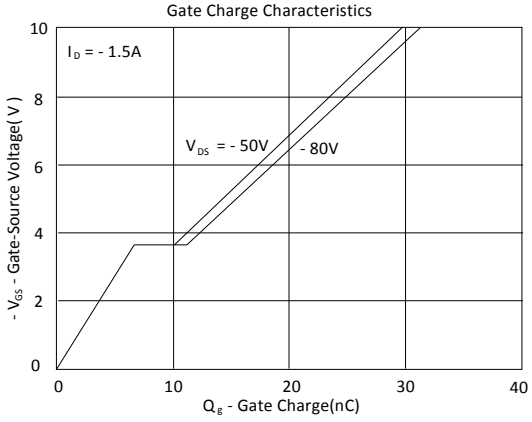




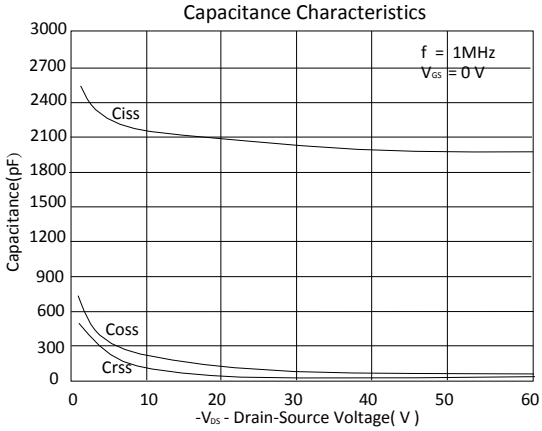




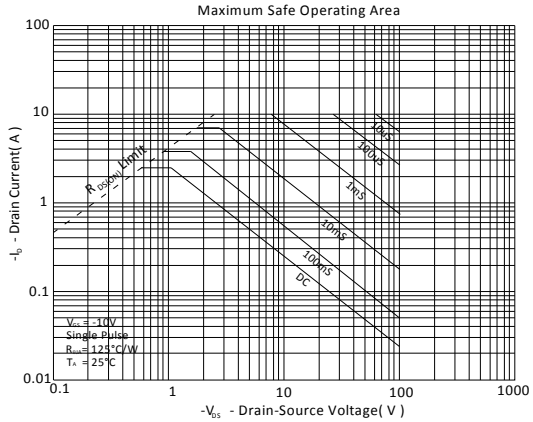
Gate Charge Characteristics



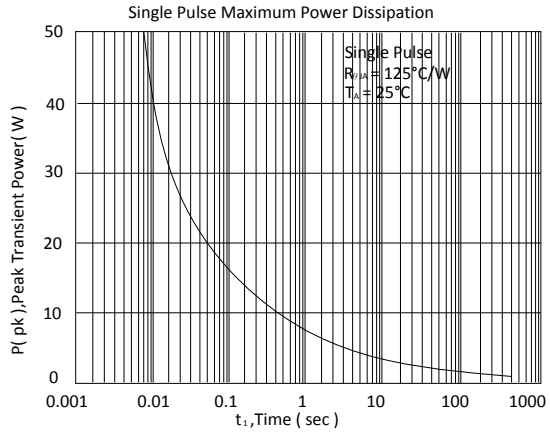
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve