杰力科技股份有限公司
Excelliance MOS Corporation

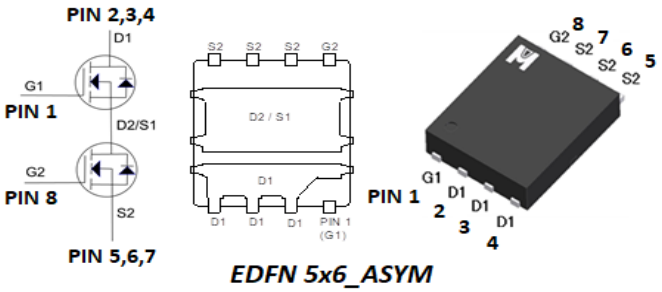
EMP19K03HPC

Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	Q1	Q2
BVDSS	30V	30V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	6.6mΩ	2.4mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	8.8mΩ	3.4mΩ
I_D @T_C=25°C	47.0A	93.0A
I_D @T_A=25°C	16.0A	27.0A

▪ Pin Description:



EDFN 5x6_ASYM

Dual N Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	47	93	A
	T_C = 100 °C		29	59	
Continuous Drain Current	T_A = 25 °C	I_D	16	27	
	T_A = 70 °C		13	22	
Pulsed Drain Current[1]		I_{DM}	77	158	
Avalanche Current		I_{AS}	34	65	
Avalanche Energy	L = 0.1mH	EAS	57.8	211.3	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	28.9	105.6	
Power Dissipation	T_C = 25 °C	P_D	25	35.7	W
	T_C = 100 °C		10	14.3	
Power Dissipation	T_A = 25 °C	P_D	3.1	3.1	W
	T_A = 70 °C		2	2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪ 100% UIS testing in condition of VD=15V, L=0.1mH, VG=10V, IL=21A, Rated VDS=30V N-CH_Q1

▪ 100% UIS testing in condition of VD=15V, L=0.1mH, VG=10V, IL=39A, Rated VDS=30V N-CH_Q2

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM		UNIT
				Q1	Q2	
Junction-to-Case		$R_{\theta JC}$		5	3.5	°C/W
Junction-to-Ambient[3]	t≦10s	$R_{\theta JA}$		40	40	
	Steady-State	$R_{\theta JA}$		65	65	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]65°C / W when mounted on a 1 in^2 pad of 2 oz copper.
[4]Guarantee by Engineering test

▪ **Q1_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	uA
		V_{DS} =30V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	47			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		5.5	6.6	mΩ
		V_{GS} = 4.5V, I_D = 20A		7	8.8	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		48		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		1033		pF
Output Capacitance[5]	C_{oss}			155		
Reverse Transfer Capacitance[5]	C_{rss}			99		
Gate Resistance[4,5]	R_g	f = 1MHz		0.6	1.2	Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 20A		19.0		nC
	Q_g(V_{GS}=4.5V)			9.7		
Gate-Source Charge[1,2,5]	Q_{gs}			2.6		
Gate-Drain Charge[1,2,5]	Q_{gd}			4.2		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		6.4		nS
Rise Time[1,2,5]	t_r			11.1		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			14.6		
Fall Time[1,2,5]	t_f			1.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				47	A
Pulsed Current[3]	I_{SM}				77	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 400A / uS		7.8		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.24		A
Reverse Recovery Charge[5]	Q_{rr}			9.2		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪Q1_TYPICAL CHARACTERISTICS

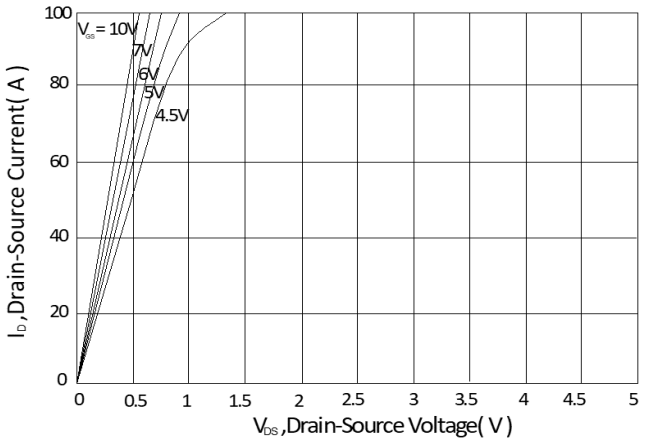


Fig.1 Typical Output Characteristics

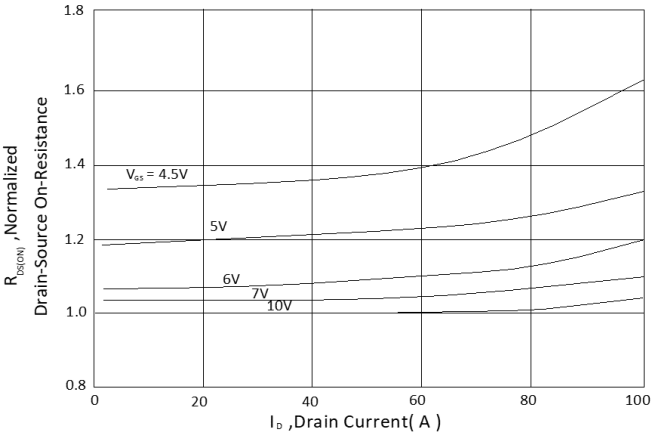


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

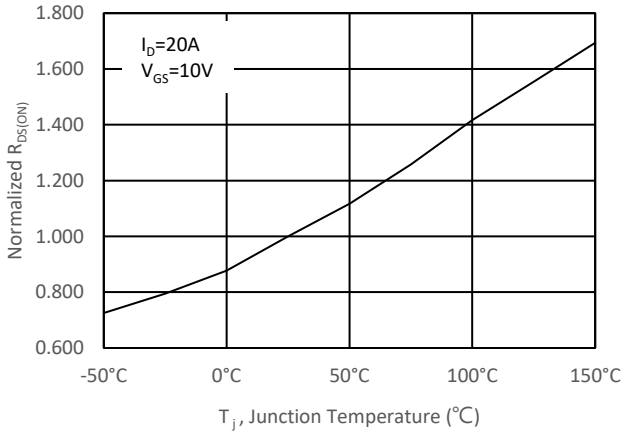


Fig.3 Normalized On-Resistance v.s. Junction Temperature

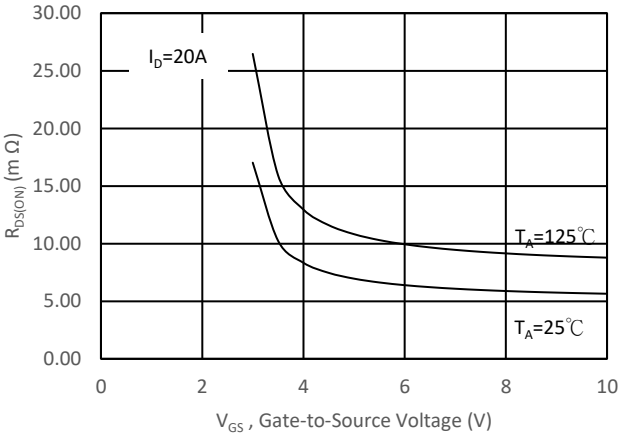


Fig.4 On-Resistance v.s. Gate Voltage

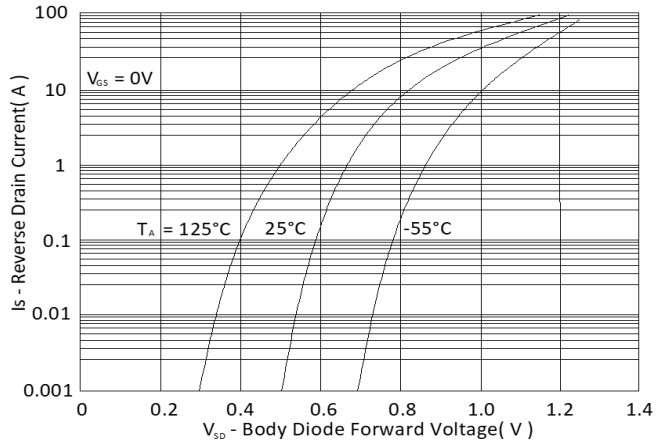


Fig.5 Forward Characteristic of Reverse Diode

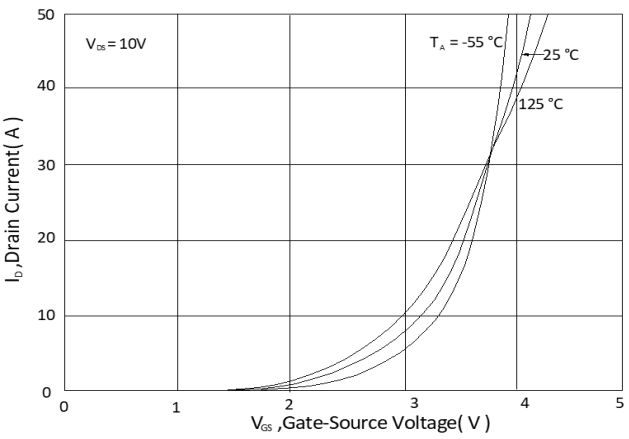


Fig.6 Transfer Characteristics

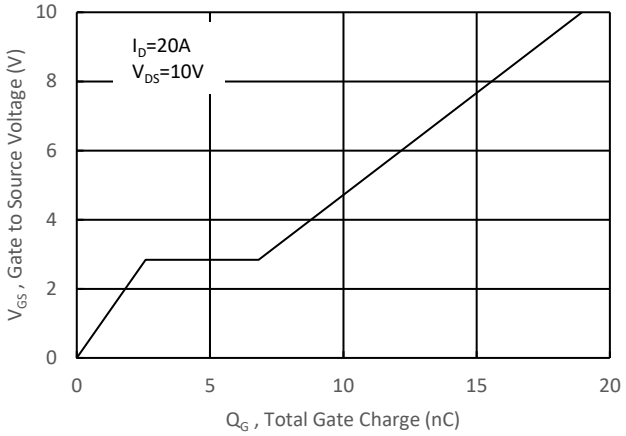


Fig.7 Gate Charge Characteristics

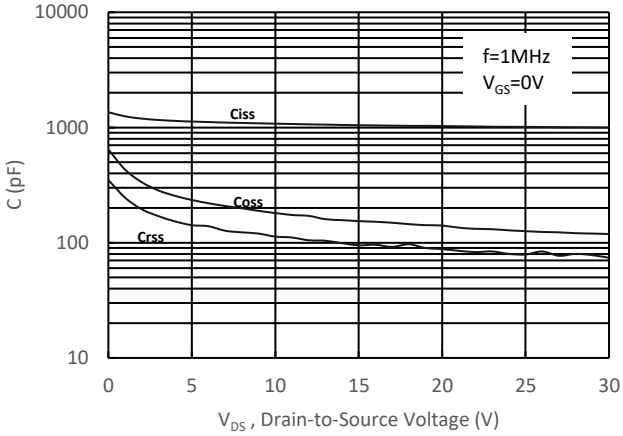


Fig.8 Typical Capacitance Characteristics

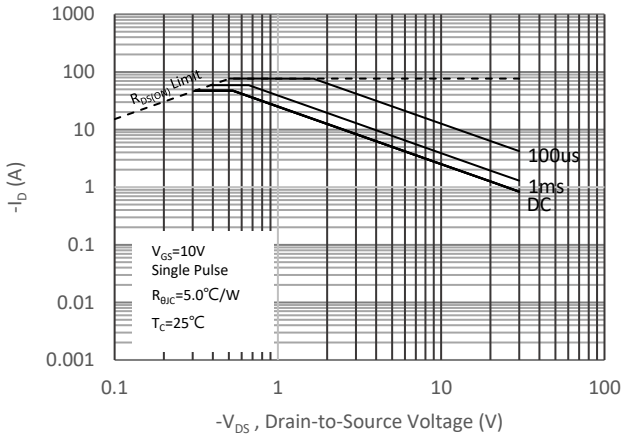


Fig 9. Maximum Safe Operating Area

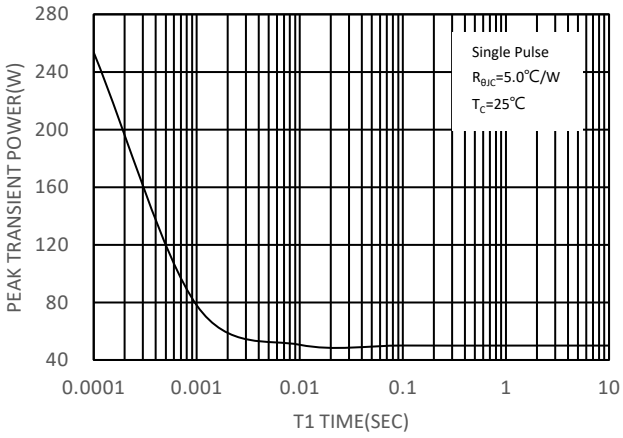


Fig 10. Single Pulse Maximum Power Dissipation

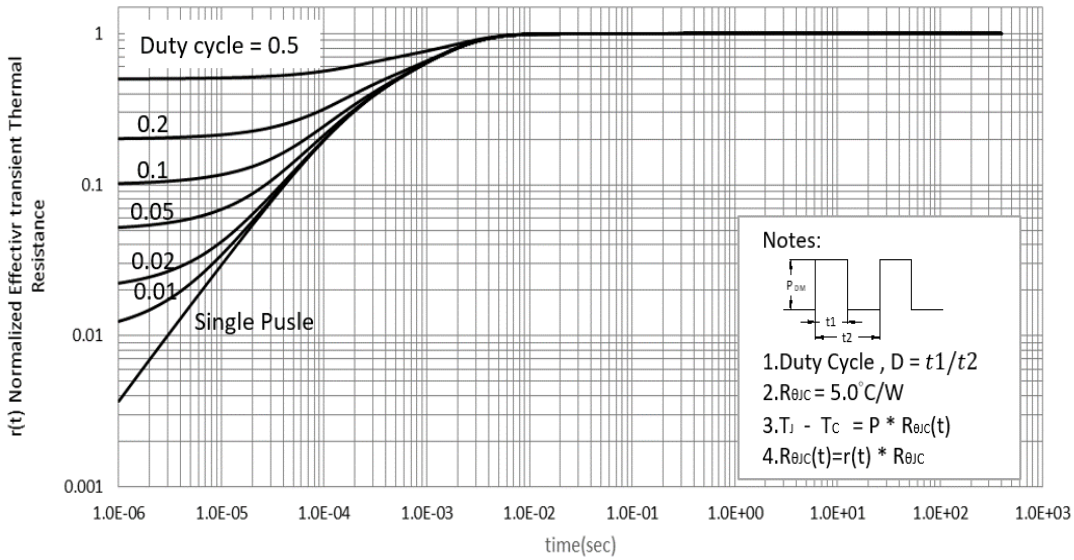


Fig 11. Effective Transient Thermal Impedance

▪ **Q2_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	30			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	uA
		V_{DS} =30V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	93			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		1.9	2.4	mΩ
		V_{GS} = 4.5V, I_D = 20A		2.6	3.4	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		72		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		3029		pF
Output Capacitance[5]	C_{oss}			421		
Reverse Transfer Capacitance[5]	C_{rss}			299		
Gate Resistance[4,5]	R_g	f = 1MHz		1.4	2.8	Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 20A		63.9		nC
	Q_g(V_{GS}=4.5V)			32.9		
Gate-Source Charge[1,2,5]	Q_{gs}			6.0		
Gate-Drain Charge[1,2,5]	Q_{gd}			14.7		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		10.0		nS
Rise Time[1,2,5]	t_r			15.4		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			14.6		
Fall Time[1,2,5]	t_f			1.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				93	A
Pulsed Current[3]	I_{SM}				158	
Forward Voltage[1,4]	V_{SD}	I_F = 20A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 20A, dI_F/dt = 400A / uS		17.8		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.80		A
Reverse Recovery Charge[5]	Q_{rr}			26.3		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

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▪Q2_TYPICAL CHARACTERISTICS

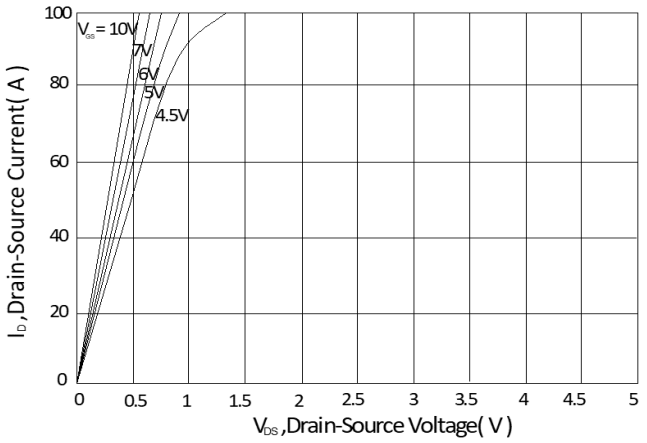


Fig.1 Typical Output Characteristics

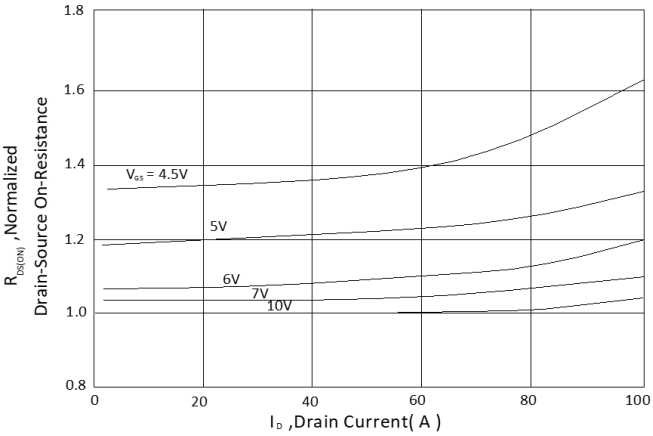


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

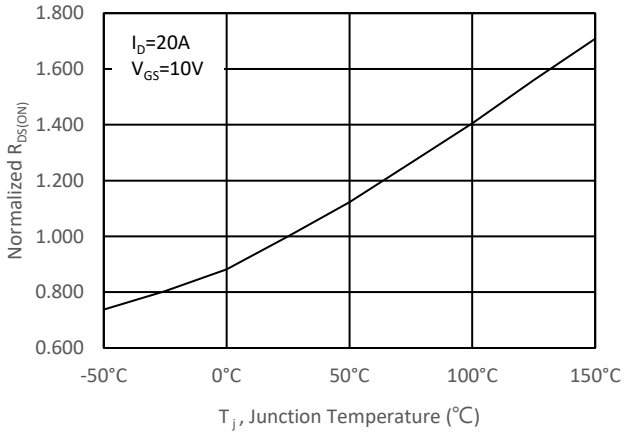


Fig.3 Normalized On-Resistance v.s. Junction Temperature

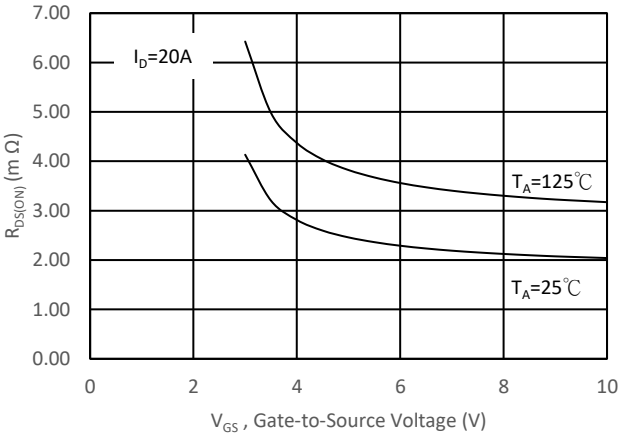


Fig.4 On-Resistance v.s. Gate Voltage

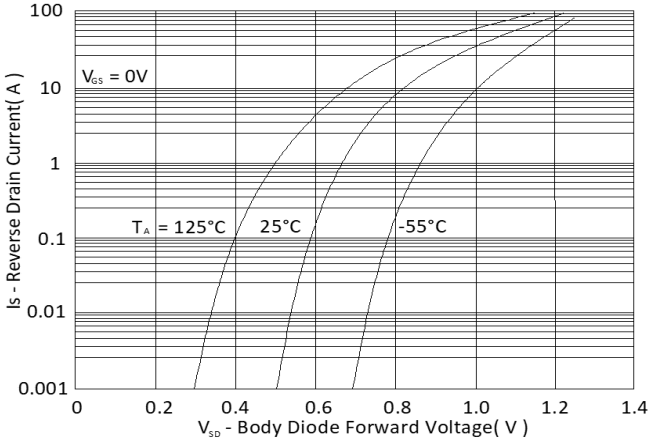


Fig.5 Forward Characteristic of Reverse Diode

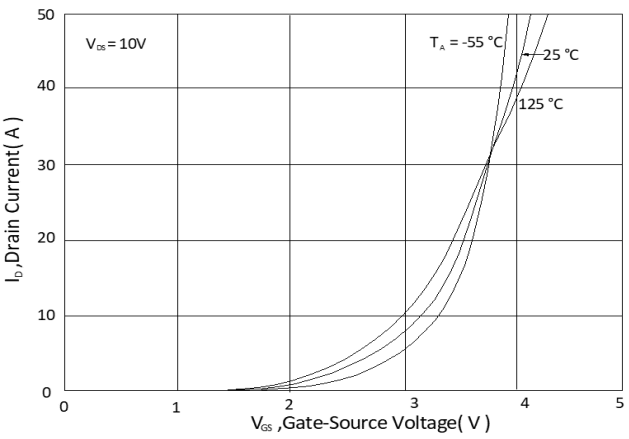


Fig.6 Transfer Characteristics

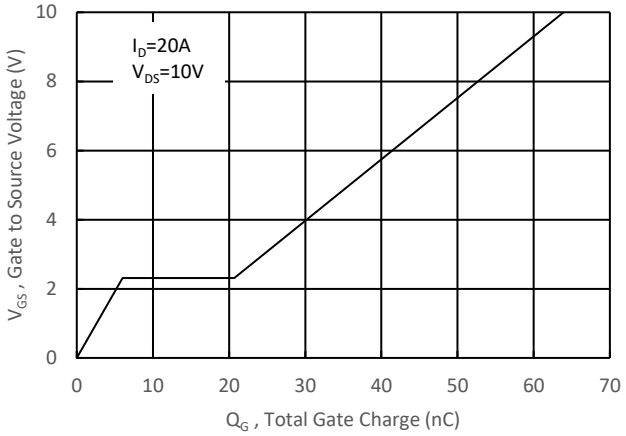


Fig.7 Gate Charge Characteristics

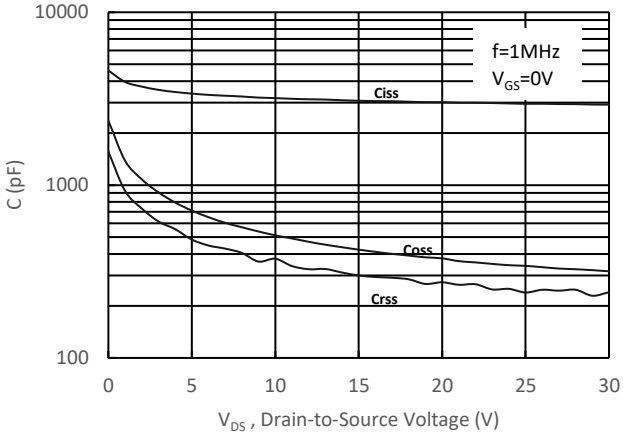


Fig.8 Typical Capacitance Characteristics

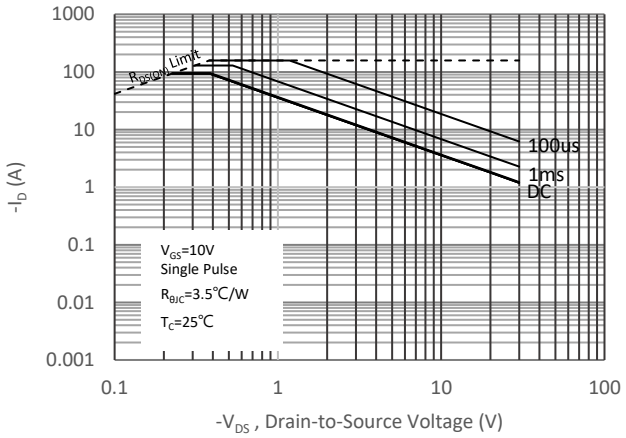


Fig 9. Maximum Safe Operating Area

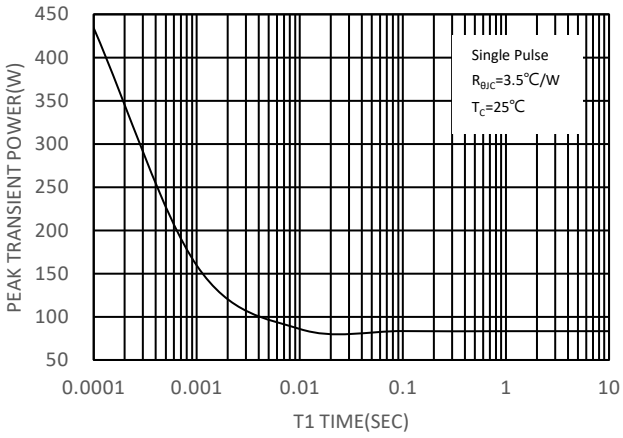


Fig 10. Single Pulse Maximum Power Dissipation

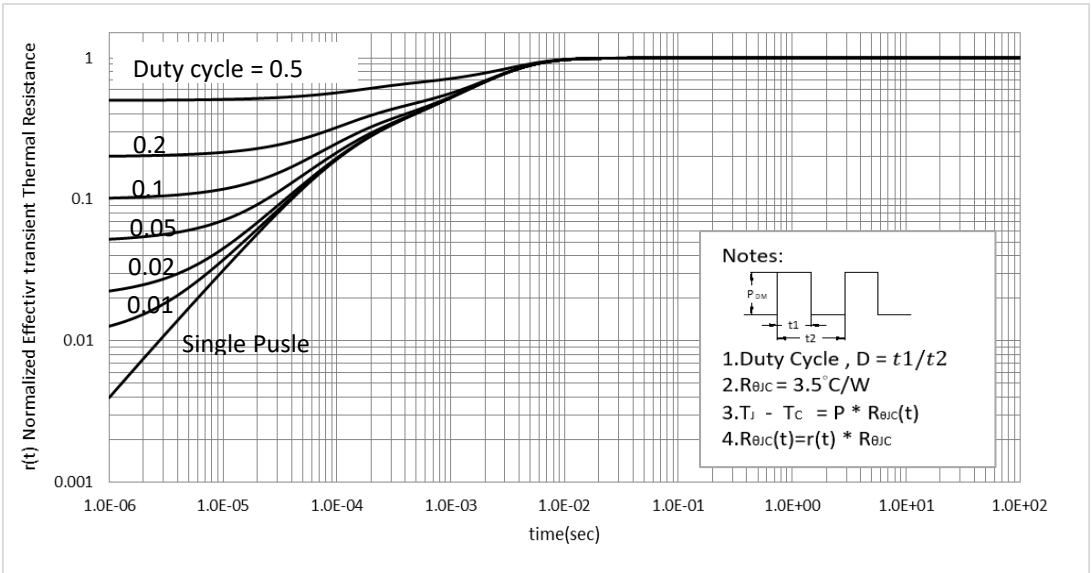
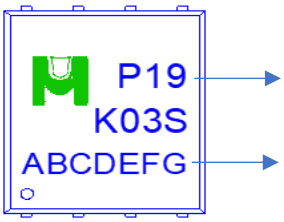


Fig 11. Effective Transient Thermal Impedance

Ordering & Marking Information:

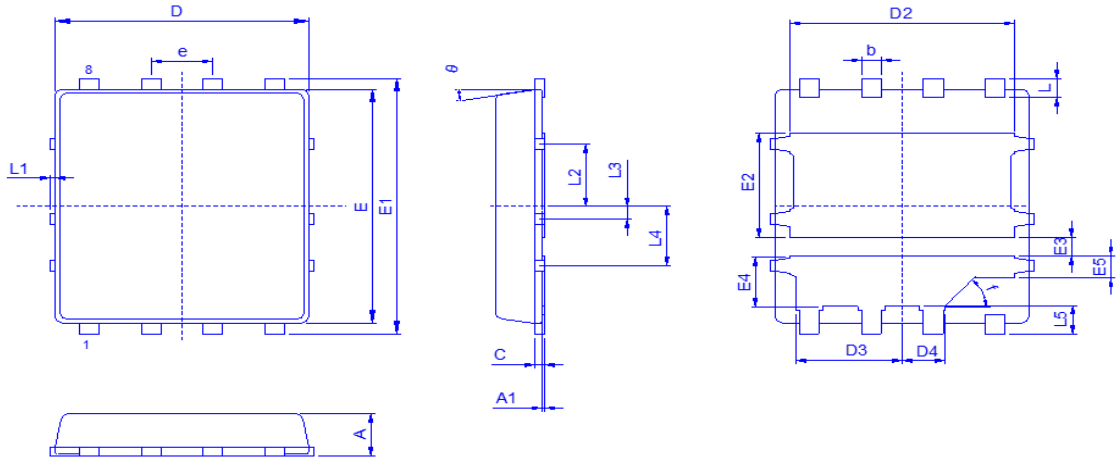
Device Name: EMP19K03HPC for Asymmetric Dual EDFN5X6 (EDFN 5x6_ASYM)



P19K03S: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

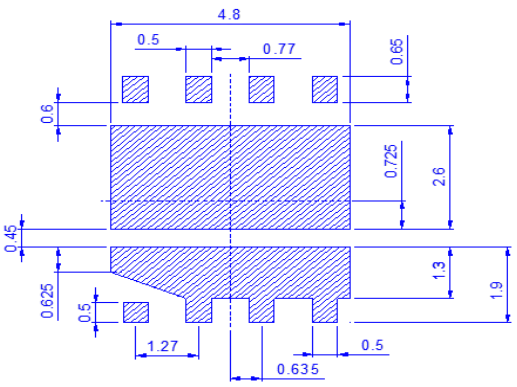
Outline Drawing



Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4
Min.	0.85	0	0.35	0.15	4.8	4.3	1.995	0.835	5.55	5.9	1.95	0.3	1.025
Typ.	0.9		0.4	0.2	5	4.5	2.105	0.885	5.55	6.05	2.1	0.45	1.175
Max.	1	0.05	0.48	0.28	5.2	4.7	2.255	1.3	5.85	6.2	2.5	0.6	1.325

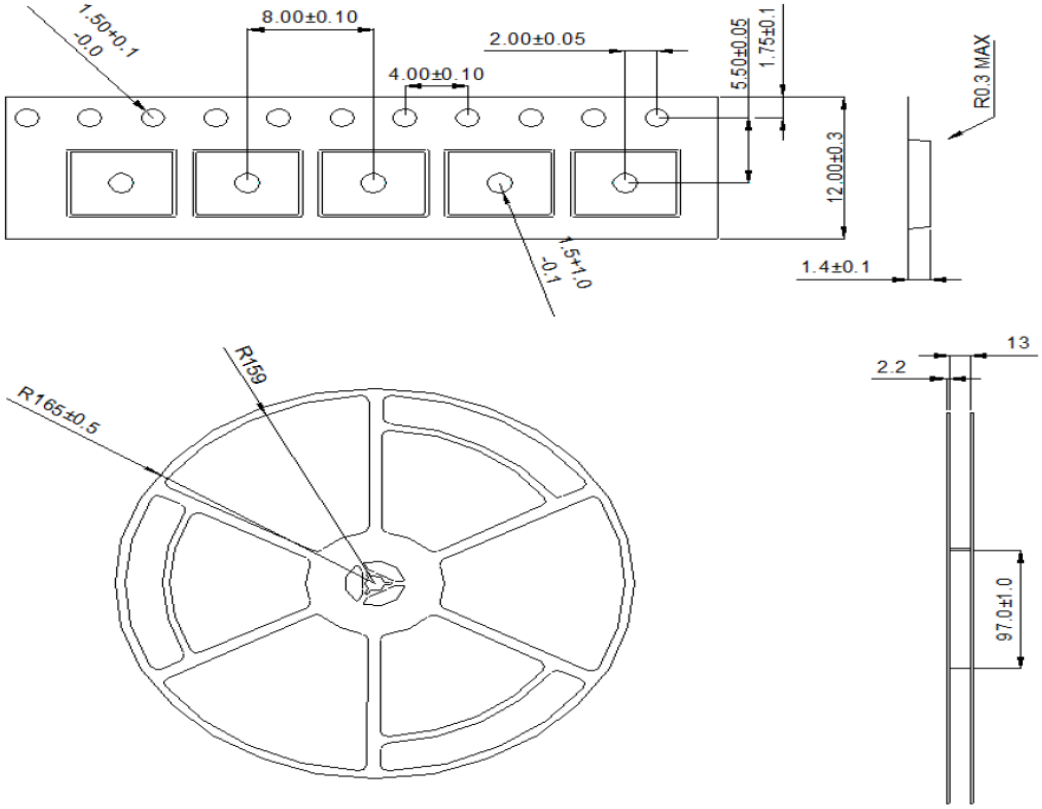
Dimension	E5	e	L	L1	L2	L3	L4	L5	F	θ
Min.	0.375		0.35	-	1	0.2	1.3	0.575		0°
Typ.	0.525	1.27	0.45		1.1	0.3	1.4	0.675	45°	
Max.	0.675		0.55	0.15	1.575	0.4	1.5	0.775		14°

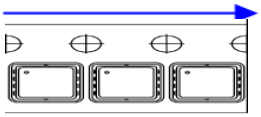
Footprint



◆ **Tape&Reel Information:2500pcs/Reel**

(Dimension in millimeter)



產品別	EDFN 5x6
Reel尺寸	13"
編帶方式	FEED DIRECTION 
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	01:01
內盒滿箱數	2.5K
內/外箱比	10:01
外箱滿箱數	25K

★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Johnson	Sam	2020/7/8
A.0	Adjust Junction-to-Case data	Johnson	Sam	2020/8/12