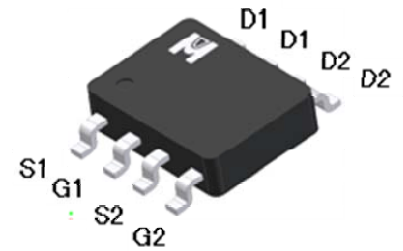
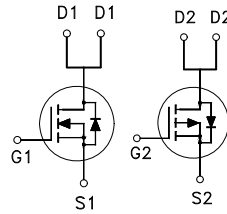


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	30V	-30V
$R_{DS(on) (MAX.)}$	28m Ω	40m Ω
I_D	7A	-6A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			± 20	± 20	
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	7	-6	A
	$T_A = 100^\circ\text{C}$		6	-5	
Pulsed Drain Current ¹		I_{DM}	28	-24	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2		W
	$T_A = 100^\circ\text{C}$		0.8		
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$ $V_{GS} = 0V, I_D = -250\mu A$	N-CH	30		V
			P-CH	-30		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$ $V_{DS} = V_{GS}, I_D = -250\mu A$	N-CH	1.0	1.5	3.0
			P-CH	-1.0	-1.5	-3.0
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$ $V_{DS} = 0V, V_{GS} = \pm 20V$	N-CH			± 100
			P-CH			± 100
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$ $V_{DS} = -24V, V_{GS} = 0V$	N-CH			1
			P-CH			-1
			N-CH			25
			P-CH			-25
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$ $V_{DS} = -5V, V_{GS} = -10V$	N-CH	7		A
			P-CH	-6		
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 7A$ $V_{GS} = -10V, I_D = -6A$ $V_{GS} = 4.5V, I_D = 6A$ $V_{GS} = -4.5V, I_D = -5A$	N-CH		24	28
			P-CH		35	40
			N-CH		33	40
			P-CH		55	65
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 7A$ $V_{DS} = -5V, I_D = -6A$	N-CH		14	S
			P-CH		16	
DYNAMIC						
Input Capacitance	C_{iss}	N-CH $V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$ P-CH $V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	N-CH		520	pF
Output Capacitance	C_{oss}		P-CH		820	
			N-CH		88	
Reverse Transfer Capacitance	C_{rss}		P-CH		122	
			N-CH		62	
			P-CH		97	



Total Gate Charge ^{1,2}	Q_g	N-CH $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 7A$ P-CH $V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -6A$	N-CH		11.5		nC	
Gate-Source Charge ^{1,2}	Q_{gs}		P-CH		9			
Gate-Drain Charge ^{1,2}	Q_{gd}		N-CH		1.6			
			P-CH		2.2			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		N-CH		11			nS
			P-CH		10			
Rise Time ^{1,2}	t_r	$I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$	N-CH		16			
			P-CH		15			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$		P-CH $V_{DS} = -10V,$	N-CH		36		
				P-CH		28		
Fall Time ^{1,2}	t_f	$I_D = -1A, V_{GS} = -10V, R_{GS} = 6\Omega$	N-CH		20			
			P-CH		15			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ C$)								
Continuous Current	I_S		N-CH			2.3	A	
			P-CH			-2.3		
Pulsed Current ³	I_{SM}		N-CH			9.2		
			P-CH			-9.2		
Forward Voltage ¹	V_{SD}		$I_F = I_S, V_{GS} = 0V$	N-CH			1.3	V
				P-CH			-1.3	

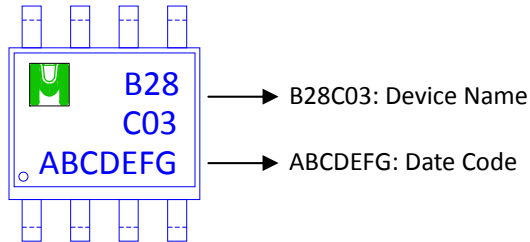
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

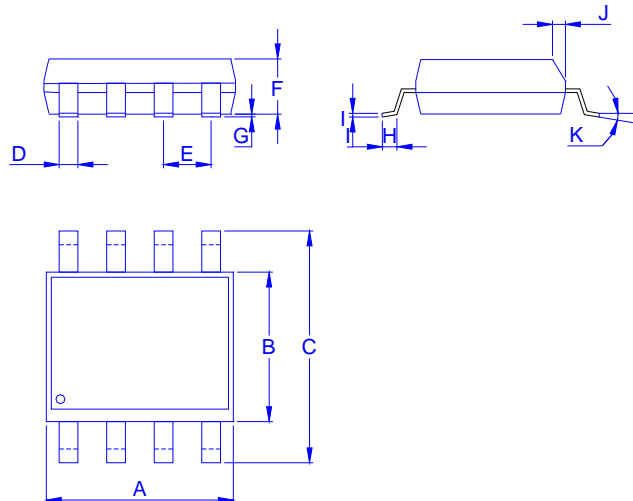
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB28C03G for SOP-8



Outline Drawing

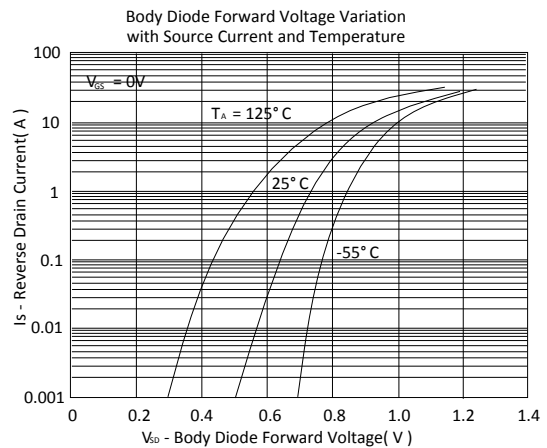
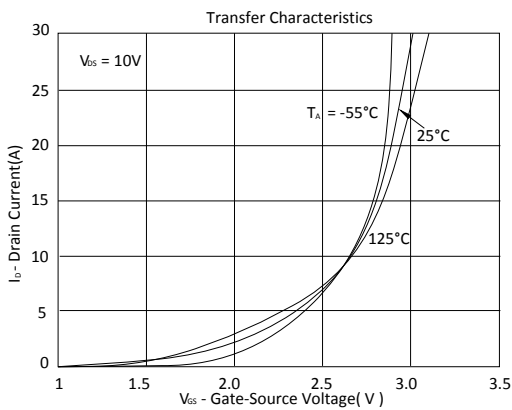
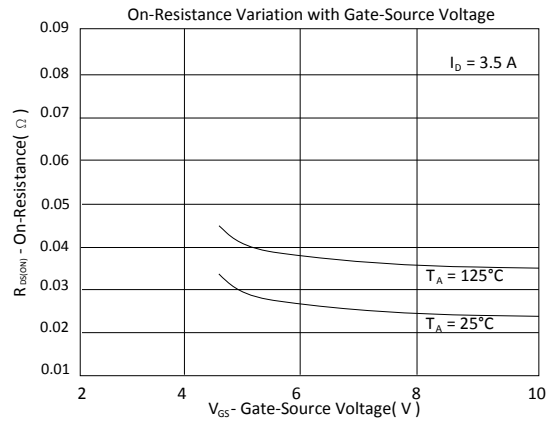
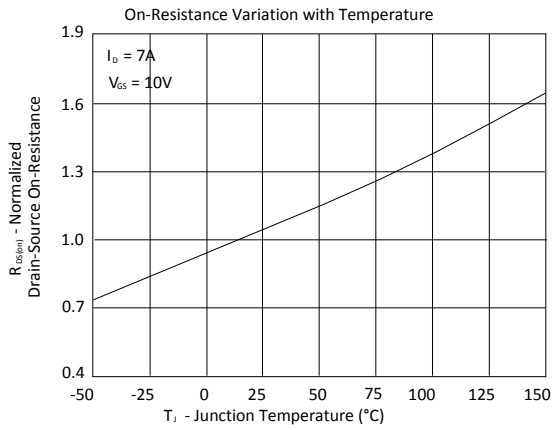
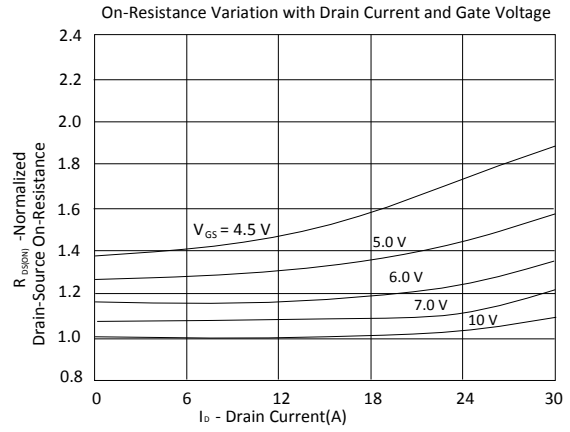
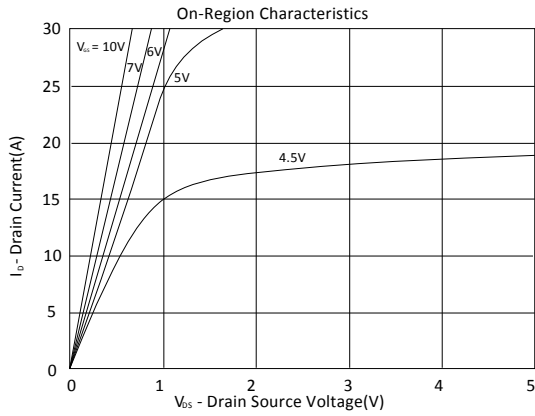


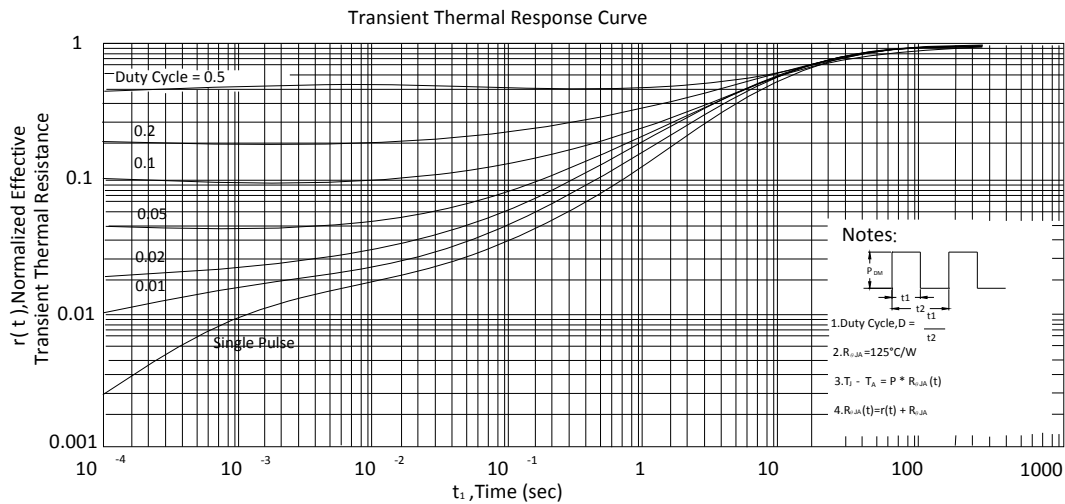
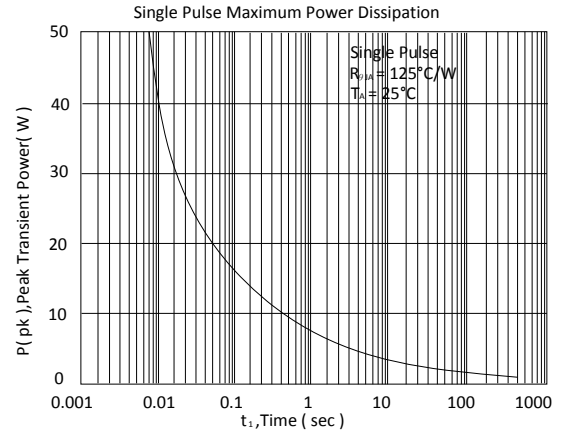
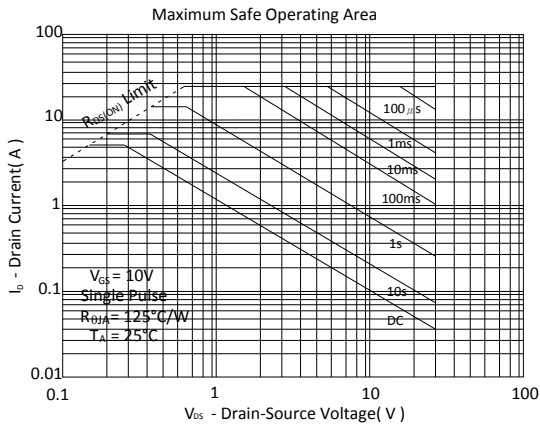
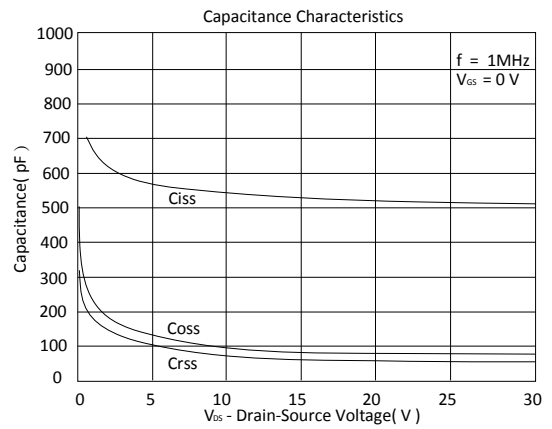
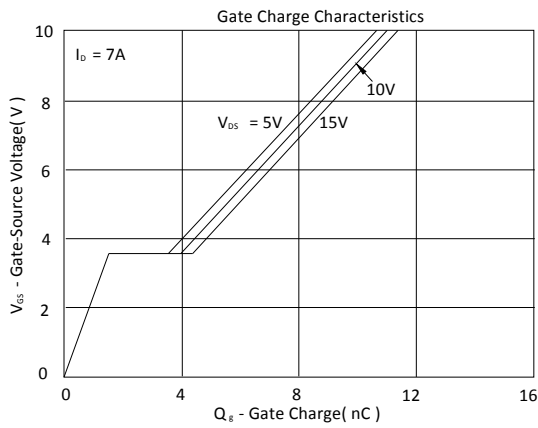
Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



N-Channel







P-Channel

