杰力科技股份有限公司
Excelliance MOS Corporation (Preliminary)

EMB03K03HP

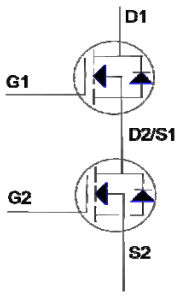
N-Channel Logic Level Enhancement Mode Field Effect Transistor

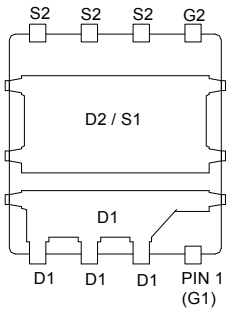
Product Summary:

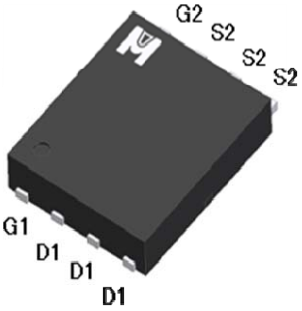
	N-CH-Q1	N-CH-Q2
BV_{DSS}	30V	30V
$R_{DSON\ (MAX.)}$	7mΩ	3.5mΩ
I_D	15A	25A

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free







GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			Q1	Q2	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	15	25	A
	T_C = 100 °C		12	18	
Pulsed Drain Current[1]		I_{DM}	60	100	
Avalanche Current		I_{AS}	15	25	
Avalanche Energy	L = 0.1mH, R_G=25Ω	E_{AS}	11.25	31.25	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	5.62	15.62	
Power Dissipation	T_C = 25 °C	P_D	48	100	W
	T_C = 100 °C		19	40	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM		UNIT
Junction-to-Case	$R_{\theta JC}$	Steady State		2.6	1.25	°C / W
Junction-to-Ambient	$R_{\theta JA}$	Steady State		62	55	
	$R_{\theta JA}$	t ≦ 10 s		27	24	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

$R_{\theta JA}$ when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q1	30			V
			Q2	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.5	3	
			Q2	1	1.5	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	nA
			Q2			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q1			1	μA
			Q2			1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C	Q1			25	
			Q2			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	Q1	15			A
			Q2	25			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 12A	Q1		5.5	7	mΩ
		V_{GS} = 10V, I_D = 20A	Q2		2.5	3.5	
		V_{GS} = 4.5V, I_D = 9A	Q1		7	9.5	
		V_{GS} = 4.5V, I_D = 15A	Q2		3.5	4.7	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 13A	Q1		50		S
		V_{DS} = 5V, I_D = 20A	Q2		95		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q1		975		pF
			Q2		2200		
Output Capacitance	C_{oss}		Q1		168		
			Q2		427		
Reverse Transfer Capacitance	C_{rss}		Q1		95		
			Q2		231		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz	Q1		2.5		Ω
			Q2		2.5		
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DD} = 15V, V_{GS} = 10V, I_D = 10A	Q1		17		nC
			Q2		32		
	Q_g(V_{GS}=4.5V)		Q1		8.7		
			Q2		17		

Gate-Source Charge[1,2]	Q_{gs}	V_{DD} = 15V, V_{GS} = 10V, I_D = 10A	Q1		3		
			Q2		4.1		
Gate-Drain Charge[1,2]	Q_{gd}		Q1		2.8		
			Q2		8.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7Ω	Q1		8		nS
			Q2		15		
Rise Time[1,2]	t_r		Q1		10		
			Q2		10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		Q1		20		
			Q2		50		
Fall Time[1,2]	t_f		Q1		15		
			Q2		15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		Q1			15	A
			Q2			25	
Pulsed Current[3]	I_{SM}		Q1			60	
			Q2			100	
Forward Voltage[1]	V_{SD}	I_F = 10A, V_{GS} = 0V	Q1			1.2	V
			Q2			1.2	
Reverse Recovery Time	t_{rr}	Q1 I_F = 10A, dI_F/dt = 100A / μS	Q1		20		nS
			Q2		30		
Reverse Recovery Charge	Q_{rr}	Q2 I_F = 10A, dI_F/dt = 100A / μS	Q1		11		nC
			Q2		10		

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

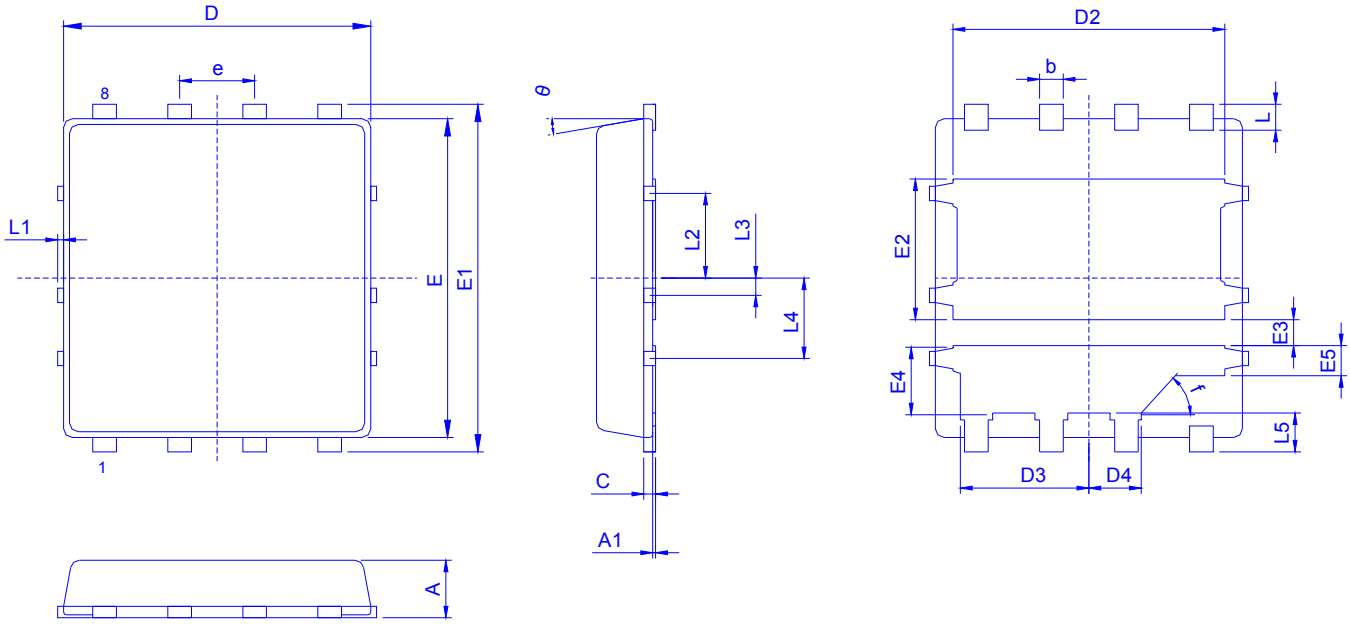
Ordering & Marking Information:

Device Name: EMB03K03HP for Asymmetric Dual EDFN 5 x 6

→ B03K03: Device Name

→ ABCDEFG: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D2	D3	D4	E	E1	E2	E3	E4	E5
Min.	0.85	0.00	0.35	0.15		4.5	2.125	0.835			2.4	0.40	1.125	0.475
Typ.	0.90		0.40	0.20	5.2	4.6	2.175	0.885	5.55	6.05	2.45	0.45	1.175	0.525
Max.	1.00	0.05	0.45	0.25		4.7	2.225	0.935			2.5	0.50	1.225	0.575

Dimension	e	L	L1	L2	L3	L4	L5	F	θ
Min.		0.35	0	1.375	0.2	1.3	0.575		0°
Typ.	1.27	0.45		1.475	0.3	1.4	0.675	45°	
Max.		0.55	0.1	1.575	0.4	1.5	0.775		10°

Recommended minimum pads