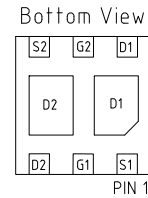
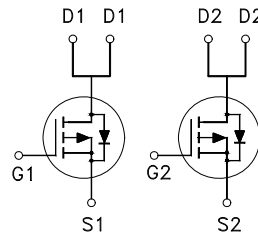


Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DS(on)}$ (MAX.)	65m Ω
I_D	-3A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 8	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-3	A
	$T_A = 70^\circ\text{C}$		-2	
Pulsed Drain Current ¹		I_{DM}	-12	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	1.9	W
	$T_A = 70^\circ\text{C}$		1.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		15	$^\circ\text{C}/\text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		65	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³65 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.35	-0.60	-0.85	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-3			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -3A		52	65	mΩ
		V _{GS} = -2.5V, I _D = -2A		78	100	
		V _{GS} = -1.8V, I _D = -1A		100	140	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -3A		10		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		382		pF
Output Capacitance	C _{oss}			70		
Reverse Transfer Capacitance	C _{rss}			60		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -3A		7.2		nC
Gate-Source Charge ^{1,2}	Q _{gs}			1.2		
Gate-Drain Charge ^{1,2}	Q _{gd}			2.3		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -10V, I _D = -1A, V _{GS} = -4.5V, R _{GS} = 6Ω		17		nS
Rise Time ^{1,2}	t _r			32		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			37		
Fall Time ^{1,2}	t _f			32		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-3	A
Pulsed Current ³	I _{SM}				-12	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V

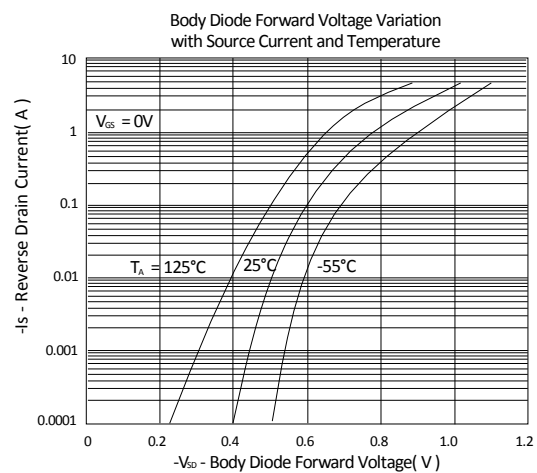
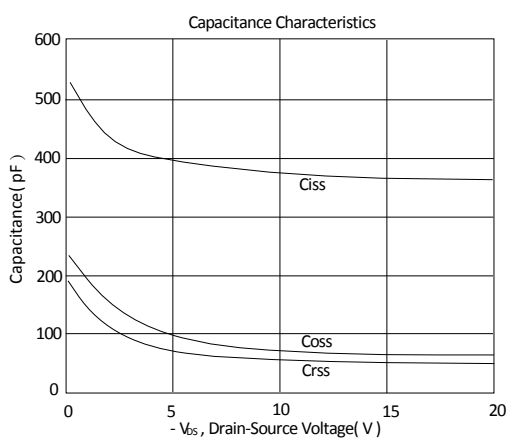
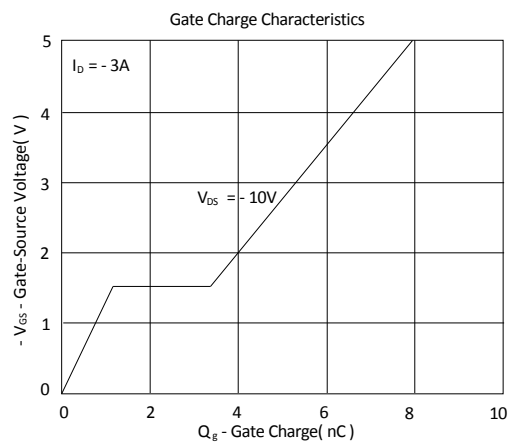
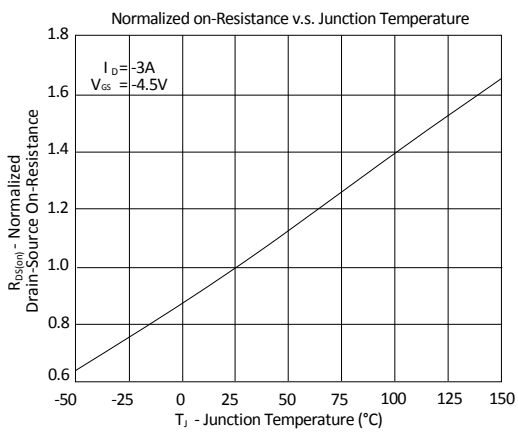
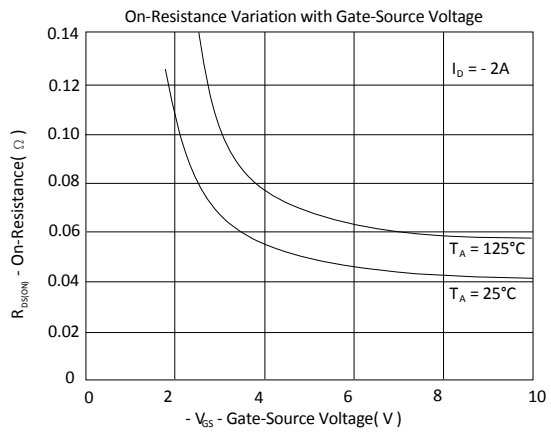
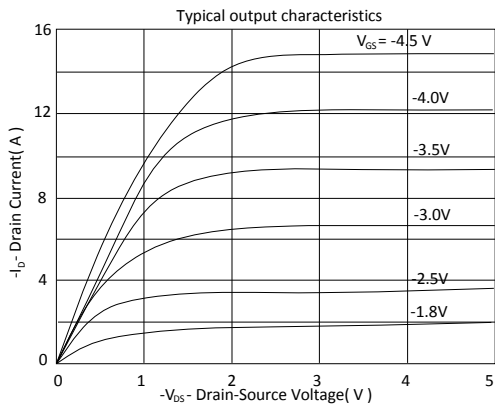
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

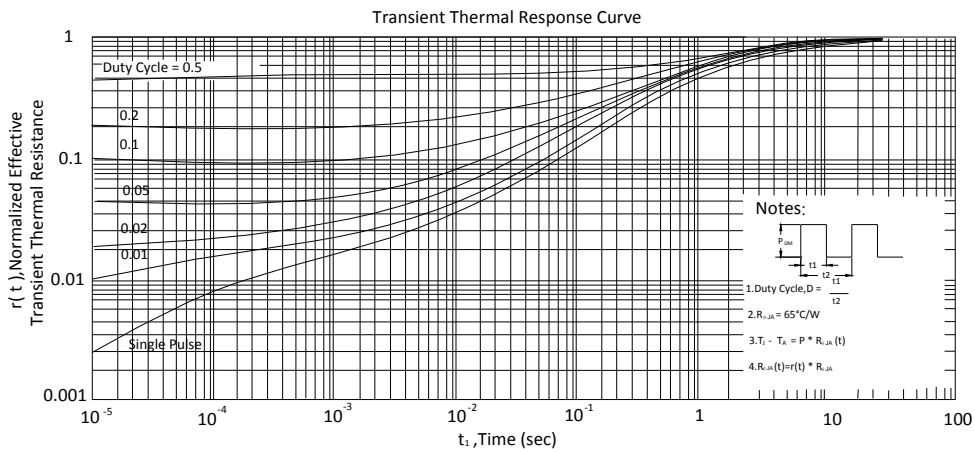
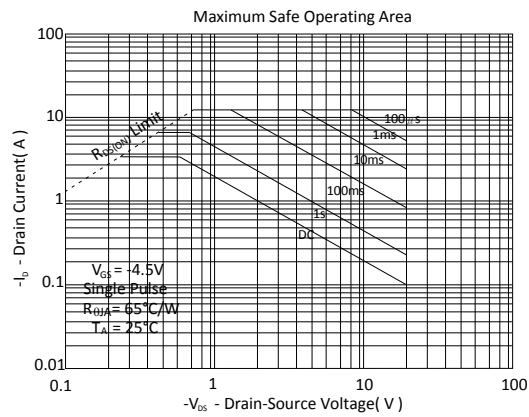
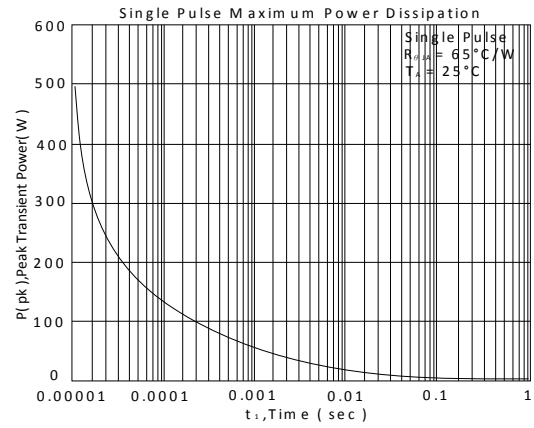
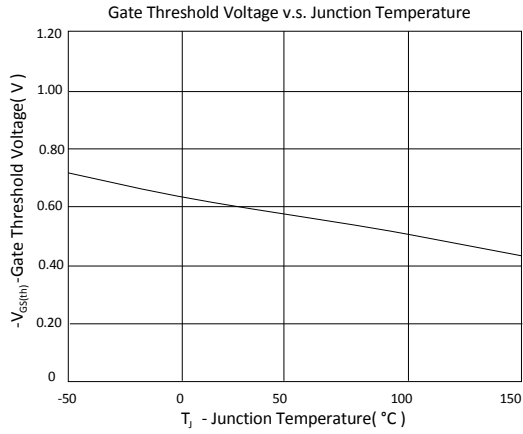
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.



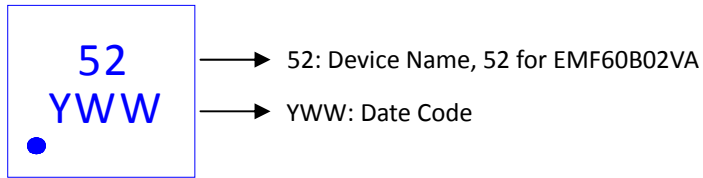
TYPICAL CHARACTERISTICS



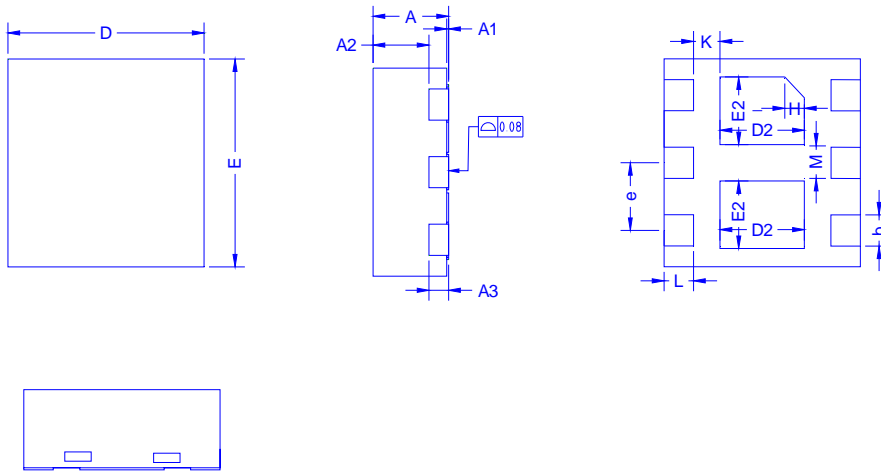


Ordering & Marking Information:

Device Name: EMF60B02VA for EDFN 2 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	A3	b	D	E	D2	E2	e	H	K	L	M
Min.	0.70	0.00	0.50	0.20 REF	0.25	1.90	1.90	0.76	0.55	0.55	0.20 REF	0.17	0.25	0.25
Max.	0.80	0.05	0.60		0.35	2.10	2.10	0.96	0.75	0.75		0.37	0.35	0.45

Recommended minimum pads

